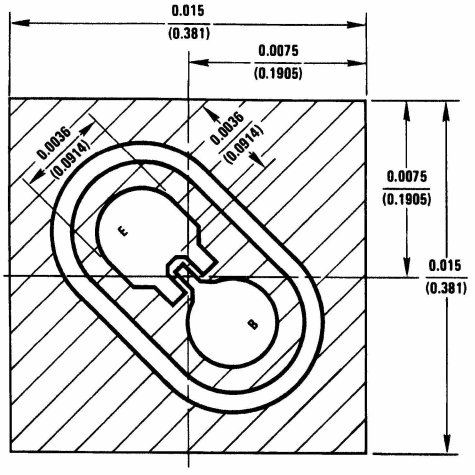
National Semiconductor

Process 65
PNP High Speed Switch



TL/G/10038–14

DESCRIPTION

Process 65 is an overlay, double-diffused, gold doped, silicon epitaxial device. Complement to Process 21.

APPLICATION

This device was designed for very high speed saturate switching at collector currents to 50 mA.

PRINCIPAL DEVICE TYPES

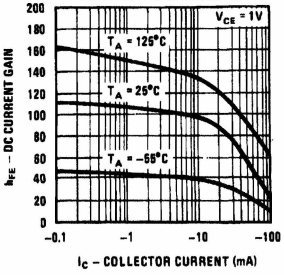
TO-18 EBC: 2N4208
TO-92 EBC: PN3640, 2N5771
TO-236: MMBT3640
TO-116: MPQ3640
16-SOIC: MMPQ3640

ELECTRICAL CHARACTERISTICS (T_A = 25°C)

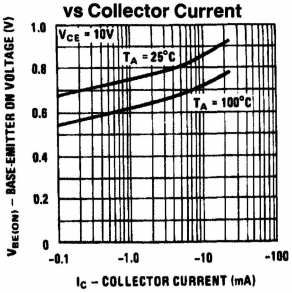
Symbol	Conditions	Min	Typ	Max	Units
t_{OFF}	I_C = 10 mA, I_{B2} = 1 mA *(Figure 1)*		18	25	ns
t_{ON}	I_C = 10 mA, I_{B1} = 1 mA *(Figure 1)*		11	15	ns
t_s	I_C = I_{B1} = I_{B2} = 10 mA		15	20	ns
C_{ob}	V_{CB} = 5V		2	3	pF
C_{ib}	V_{EB} = 0.5V			3.5	pF
h_{fe}	V_{CE} = 10V, I_C = 10 mA, f = 100 MHz	6.5	9		
h_{FE}	I_C = 1 mA, V_{CE} = 1V I_C = 10 mA, V_{CE} = 1V I_C = 50 mA, V_{CE} = 1V I_C = 100 mA, V_{CE} = 1V I_C = 1 mA, V_{CE} = 0.5V I_C = 10 mA, V_{CE} = 0.3V	20 30 25 20 20 20	 85 75	 150	
$V_{CE(SAT)}$	I_C = 1 mA, I_B = 0.1 mA I_C = 10 mA, I_B = 1 mA I_C = 50 mA, I_B = 5 mA			0.15 0.20 0.50	V V V
$V_{BE(SAT)}$	I_C = 1 mA, I_B = 0.1 mA I_C = 10 mA, I_B = 1 mA I_C = 50 mA, I_B = 5 mA			0.8 0.95 1.5	V V V
BV_{CEO}	I_C = 3 mA	15			V
BV_{CBO}	I_C = 100 μA	15			V
BV_{EBO}	I_C = 10 μA	4.5			V
I_{CBO}	V_{CB} = 10V			100	nA
I_{EBO}	V_{EB} = 3V			100	nA

Process 65

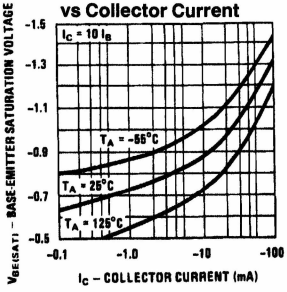
DC Current Gain vs Collector Current



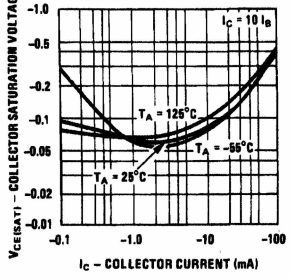
Base-Emitter ON Voltage vs Collector Current



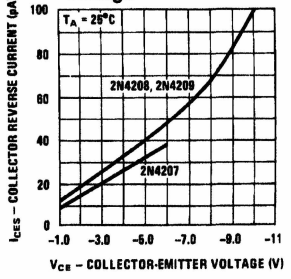
Base Saturation Voltage vs Collector Current



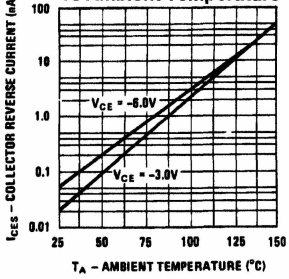
Collector Saturation Voltage vs Collector Current



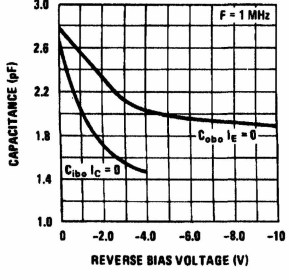
Collector Reverse Current vs Collector-Emitter Voltage



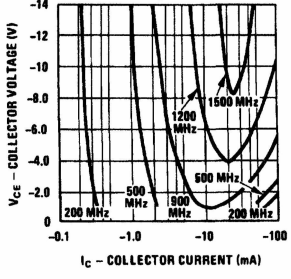
Collector Reverse Current vs Ambient Temperature



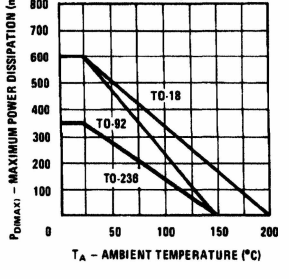
Input and Output Capacitance vs Reverse Bias Voltage



Contours of Constant Gain Bandwidth Product (f_T)



Maximum Power Dissipation vs Ambient Temperature



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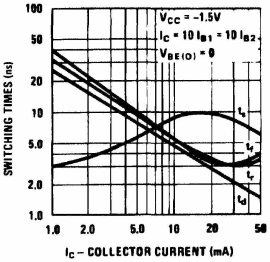
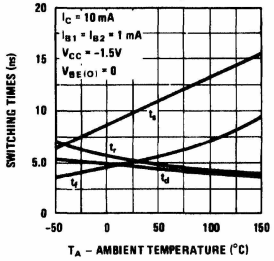
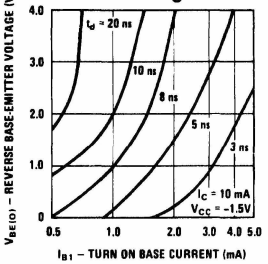
Switching Times vs Collector Current



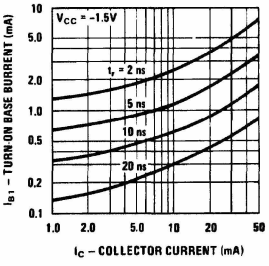
Switching Times vs Ambient Temperature



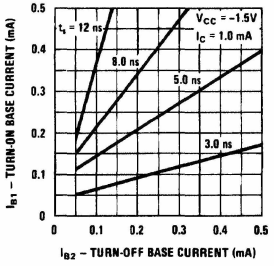
Delay Time vs Turn On Base Current and Reverse Base-Emitter Voltage



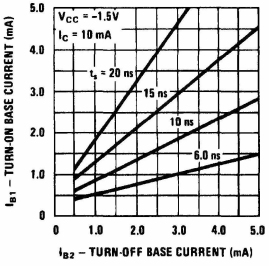
Rise Time vs Collector and Turn On Base Currents



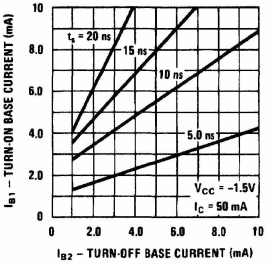
Storage Time vs Turn On and Turn Off Base Currents



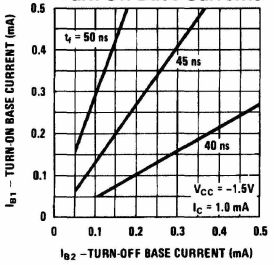
Storage Time vs Turn On and Turn Off Base Currents



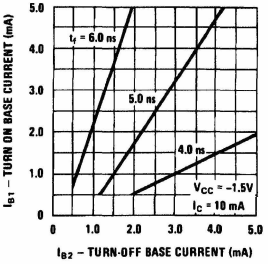
Storage Time vs Turn On and Turn Off Base Currents



Fall Time vs Turn On and Turn Off Base Currents



Fall Time vs Turn On and Turn Off Base Currents



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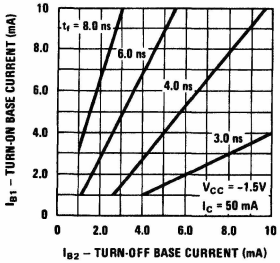
Fall Time vs Turn On and Turn Off Base Currents



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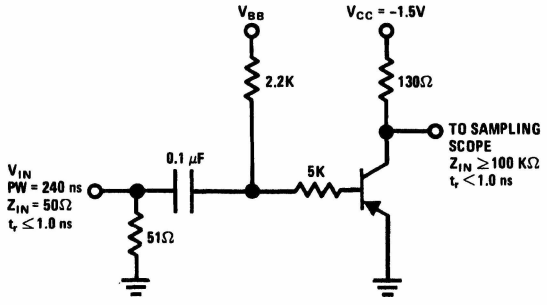
Process 65



TL/G/10038–18

t_{ON}
V_{BB} = Ground
V_{IN} = −5.8V

t_{OFF}
V_{BB} = −8.0V
V_{IN} = +9.8V

I_C = 10 mA, I_{B1} = 1.0 mA, I_{B2} = 1.0 mA

FIGURE 1. t_{ON} and t_{OFF} Test Circuit