

TL/G/10034-56

DESCRIPTION

Process 25 is an overlay, double-diffused, gold doped, silicon epitaxial device. Complement to Process 70.

APPLICATION

This device was designed for high speed core driver applications up to collector current of 1A.

PRINCIPAL DEVICE TYPES
TO-39 EBC: 2N3725

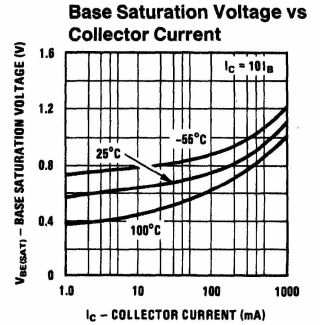
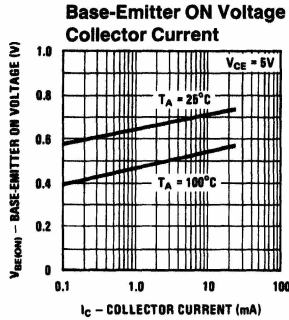
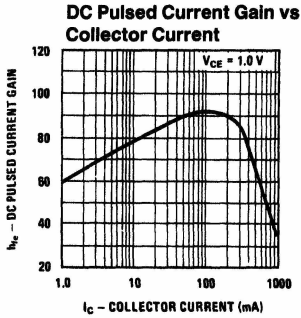
TO-237 EBC: TN3725

TO-116: MPQ3725

ELECTRICAL CHARACTERISTICS (T_A = 25°C)

Symbol	Conditions	Min	Typ	Max	Units
t _{ON}	I _C = 500 mA, I _{B1} = 50 mA (Figure 1)		12	35	ns
t _{OFF}	I _C = 500 mA, I _{B2} = 50 mA (Figure 1)		50	60	ns
h _{fe}	I _C = 50 mA, V _{CE} = 10V, f = 100 MHz	2.5	4.25		
C _{ob}	V _{CB} = 10V, f = 1 MHz		6	8	pF
C _{ib}	V _{EB} = 0.5V, f = 1 MHz			55	pF
h _{FE}	I _C = 10 mA, V _{CE} = 1V I _C = 100 mA, V _{CE} = 1V I _C = 300 mA, V _{CE} = 1V I _C = 500 mA, V _{CE} = 1V I _C = 800 mA, V _{CE} = 1V I _C = 1A, V _{CE} = 1V I _C = 800 mA, V _{CE} = 2V I _C = 1A, V _{CE} = 5V	40 45 35 25 20 15 25 25	90	150	
V _{CE(SAT)}	I _C = 10 mA, I _B = 1 mA I _C = 100 mA, I _B = 10 mA I _C = 300 mA, I _B = 30 mA I _C = 500 mA, I _B = 50 mA I _C = 800 mA, I _B = 80 mA I _C = 1A, I _B = 100 mA			0.20 0.20 0.40 0.50 0.80 1.20	V V V V V V
V _{BE(SAT)}	I _C = 10 mA, I _B = 1 mA I _C = 100 mA, I _B = 10 mA I _C = 300 mA, I _B = 30 mA I _C = 500 mA, I _B = 50 mA I _C = 800 mA, I _B = 80 mA I _C = 1A, I _B = 100 mA			0.70 0.85 1.20 1.20 1.50 1.70	V V V V V V

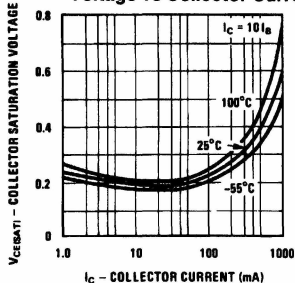
Symbol	Conditions	Min	Typ	Max	Units
BV_{CEO}	$I_C = 10 \text{ mA}$	40			V
BV_{CBO}	$I_C = 100 \mu\text{A}$	80			V
BV_{EBO}	$I_C = 10 \mu\text{A}$	6			V
I_{CBO}	$V_{CB} = 40\text{V}$			100	nA
I_{EBO}	$V_{EB} = 4\text{V}$			100	nA
$P_D(\text{max})$ TO-39 TO-237 TO-116	$T_C = 25^\circ\text{C}$	7			W
	$T_A = 25^\circ\text{C}$	1			W
	$T_A = 25^\circ\text{C}$	850			mW
	$T_A = 25^\circ\text{C}$	1			W
	(Total) (Each Transistor)	600			mW
$T_j(\text{max})$	All Metal Can Parts	200			$^\circ\text{C}$
	All Plastic Parts	150			$^\circ\text{C}$



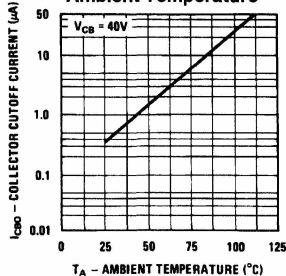
TL/G/10034-57

Process 25

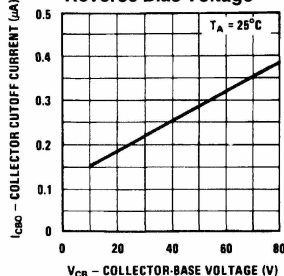
Collector Saturation Voltage vs Collector Current



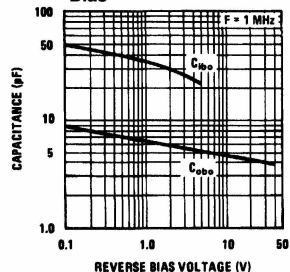
Collector Cutoff Current vs Ambient Temperature



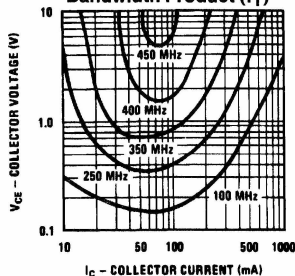
Collector Cutoff Current vs Reverse Bias Voltage



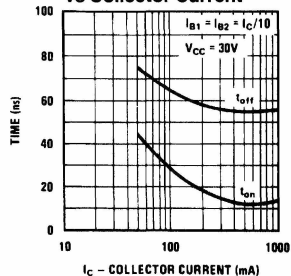
Input and Output Capacitance vs Reverse Bias



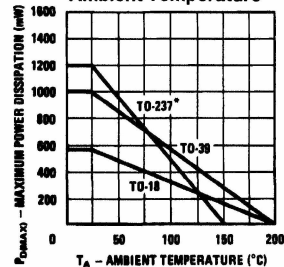
Contours of Constant Bandwidth Product (f_T)



Turn On and Turn Off Times vs Collector Current

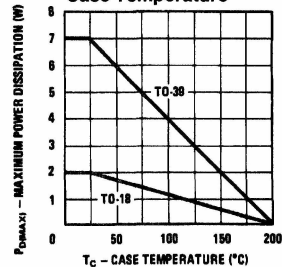


Maximum Power Dissipation vs Ambient Temperature

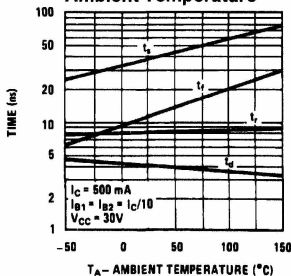


* One square inch of copper run

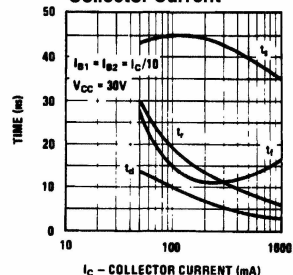
Maximum Power Dissipation vs Case Temperature



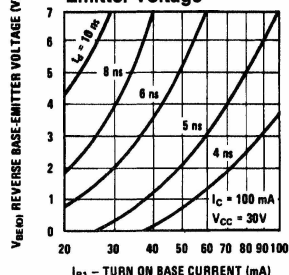
Switching Times vs Ambient Temperature



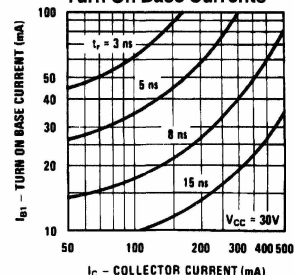
Switching Times vs Collector Current



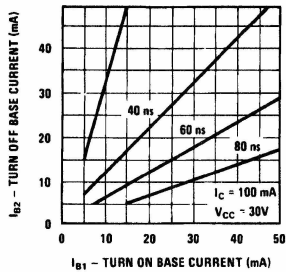
Delay Time vs Turn On Base Current and Reverse Base-Emitter Voltage



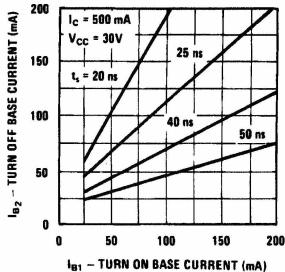
Rise Time vs Collector and Turn On Base Currents



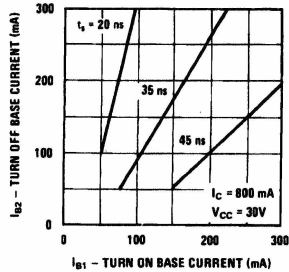
Storage Time vs Turn On and Turn Off Base Currents



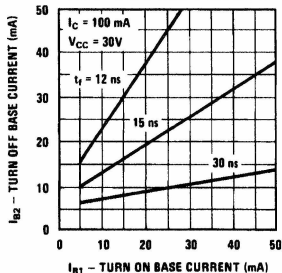
Storage Time vs Turn On and Turn Off Base Currents



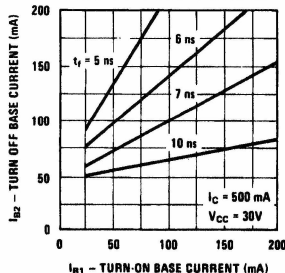
Storage Time vs Turn On and Turn Off Base Currents



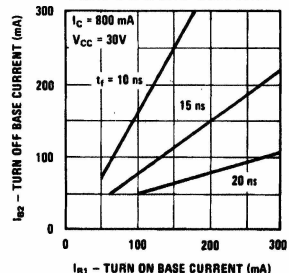
Fall Time vs Turn On and Turn Off Base Currents



Fall Time vs Turn On and Turn Off Base Currents

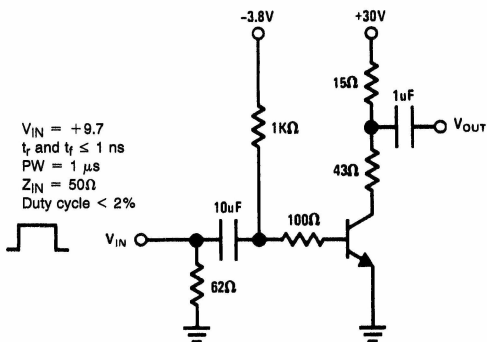


Fall Time vs Turn On and Turn Off Base Currents



TL/G/10034-59

Switching Time Test Circuit



$V_{IN} = +9.7$
 t_r and $t_f \leq 1$ ns
 $PW = 1 \mu s$
 $Z_{IN} = 50 \Omega$
 Duty cycle < 2%

To sampling scope
 $t_r < 1$ ns
 $Z_{IN} \geq 100$ k Ω

FIGURE 1. $I_C = 500$ mA, $I_{B1} = 50$ mA, $I_{B2} = 50$ mA

TL/G/10034-60