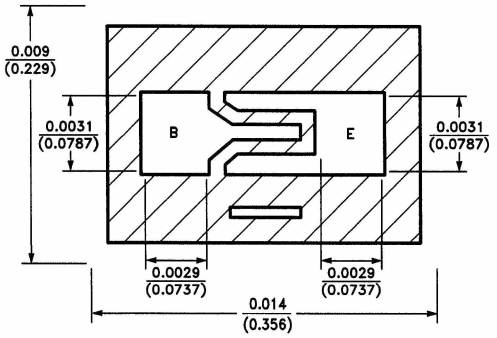
National Semiconductor

Process 21
NPN High Speed Switch



TL/G/10034–25

DESCRIPTION

Process 21 is an overlay, double-diffused, gold doped, silicon epitaxial device. Complement to Process 65.

APPLICATION

This device was designed for high speed saturated switching at collector currents of 10 mA to 100 mA.

PRINCIPAL DEVICE TYPES

TO-18 EBC: 2N2369, 2N2369A

TO-92 EBC: PN2369

TO-236: MMBT2369

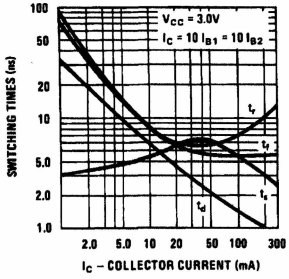
16-SOIC: MMPQ2369

ELECTRICAL CHARACTERISTICS (T_A = 25°C)

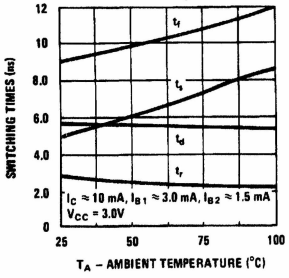
Symbol	Conditions	Min	Typ	Max	Units
t_s	$I_{B1} = I_{B2} = I_C$ = 10 mA *(Figure 1)*		7	13	ns
t_{ON}	I_C = 10 mA, I_{B1} = 3 mA *(Figure 2)*		9	12	ns
t_{OFF}	I_C = 10 mA, I_{B2} = 1.50 mA *(Figure 2)*		12	20	ns
h_{fe}	I_C = 10 mA, V_{CE} = 10V, f = 100 MHz	4.5	6.5		
C_{ob}	V_{CB} = 5V, f = 1 MHz		2.0	4.0	pF
C_{ib}	V_{EB} = 0.5V, f = 1 MHz			5.0	pF
h_{FE}	I_C = 1 mA, V_{CE} = 1V	30			
	I_C = 10 mA, V_{CE} = 1V	35	70	150	
	I_C = 50 mA, V_{CE} = 1V	30	55	150	
	I_C = 100 mA, V_{CE} = 1V	20			
	I_C = 10 mA, V_{CE} = 0.35V	30			
	I_C = 30 mA, V_{CE} = 0.4V	30			
$V_{CE(SAT)}$	I_C = 10 mA, I_B = 1 mA			0.2	V
	I_C = 100 mA, I_B = 10 mA			0.5	V
$V_{BE(SAT)}$	I_C = 10 mA, I_B = 1 mA			0.85	V
	I_C = 100 mA, I_B = 10 mA			1.5	V
BV_{CEO}	I_C = 10 mA	12			V
BV_{CBO}	I_C = 10 μA	30			V
BV_{EBO}	I_E = 10 μA	4.5			V
I_{CBO}	V_{CB} = 20V			100	nA
I_{EBO}	V_{EB} = 3V			100	nA
$P_{D(max)}$					
TO-18	T_A = 25°C	600			mW
TO-92	T_A = 25°C	600			mW
TO-236	T_A = 25°C	350			mW

Process 21

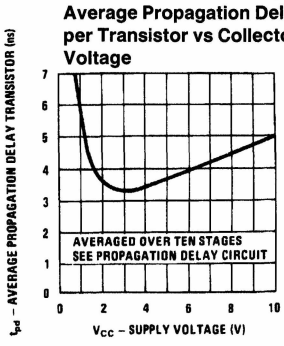
Switching Times vs Collector Current



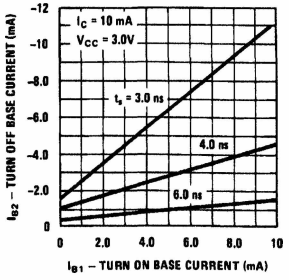
Switching Times vs Ambient Temperature



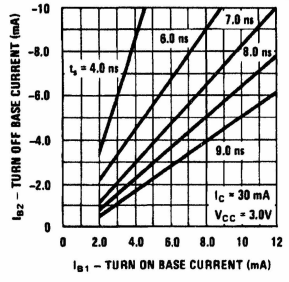
Average Propagation Delay per Transistor vs Collector Voltage



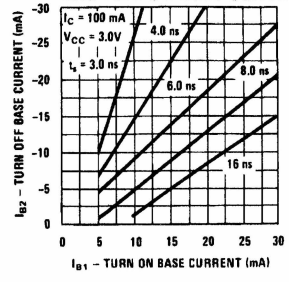
Storage Time vs Turn On and Turn Off Base Currents



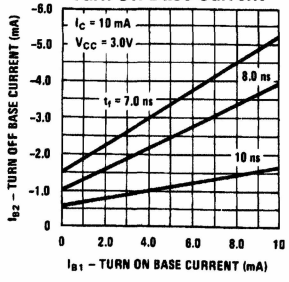
Storage Time vs Turn On and Turn Off Base Currents



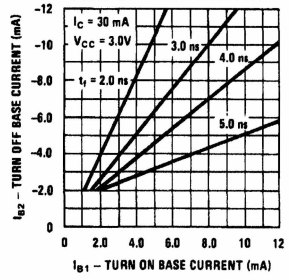
Storage Time vs Turn On and Turn Off Base Currents



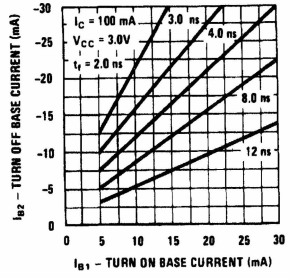
Fall Time vs Turn On and Turn Off Base Current



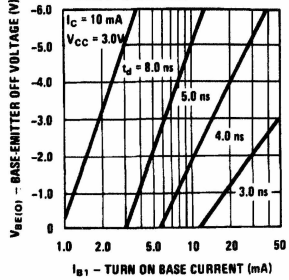
Fall Time vs Turn On and Turn Off Base Current



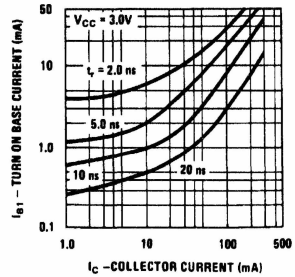
Fall Time vs Turn On and Turn Off Base Current



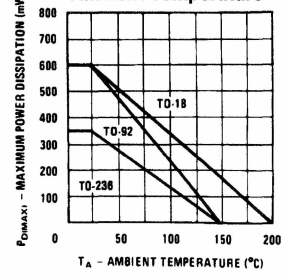
Delay Time vs Base-Emitter Off Voltage and Turn On Base Current



Rise Time vs Turn On Base Current and Collector Current



Maximum Power Dissipation vs Ambient Temperature



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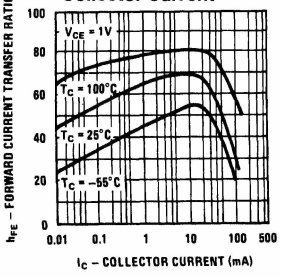
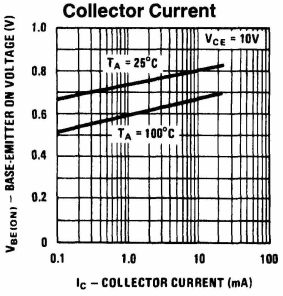
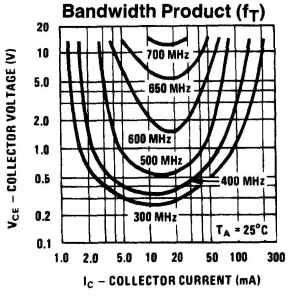
DC Current Gain vs Collector Current



Base-Emitter On Voltage vs Collector Current



Contours of Constant Gain Bandwidth Product (f_T)



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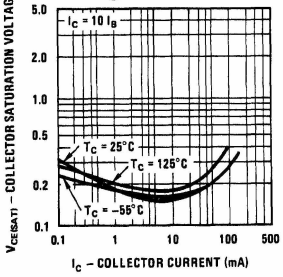
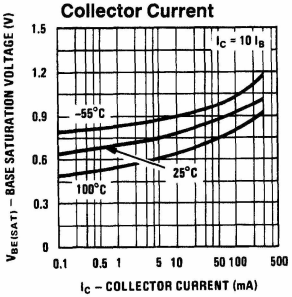
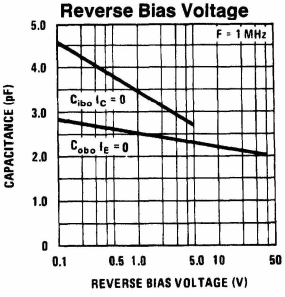
Collector Saturation Voltage vs Collector Current



Base Saturation Voltage vs Collector Current



Emitter Transition and Output Capacitances vs Reverse Bias Voltage



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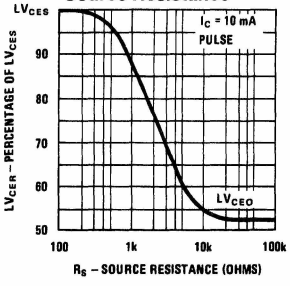
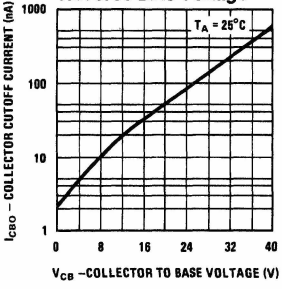
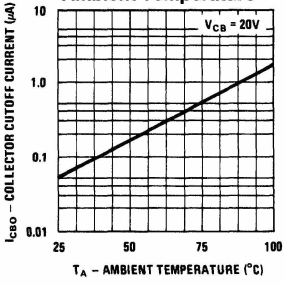
Lower Limiting Voltage vs Source Resistance



Collector Cutoff Current vs Reverse Bias Voltage



Collector Cutoff Current vs Ambient Temperature



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Process 21

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Pulse generator
V_{IN} rise time < 1 ns
Source impedance = 50Ω
PW ≥ 300 ns
Duty cycle < 2%

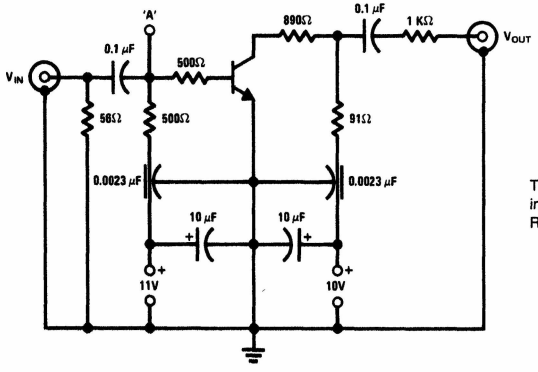

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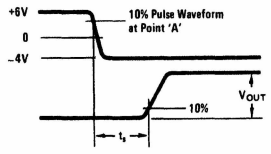
FIGURE 1. Charge Storage Time Measurement Circuit



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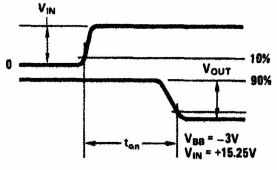
To sampling oscilloscope
input impedance = 50Ω
Rise Time ≤ 1 ns



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Pulse generator
V_{IN} rise time < 1 ns
Source impedance = 50Ω
PW ≥ 300 ns
Duty cycle < 2%

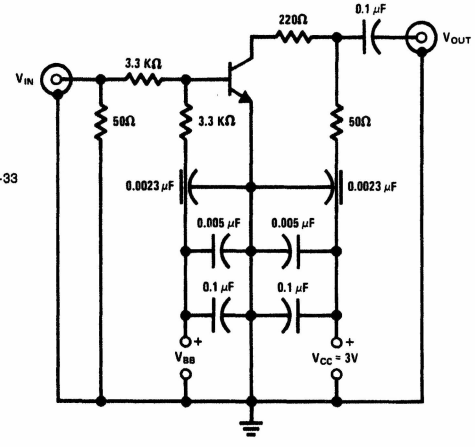

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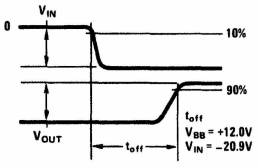
FIGURE 2. t_{ON}, t_{OFF} Measurement Circuit



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To sampling oscilloscope
input impedance = 50Ω
Rise Time ≤ 1 ns