

TL/G/10040-14

DESCRIPTION

These dice are n-channel, enhancement mode, power MOSFETs designed especially for high power, high speed applications, such as power supplies, AC and DC motor control and high energy pulse circuits.

This process is available in the following device types:

TO-220 (Case 37)

IRF610

IRF611

IRF612

IRF613

MTP2N18

MTP2N20

Electrical Characteristics $T_C = 25^\circ\text{C}$ (unless otherwise noted)

Symbol	Parameter	Test Conditions	Min	Max	Units
V_{DS}	Drain to Source Voltage (Note 1)	$I_D = 250 \mu\text{A}; V_{GS} = 0\text{V}$	200		V
I_{DSS}	Zero Gate Voltage Drain	$V_{DS} = \text{Rated Voltage}$ $V_{GS} = 0\text{V}$		250	μA
I_{GSS}	Gate Leakage Current	$V_{DS} = \pm 20\text{V}; V_{GS} = 0\text{V}$		100	nA
$V_{GS(TH)}$	Gate Threshold Voltage	$I_D = 250 \mu\text{A}; V_{DS} = V_{GS}$	2.0	4.0	V
$R_{DS(ON)}$	Static On-Resistance (Note 2)	$V_{GS} = 10\text{V}; I_D = 1.25\text{A}$		1.5	Ω
g_{FS}	Forward Transconductance	$V_{DS} = 10\text{V}; I_D = 1.25\text{A}$	0.8		Siemens
C_{iss}	Input Capacitance	$V_{DS} = 25\text{V}; V_{GS} = 0\text{V}$ $f = 1 \text{ MHz}$		200	pF
C_{oss}	Output Capacitance			80	pF
C_{rss}	Reverse Transfer			25	pF
$t_{d(on)}$	Turn-On Delay Time (Note 3)	$V_{DD} = 50\text{V}; I_D = 1.25\text{A}$ $V_{GS} = 10\text{V}; R_{GEN} = 50\Omega$		15	ns
t_r	Rise Time	$R_{GS} = 50\Omega$		25	ns
$t_{d(off)}$	Turn-Off Delay Time			15	ns
t_f	Fall Time			15	ns
Q_g	Total Gate Charge	$V_{GS} = 10\text{V}; I_D = 3.0\text{A}$ $V_{DD} = 45\text{V}$		7.5	nC

Note 1: $T_J = +25^\circ\text{C}$ to $+150^\circ\text{C}$.

Note 2: Pulse Test: Pulse Width $\leq 80 \mu\text{s}$, Duty Cycle $\leq 1\%$.

Note 3: Switching time measurements performed on LEM TR-58 test equipment.

Typical Performance Characteristics

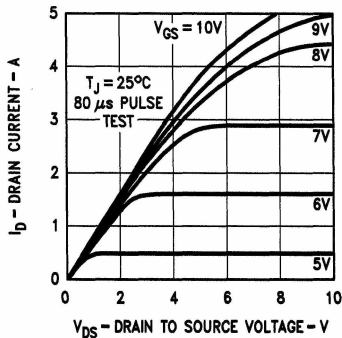


FIGURE 1. Output Characteristics

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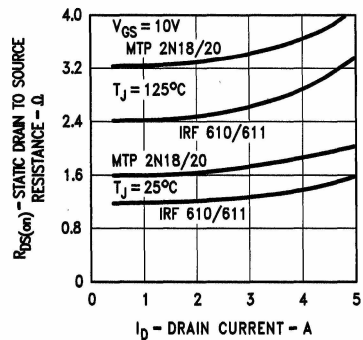


FIGURE 2. Static Drain to Source Resistance vs Drain Current

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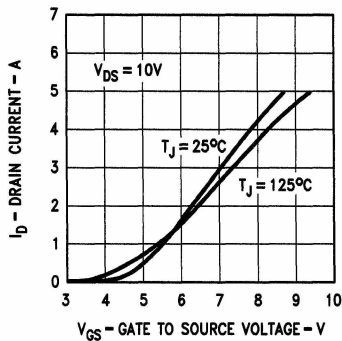


FIGURE 3. Transfer Characteristics

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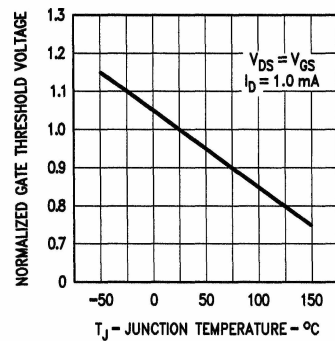


FIGURE 4. Temperature Variation of Gate to Source Threshold Voltage

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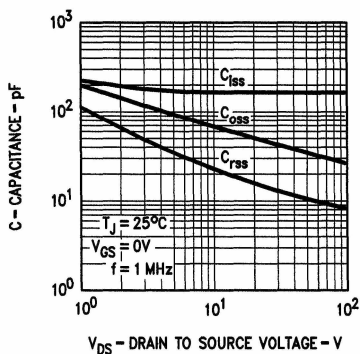


FIGURE 5. Capacitance vs Drain to Source Voltage

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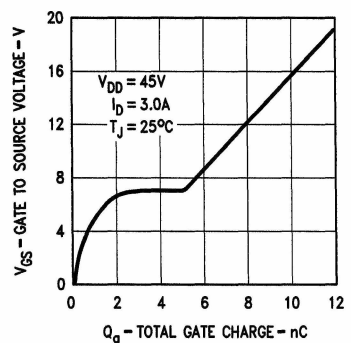
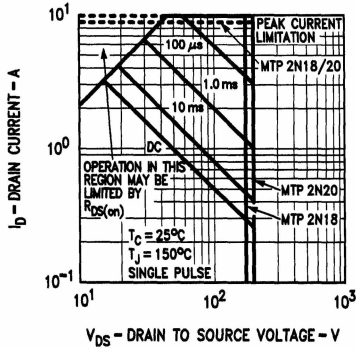


FIGURE 6. Gate to Source Voltage vs Total Gate Charge

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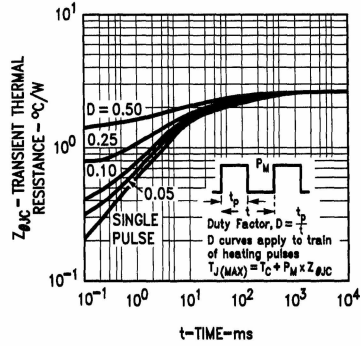
Process A2

Typical Performance Characteristics (Continued)



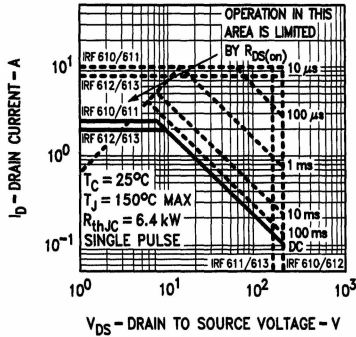
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FIGURE 7. Forward Biased Safe Operating Area for MTP2N18/2N20



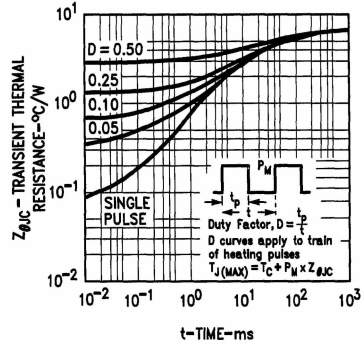
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FIGURE 8. Transient Thermal Resistance vs Time for MTP2N18/2N20



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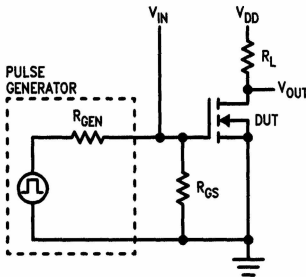
FIGURE 9. Forward Biased Safe Operating Area for IRF610-613



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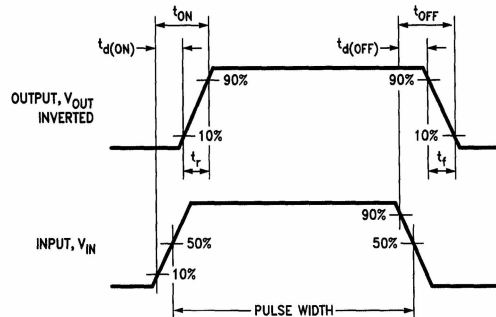
FIGURE 10. Transient Thermal Resistance vs Time for IRF610-613

Typical Electrical Characteristics



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FIGURE 11. Switching Test Circuit



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FIGURE 12. Switching Waveforms