

TL/G/10035-16

### DESCRIPTION

Process 83 is a monolithic dual JFET with a diode isolated substrate. It is intended for operational amplifier input buffer applications. Processing results in low input bias current and virtually unmeasurable offset current. Likewise matching characteristics are virtually independent of operating current and voltage, providing design flexibility. Most GP 2N types are sorted from this family.

### Electrical Characteristics (T<sub>A</sub> = 25°C)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
BV <sub>GS</sub>	Gate-Source Breakdown Voltage	V <sub>DS</sub> = 0V, I <sub>G</sub> = -1 μA	-50	-70		V
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	V <sub>DS</sub> = 15V, V <sub>GS</sub> = 0V	0.5	2.5	8.0	mA
g <sub>fs</sub>	Forward Transconductance	V <sub>DS</sub> = 15V, V <sub>GS</sub> = 0V	1.0	2.5	5.0	mmho
V <sub>GS(OFF)</sub>	Pinch Off Voltage	V <sub>DS</sub> = 15V, I <sub>D</sub> = 1 nA	-0.5	-2.0	-4.5	V
I <sub>G</sub>	Gate Current	V <sub>DG</sub> = 20V, I <sub>D</sub> = 0.2 mA		3.0	50	pA
g <sub>fs</sub>	Forward Transconductance	V <sub>DG</sub> = 15V, I <sub>D</sub> = 0.2 mA	600	850		μmhos
g <sub>os</sub>	Output Conductance	V <sub>DG</sub> = 15V, I <sub>D</sub> = 0.2 mA		1.0	5.0	μmhos
r <sub>DS(ON)</sub>	ON Resistance	V <sub>DS</sub> = 100 mV, V <sub>GS</sub> = 0V		450		Ω
e <sub>n</sub>	Noise Voltage	V <sub>DG</sub> = 15V, I <sub>D</sub> = 0.2 mA, f = 100 Hz		10	50	nV/√Hz
V <sub>GS1</sub> - V <sub>GS2</sub>	Differential Match	V <sub>DG</sub> = 15V, I <sub>D</sub> = 0.2 mA		7.0	25	mV
ΔV <sub>GS1</sub> - V <sub>GS2</sub>	Differential Match Drift	V <sub>DG</sub> = 15V, I <sub>D</sub> = 0.2 mA		10	50	μV/°C
CMRR	Common-Mode Rejection	V <sub>DG</sub> = 15V, I <sub>D</sub> = 0.2 mA	80	95		dB
C <sub>rs</sub>	Feedback Capacitance	V <sub>DG</sub> = 15V, I <sub>D</sub> = 0.2 mA, f = 1 MHz		1.0	1.2	pF
C <sub>is</sub>	Input Capacitance	V <sub>DG</sub> = 15V, I <sub>D</sub> = 0.2 mA, f = 1 MHz		3.4	4.0	pF

# Process 83

This process is available in the following device types. \*Denotes preferred parts.

### TO-71 (NS Package 12)

*2N3954	*2N5196	U231
*2N3954A	*2N5197	U232
*2N3955	*2N5198	U233
*2N3955A	*2N5199	U234
*2N3956	2N5452	U235
*2N3957	2N5453	
*2N3958	2N5454	
2N5045	*2N5545	
2N5046	*2N5546	
2N5047	*2N5547	

### 8-Pin MiniDIP (NS Package 60)

J410
J411
J412

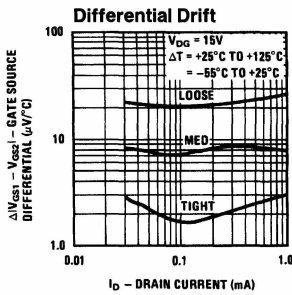
Pin	60
1	NC
2	S1
3	D1
4	G1
5	S2
6	D2
7	G2
8	NC

### 8-Pin MiniDIP (NS Package 67)

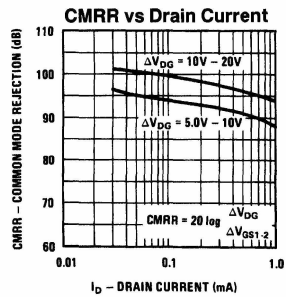
- \*NPD8301
- \*NPD8302
- \*NPD8303
- \*NPD8304

Pin	67
1	S1
2	D1
3	NC
4	G1
5	S2
6	D2
7	NC
8	G2

Note: S0-8 to be announced.



TL/G/10035-18



TL/G/10035-19

