

BTW42 SERIES

THYRISTORS

Glass-passivated silicon thyristors in metal envelopes with high dV_D/dt capabilities. They are intended for use in power control circuits and switching systems where high transients can occur (e.g. phase control in three-phase systems).

The series consists of reverse polarity types (anode to stud) identified by a suffix R: BTW42-600R to 1000R.

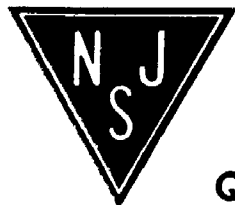
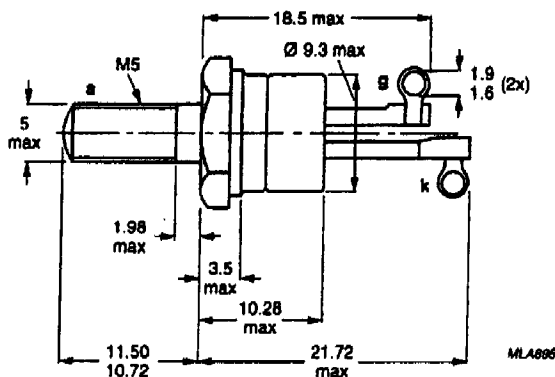
QUICK REFERENCE DATA

| | | BTW42-600R 800R 1000R | | | | |
|---|-------------------|---------------------------|-----|------|------|------------|
| Repetitive peak voltages | V_{DRM}/V_{RRM} | max. | 600 | 800 | 1000 | V |
| Average on-state current | $I_T(AV)$ | max. | | 10 | | A |
| R.M.S. on-state current | $I_T(RMS)$ | max. | | 16 | | A |
| Non-repetitive peak on-state current | I_{TSM} | max. | | 150 | | A |
| Rate of rise of off-state voltage that will not trigger any device | dV_D/dt | < | | 500 | | V/ μs |
| On request (see Ordering Note) | dV_D/dt | < | | 1000 | | V/ μs |

MECHANICAL DATA

Dimensions in mm

Fig.1 TO-64



RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Anode to cathode

| | | BTW42-600R | 800R | 1000R |
|---|-------------------|------------|------|----------------------|
| Non-repetitive peak voltages ($t \leq 10$ ms) | V_{DSM}/V_{RSM} | max. 600 | 800 | 1000 V |
| Repetitive peak voltages | V_{DRM}/V_{RRM} | max. 600 | 800 | 1000 V |
| Crest working voltages | V_{DWM}/V_{RWM} | max. 400 | 600 | 700 V* |
| Average on-state current (averaged over any 20 ms period) up to $T_{mb} = 85$ °C | $I_T(AV)$ | | max. | 10 A |
| R.M.S. on-state current | $I_T(RMS)$ | | max. | 16 A |
| Repetitive peak on-state current | I_{TRM} | | max. | 75 A |
| Non-repetitive peak on-state current; $t = 10$ ms; half sine-wave; $T_j = 125$ °C prior to surge; with reapplied V_{RWMmax} | I_{TSM} | | max. | 150 A |
| I^2t for fusing ($t = 10$ ms) | I^2t | | max. | 112 A ² s |
| Rate of rise of on-state current after triggering with $I_G = 250$ mA to $I_T = 25$ A; $dI_G/dt = 0,25$ A/ μ s | dI_T/dt | | max. | 50 A/ μ s |

Gate to cathode

| | | | |
|---|-----------|------|-------|
| Average power dissipation (averaged over any 20 ms period) | $P_G(AV)$ | max. | 0,5 W |
| Peak power dissipation | P_{GM} | max. | 5 W |

Temperatures

| | | |
|----------------------|-----------|-----------------|
| Storage temperature | T_{stg} | -55 to + 125 °C |
| Junction temperature | T_j | max. 125 °C |

THERMAL RESISTANCE

| | | | |
|--|---------------|---|---------|
| From junction to mounting base | $R_{th j-mb}$ | = | 1,8 K/W |
| From mounting base to heatsink with heatsink compound | $R_{th mb-h}$ | = | 0,5 K/W |
| From junction to ambient in free air | $R_{th j-a}$ | = | 45 K/W |
| Transient thermal impedance ($t = 1$ ms) | $Z_{th j-mb}$ | = | 0,1 K/W |

OPERATING NOTE

The terminals should neither be bent nor twisted; they should be soldered into the circuit so that there is no strain on them.

During soldering the heat conduction to the junction should be kept to a minimum.

CHARACTERISTICS

Anode to cathode

On-state voltage (measured under pulse conditions)

$$I_T = 20 \text{ A}; T_j = 25 \text{ }^\circ\text{C}$$

$$V_T < 2 \text{ V}$$

Rate of rise of off-state voltage that will not trigger any device; exponential method;

$$V_D = 2/3 V_{DRMmax}; T_j = 125 \text{ }^\circ\text{C}$$

$$dV_D/dt < 500 \text{ V}/\mu\text{s}$$

Reverse current

$$V_R = V_{RWMmax}; T_j = 125 \text{ }^\circ\text{C}$$

$$I_R < 3 \text{ mA}$$

Off-state current

$$V_D = V_{DWMmax}; T_j = 125 \text{ }^\circ\text{C}$$

$$I_D < 3 \text{ mA}$$

Latching current; $T_j = 25 \text{ }^\circ\text{C}$

$$I_L < 150 \text{ mA}$$

Holding current; $T_j = 25 \text{ }^\circ\text{C}$

$$I_H < 75 \text{ mA}$$

Gate to cathode

Voltage that will trigger all devices

$$V_D = 6 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$$

$$V_{GT} > 1.5 \text{ V}$$

Voltage that will not trigger any device

$$V_D = V_{DRMmax}; T_j = 125 \text{ }^\circ\text{C}$$

$$V_{GD} < 200 \text{ mV}$$

Current that will trigger all devices

$$V_D = 6 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$$

$$I_{GT} > 50 \text{ mA}$$

Switching characteristics

Gate-controlled turn-on time ($t_{gt} = t_d + t_r$) when

switched from $V_D = V_{DRMmax}$ to $I_T = 40 \text{ A}$;

$$I_{GT} = 100 \text{ mA}; dI_G/dt = 5 \text{ A}/\mu\text{s}; T_j = 25 \text{ }^\circ\text{C}$$

$$t_{gt} \text{ typ. } 2 \text{ } \mu\text{s}$$

Circuit-commutated turn-off time when switched

from $I_T = 40 \text{ A}$ to $V_R > 50 \text{ V}$ with

$$-dI_T/dt = 10 \text{ A}/\mu\text{s}; dV_D/dt = 50 \text{ V}/\mu\text{s}; T_j = 115 \text{ }^\circ\text{C}$$

$$t_q \text{ typ. } 35 \text{ } \mu\text{s}$$