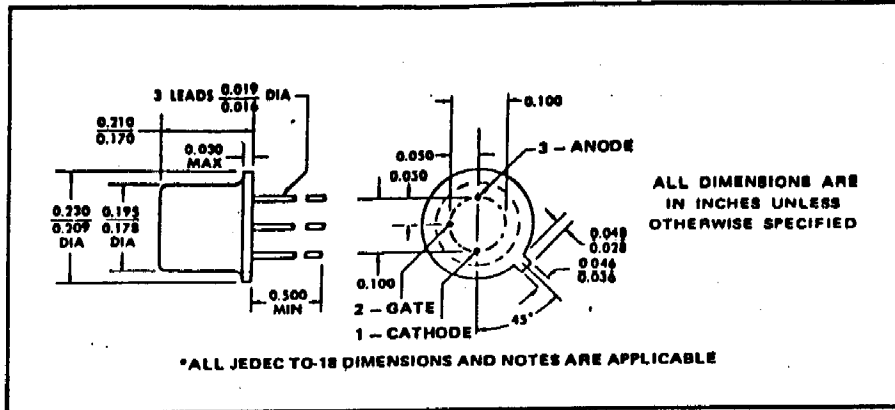


**2N3008**

**SILICON REVERSE-BLOCKING TRIODE THYRISTOR**



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

|  | 2N3008     | UNIT |
|--|------------|------|
| *Static Off-State Voltage, $V_D$ (See Note 1)  | 200        | V    |
| *Repetitive Peak Off-State Voltage, $V_{DRM}$ (See Note 1)   | 200        | V    |
| *Static Reverse Voltage, $V_R$ (See Note 2)  | 200        | V    |
| *Repetitive Peak Reverse Voltage, $V_{RRM}$ (See Note 2)   | 200        | V    |
| *Continuous or RMS On-State Current at (or below) 55°C Free-Air Temperature <sup>1</sup>               | 350        | mA   |
| *Average On-State Current (180° Conduction Angle) at (or below) 55°C Free-Air Temperature <sup>1</sup> | 250        | mA   |
| *Surge On-State Current (See Note 3)   | 6          | A    |
| Peak Negative Gate Voltage   | 8          | V    |
| *Peak Positive Gate Current (Pulse Width < 8 ms)   | 250        | mA   |
| *Average Gate Power Dissipation  | 100        | mW   |
| *Operating Free-Air Temperature Range  | -65 to 200 | °C   |
| *Storage Temperature Range   | -65 to 175 | °C   |
| *Lead Temperature 1/16 Inch from Case for 10 Seconds   | 300        | °C   |

NOTES: 1. These values apply when the gate-cathode resistance  $R_{GK} < 1 \text{ k}\Omega$ .  
 2. These values apply when the gate-cathode resistance  $R_{GK} < \infty$ .  
 3. This value applies for one 60-Hz half sine wave when the device is operating at (or below) rated values of peak reverse voltage and on-state current. Surge may be repeated after the device has returned to original thermal equilibrium.  
 \*JEDEC registered data. This data sheet contains all applicable registered data in effect at the time of publication.

\*electrical characteristics at 25°C free-air temperature (unless otherwise noted)

| PARAMETER                       | TEST CONDITIONS  | MIN | TYP | MAX | UNIT          |
|---------------------------------|--|-----|-----|-----|---------------|
| $I_D$ Static Off-State Current  | $V_D = \text{Rated } V_D, R_{GK} = 1 \text{ k}\Omega$  |     |     | 0.1 | $\mu\text{A}$ |
|                                 | $V_D = \text{Rated } V_D, R_{GK} = 1 \text{ k}\Omega, T_A = 150^\circ\text{C}$                 |     |     | 100 |               |
| $I_G$ Gate Current <sup>1</sup> | $V_G = -5 \text{ V}, I_A = 0$  |     |     | -5  | $\mu\text{A}$ |
| $I_{GT}$ Gate Trigger Current   | $V_{AA} = 5 \text{ V}, R_L = 12 \Omega, t_{p(g)} \geq 10 \mu\text{s}$                          |     |     | 90  | $\mu\text{A}$ |
|                                 | $V_{AA} = 5 \text{ V}, R_L = 12 \Omega, t_{p(g)} \geq 10 \mu\text{s}, T_A = -65^\circ\text{C}$ |     |     | 200 |               |
| $V_{GT}$ Gate Trigger Voltage   | $V_{AA} = 5 \text{ V}, R_L = 12 \Omega, t_{p(g)} \geq 10 \mu\text{s}, T_A = -65^\circ\text{C}$ |     |     | 0.9 | V             |
|                                 | $V_{AA} = 5 \text{ V}, R_L = 12 \Omega, t_{p(g)} \geq 10 \mu\text{s}$                          |     |     | 0.6 |               |
|                                 | $V_{AA} = 5 \text{ V}, R_L = 12 \Omega, t_{p(g)} \geq 10 \mu\text{s}, T_A = 150^\circ\text{C}$ | 0.2 |     | 0.8 |               |
| $I_H$ Holding Current           | $R_{GK} = 1 \text{ k}\Omega, R_L = 2 \text{ k}\Omega$  |     |     | 1.8 | mA            |
|                                 | $R_{GK} = 1 \text{ k}\Omega, R_L = 2 \text{ k}\Omega, T_A = -65^\circ\text{C}$                 |     |     | 5   |               |
| $V_T$ On-State Voltage          | $I_T = 350 \text{ mA}, R_{GK} > 1 \text{ k}\Omega, \text{ See Note 6}$                         |     |     | 1.2 | V             |

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