



P-Channel Enhancement-Mode Vertical DMOS FETs

Ordering Information

BV _{DSS} /	R _{DS(ON)}	V _{GS(th)}	I _{D(ON)}	Order Number / Package		
BV_{DGS}	(max)	(max)	(min)	TO-243AA*	Die**	
-350V	15Ω	-2.4V	-800mA	TP2435N8	TP2435NW	

^{*} Same as SOT-89. Product supplied on 2000 piece carrier tape reels.

Product marking for TO-243AA: TP4S* where * = 2-week alpha date code

Features

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☐ High input impedance

Low input capacitance

☐ Fast switching speeds

☐ Free from secondary breakdown

Low input and output leakage

☐ Complementary N- and P-channel devices

Applications

Logic	level	interfaces
Logic	1000	IIIICIIACCO

Solid state relays

Linear Amplifiers

☐ Power Management

Analog switches

Telecom switches

Absolute Maximum Ratings

Drain-to-Source Voltage	BV_{DSS}
Drain-to-Gate Voltage	BV_{DGS}
Gate-to-Source Voltage	± 20V
Operating and Storage Temperature	-55°C to +150°C
Soldering Temperature*	300°C

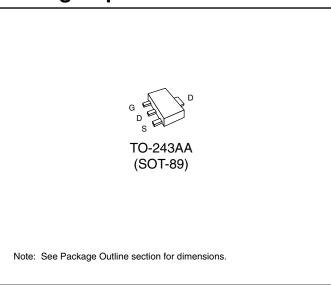
^{*} Distance of 1.6 mm from case for 10 seconds.

Low Threshold DMOS Technology

These low threshold enhancement-mode (normally-off) power transistors utilize a vertical DMOS structure and Supertex's well-proven silicon-gate manufacturing process. This combination produces devices with the power handling capabilities of bipolar transistors and with the high input impedance and positive temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, these devices are free from thermal runaway and thermally induced secondary breakdown.

Supertex's vertical DMOS FETs are ideally suited to a wide range of switching and amplifying applications where very low threshold voltage, high breakdown voltage, high input impedance, low input capacitance, and fast switching speeds are desired.

Package Option



^{**} Die in wafer form.

Thermal Characteristics

Package	I _D (continuous)*	I _D (pulsed)	Power Dissipation	$ heta_{\sf jc}$	θ_{ja}	I _{DR} *	I _{DRM}
			@ T _A = 25°C	°C/W	°C/W		
TO-243AA	-231mA	-1.1A	1.6W [†]	15	78 [†]	-231mA	-1.1A

^{*} $I_{\scriptscriptstyle D}$ (continuous) is limited by max rated $T_{\scriptscriptstyle i}$.

Electrical Characteristics (@ 25°C unless otherwise specified)

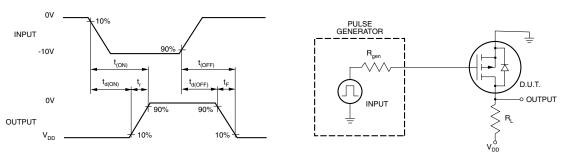
Symbol	Parameter	Min	Тур	Max	Unit	Conditions	
BV _{DSS}	Drain-to-Source Breakdown Voltage	-350			V	$V_{GS} = 0V, I_D = -250\mu A$	
V _{GS(th)}	Gate Threshold Voltage	-1.0		-2.4	V	$V_{GS} = V_{DS}$, $I_D = -1.0$ mA	
$\Delta V_{GS(th)}$	Change in V _{GS(th)} with Temperature			4.5	mV/°C	$V_{GS} = V_{DS}$, $I_D = -1.0$ mA	
I _{GSS}	Gate Body Leakage			-100	nA	$V_{GS} = \pm 20V, V_{DS} = 0V$	
I _{DSS}	Zero Gate Voltage Drain Current			-10.0	μΑ	V _{GS} = 0V, V _{DS} = Max Rating	
				-1.0	mA	$V_{GS} = 0V$, $V_{DS} = 0.8$ Max Rating $T_A = 125$ °C	
I _{D(ON)}	ON-State Drain Current	-0.3				$V_{GS} = -4.5V, V_{DS} = -25V$	
		-0.8			Α	$V_{GS} = -10V, V_{DS} = -25V$	
R _{DS(ON)}	Static Drain-to-Source			15		$V_{GS} = -3.0V, I_{D} = -20mA$	
	ON-State Resistance			15	Ω	$V_{GS} = -4.5V, I_D = -150mA$	
				15		V _{GS} = -10V, I _D = -500mA	
$\Delta R_{DS(ON)}$	Change in R _{DS(ON)} with Temperature			1.7	%/°C	$V_{GS} = -10V, I_D = -150mA$	
G _{FS}	Forward Transconductance	125			mʊ	$V_{DS} = -25V, I_{D} = -350mA$	
C _{ISS}	Input Capacitance			200		V 0V V 05V	
C _{OSS}	Common Source Output Capacitance			70	pF	$V_{GS} = 0V, V_{DS} = -25V$ f = 1.0 MHz	
C _{RSS}	Reverse Transfer Capacitance			25		1 - 1.0 WH 12	
t _{d(ON)}	Turn-ON Delay Time			15			
t _r	Rise Time			20		$V_{DD} = -25V$,	
t _{d(OFF)}	Turn-OFF Delay Time			25	ns	$I_D = -250 \text{mA},$	
t _f				50		$R_{GEN} = 25\Omega$	
V _{SD}	Diode Forward Voltage Drop			-1.5	V	$V_{GS} = 0V, I_{SD} = -750mA$	
t _{rr}	Reverse Recovery Time		300		ns	$V_{GS} = 0V, I_{SD} = -750mA$	

Notes:

 $1. All\ D.C.\ parameters\ 100\%\ tested\ at\ 25^{\circ}C\ unless\ otherwise\ stated.\ (Pulse\ test:\ 300\mu s\ pulse,\ 2\%\ duty\ cycle.)$

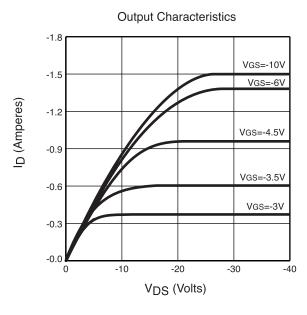
2.All A.C. parameters sample tested.

Switching Waveforms and Test Circuit

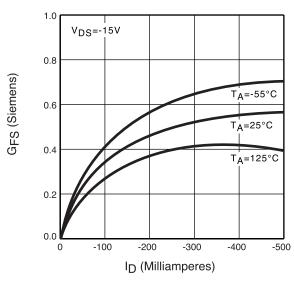


 $^{^{\}dagger}$ Mounted on FR5 board, 25mm x 25mm x 1.57mm. Significant $P_{\rm p}$ increase possible on ceramic substrate.

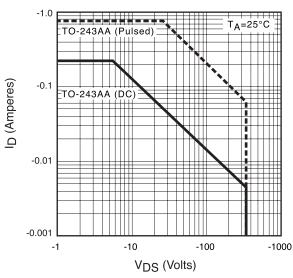
Typical Performance Curves



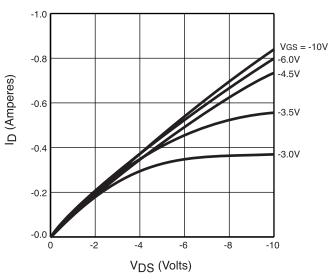
Transconductance vs. Drain Current



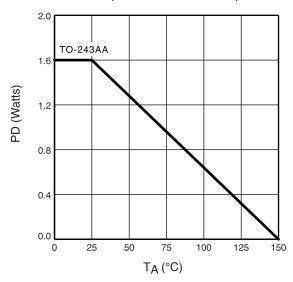
Maximum Rated Safe Operating Area



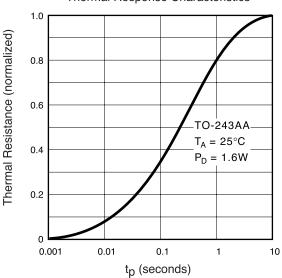
Saturation Characteristics



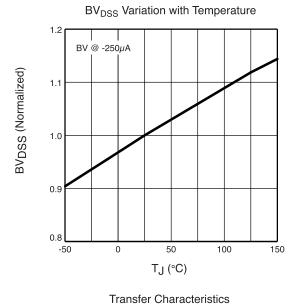
Power Dissipation vs. Ambient Temperature

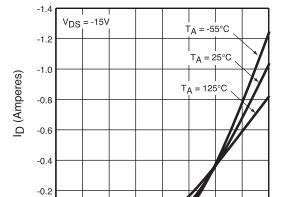


Thermal Response Characteristics



Typical Performance Curves



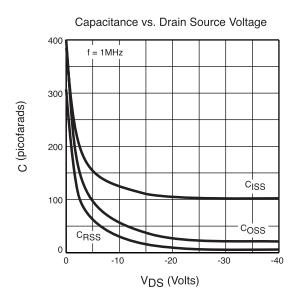


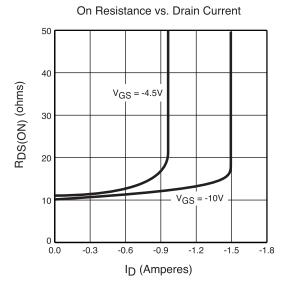
-2.0

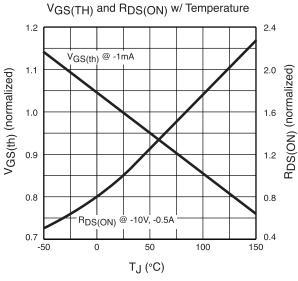
V_{GS} (Volts)

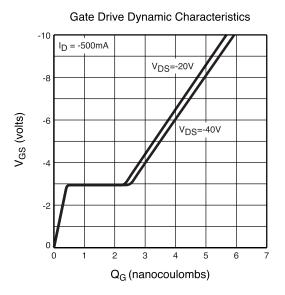
-3.0

-4.0









0.0

-1.0