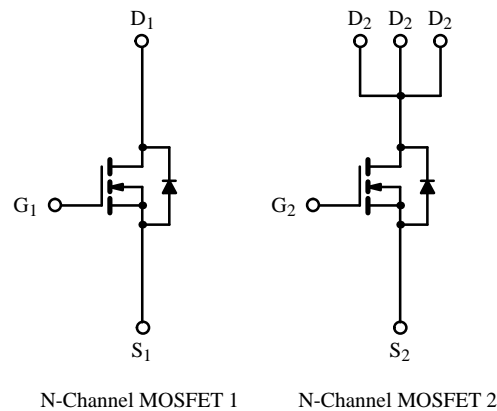
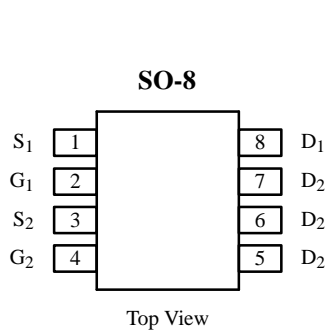


## Asymmetrical Dual N-Channel Enhancement-Mode MOSFET

### Product Summary

	V <sub>DS</sub> (V)	r <sub>DS(on)</sub> (Ω)	I <sub>D</sub> (A)
N-Channel 1	30	0.065 @ V <sub>GS</sub> = 10 V	± 3.0
		0.095 @ V <sub>GS</sub> = 4.5 V	± 2.5
0.028 @ V <sub>GS</sub> = 10 V		± 6.7	
0.042 @ V <sub>GS</sub> = 4.5 V		± 5.4	
N-Channel 2			

**TrenchFET™**  
Power MOSFETs



### Absolute Maximum Ratings (T<sub>A</sub> = 25°C Unless Otherwise Noted)

Parameter	Symbol	N-Channel 1	N-Channel 2	Unit
Drain-Source Voltage	V <sub>DS</sub>	30	30	V
Gate-Source Voltage	V <sub>GS</sub>	± 20	± 20	
Continuous Drain Current (T <sub>J</sub> = 150°C) <sup>NO TAG</sup>	I <sub>D</sub>	T <sub>A</sub> = 25°C	± 3.0	A
		T <sub>A</sub> = 70°C	± 2.4	
Pulsed Drain Current	I <sub>DM</sub>	± 20	± 30	A
Continuous Source Current (Diode Conduction) <sup>NO TAG</sup>	I <sub>S</sub>	1.25	2.0	
Maximum Power Dissipation <sup>NO TAG</sup>	P <sub>D</sub>	T <sub>A</sub> = 25°C	1.0	W
		T <sub>A</sub> = 70°C	0.64	
Operating Junction and Storage Temperature Range	T <sub>J</sub> , T <sub>stg</sub>	-55 to 150	-55 to 150	°C

### Thermal Resistance Ratings

Parameter	Symbol	N-Channel 1	N-Channel 2	Unit
Maximum Junction-to-Ambient <sup>NO TAG</sup>	R <sub>thJA</sub>	125	55	°C/W

#### Notes

a. Surface Mounted on FR4 Board, t ≤ 10 sec.

Subsequent updates to this data sheet may be obtained via facsimile by calling Siliconix FaxBack, 1-408-970-5600. Please request FaxBack document #1241. A SPICE Model data sheet is available for this product (FaxBack document #5156).

## Specifications ( $T_J = 25^\circ\text{C}$ Unless Otherwise Noted)

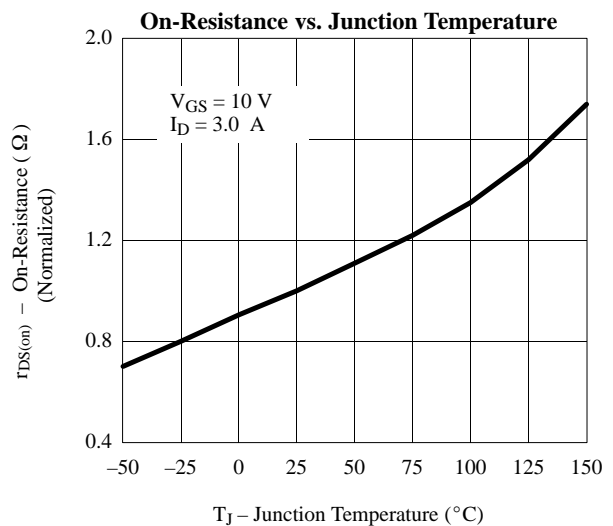
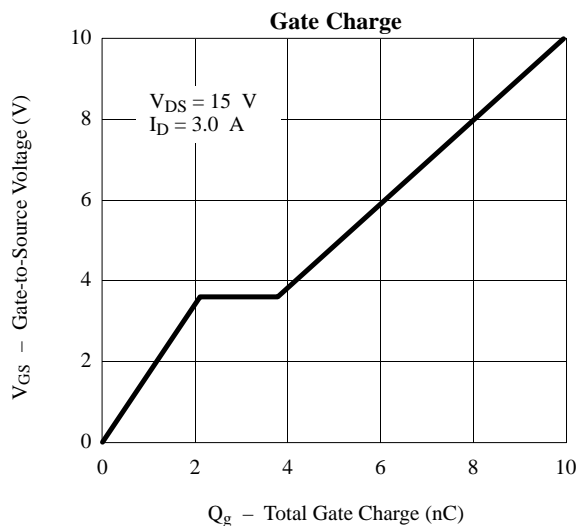
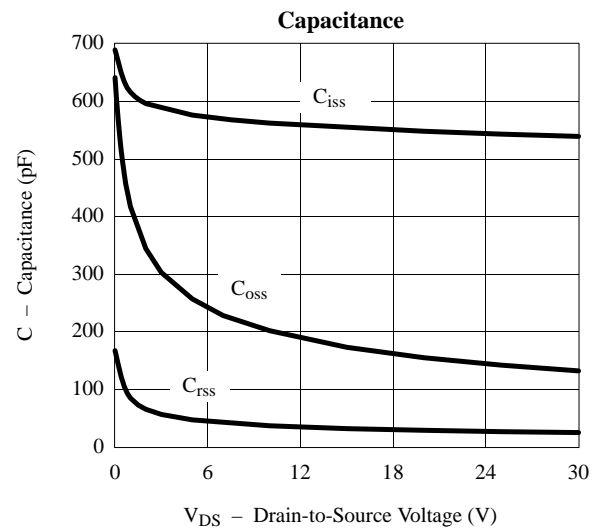
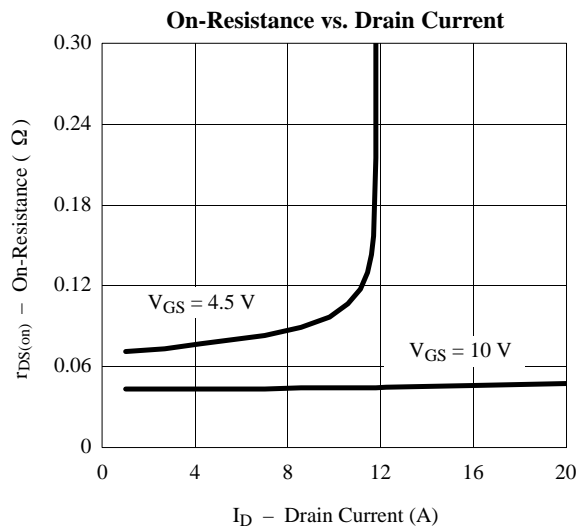
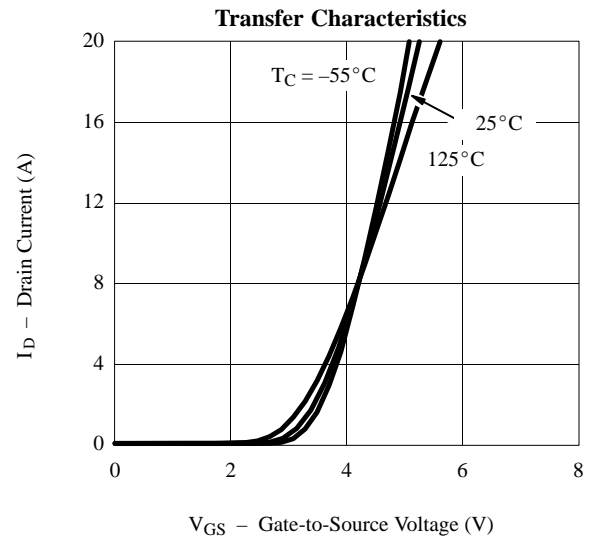
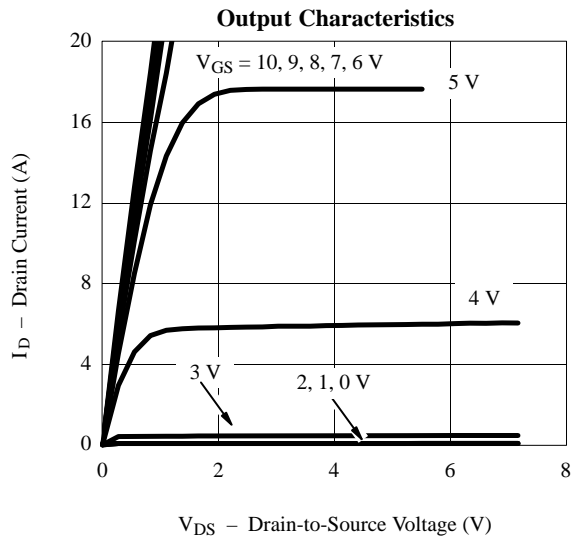
Parameter	Symbol	Test Condition	Min	Typ NO TAG	Max	Unit	
<b>Static</b>							
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250 \mu\text{A}$	N-Ch 1	1.0		V	
			N-Ch 2	1.0			
Gate-Body Leakage	$I_{GSS}$	$V_{DS} = 0 \text{ V}, V_{GS} = \pm 20 \text{ V}$	N-Ch 1		$\pm 100$	nA	
			N-Ch 2		$\pm 100$		
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS} = 30 \text{ V}, V_{GS} = 0 \text{ V}$	N-Ch 1		1	$\mu\text{A}$	
			N-Ch 2		1		
		$V_{DS} = 30 \text{ V}, V_{GS} = 0 \text{ V}, T_J = 55^\circ\text{C}$	N-Ch 1		25		
			N-Ch 2		25		
On-State Drain Current <sup>NO TAG</sup>	$I_{D(on)}$	$V_{DS} \geq 5 \text{ V}, V_{GS} = 10 \text{ V}$	N-Ch 1	20		A	
			N-Ch 2	30			
Drain-Source On-State Resistance <sup>NO TAG</sup>	$r_{DS(on)}$	$V_{GS} = 10 \text{ V}, I_D = 3.0 \text{ A}$	N-Ch 1	0.043	0.065	$\Omega$	
		$V_{GS} = 10 \text{ V}, I_D = 6.7 \text{ A}$	N-Ch 2	0.021	0.028		
		$V_{GS} = 4.5 \text{ V}, I_D = 2.5 \text{ A}$	N-Ch 1	0.073	0.095		
		$V_{GS} = 4.5 \text{ V}, I_D = 5.4 \text{ A}$	N-Ch 2	0.032	0.042		
Forward Transconductance <sup>NO TAG</sup>	$g_{fs}$	$V_{DS} = 15 \text{ V}, I_D = 3.0 \text{ A}$	N-Ch 1	6.0		S	
		$V_{DS} = 15 \text{ V}, I_D = 6.7 \text{ A}$	N-Ch 2	15.5			
Diode Forward Voltage <sup>NO TAG</sup>	$V_{SD}$	$I_S = 1.25 \text{ A}, V_{GS} = 0 \text{ V}$	N-Ch 1	0.75	1.2	V	
		$I_S = 2.0 \text{ A}, V_{GS} = 0 \text{ V}$	N-Ch 2	0.8	1.2		
<b>Dynamic<sup>NO TAG</sup></b>							
Total Gate Charge	$Q_g$	N-Channel 1 $V_{DS} = 15 \text{ V}, V_{GS} = 10 \text{ V}, I_D = 3.0 \text{ A}$ N-Channel 2 $V_{DS} = 15 \text{ V}, V_{GS} = 10 \text{ V}, I_D = 6.7 \text{ A}$	N-Ch 1		10	15	nC
Gate-Source Charge	$Q_{gs}$		N-Ch 2		24	30	
			N-Ch 1		2.1		
Gate-Drain Charge	$Q_{gd}$		N-Ch 2		4.8		
			N-Ch 1		1.7		
N-Ch 2			4.6				
Turn-On Delay Time	$t_{d(on)}$	N-Channel 1 $V_{DD} = 15 \text{ V}, R_L = 15 \Omega$ $I_D \cong 1 \text{ A}, V_{GEN} = 10 \text{ V}, R_G = 6 \Omega$ N-Channel 2 $V_{DD} = 15 \text{ V}, R_L = 15 \Omega$ $I_D \cong 1 \text{ A}, V_{GEN} = 10 \text{ V}, R_G = 6 \Omega$	N-Ch 1		10	15	ns
Rise Time	$t_r$		N-Ch 2		14	20	
			N-Ch 1		8	15	
Turn-Off Delay Time	$t_{d(off)}$		N-Ch 2		10	20	
			N-Ch 1		19	30	
Fall Time	$t_f$		N-Ch 2		36	55	
			N-Ch 1		8	15	
Source-Drain Reverse Recovery Time	$t_{rr}$		$I_F = 1.25 \text{ A}, di/dt = 100 \text{ A}/\mu\text{s}$	N-Ch 1		45	
		$I_F = 2.0 \text{ A}, di/dt = 100 \text{ A}/\mu\text{s}$	N-Ch 2		48	80	

Notes

- For design aid only; not subject to production testing.
- Pulse test; pulse width  $\leq 300 \mu\text{s}$ , duty cycle  $\leq 2\%$ .

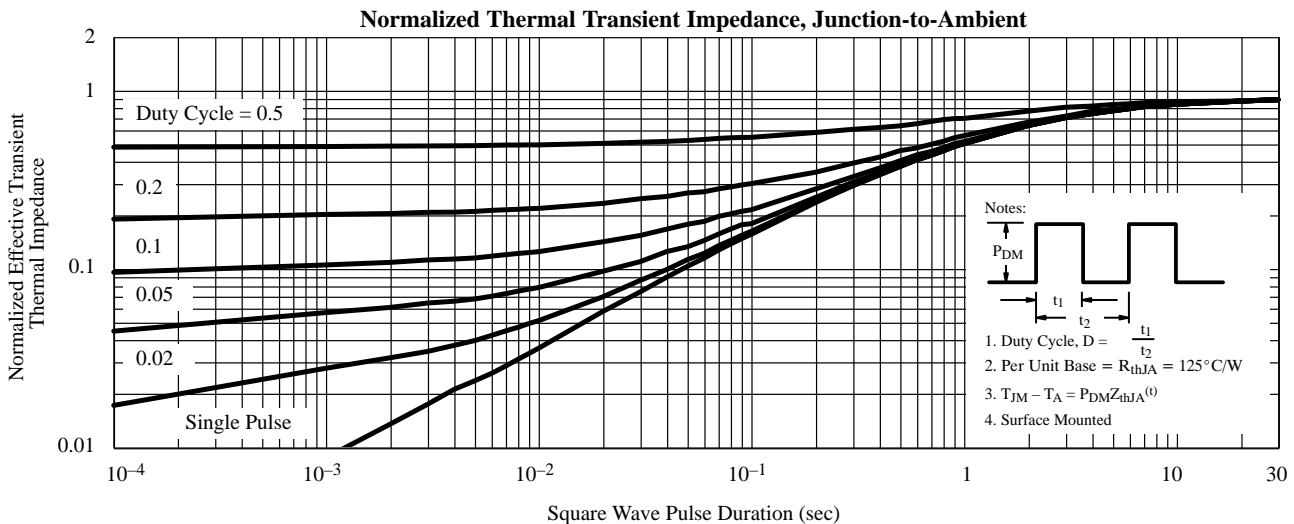
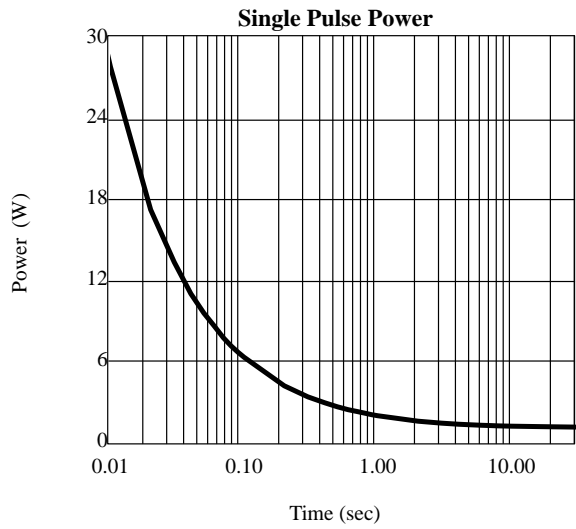
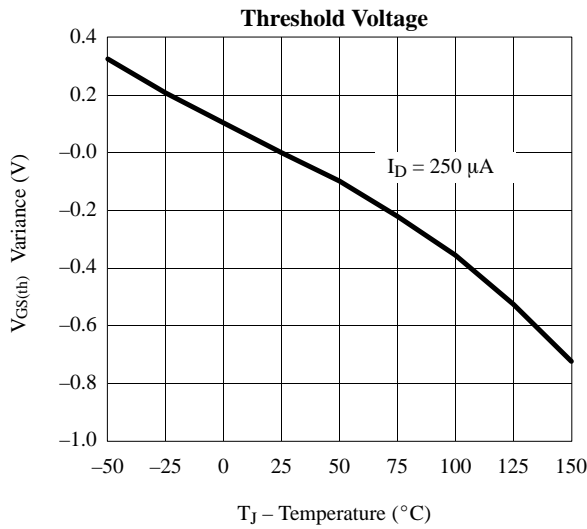
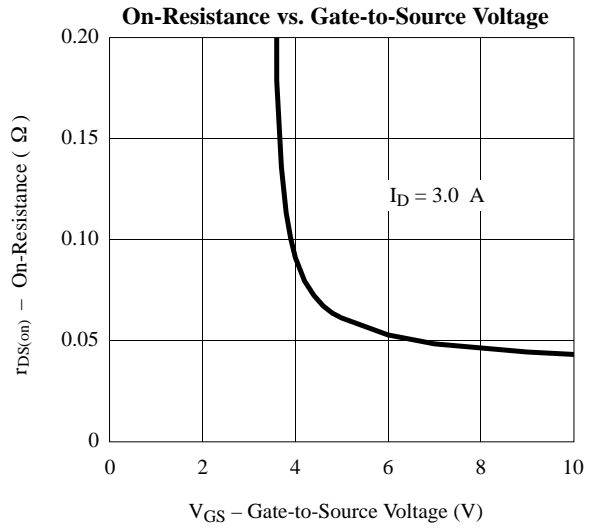
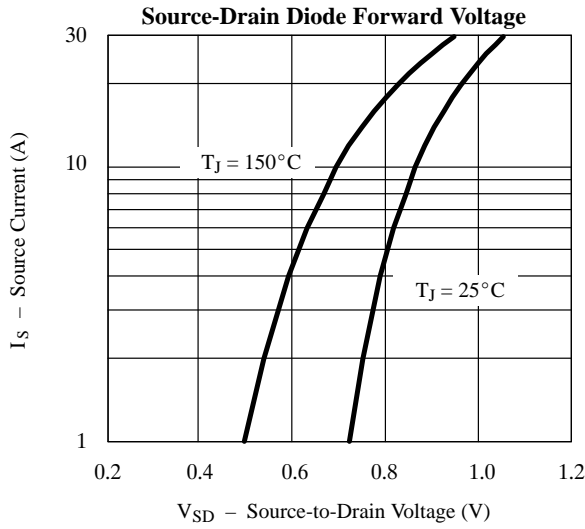
## Typical Characteristics (25°C Unless Noted)

## N-Channel 1



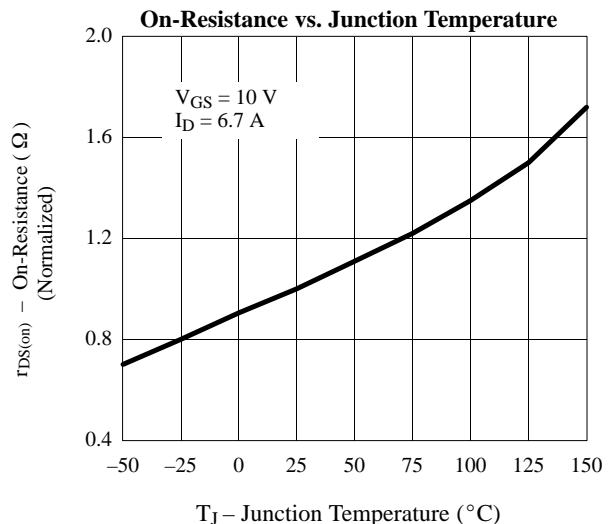
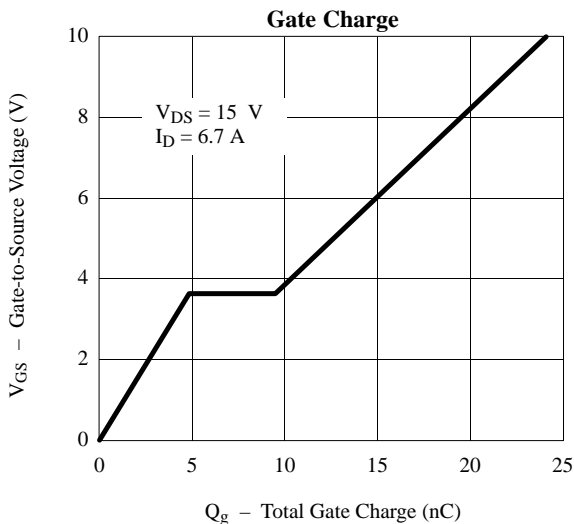
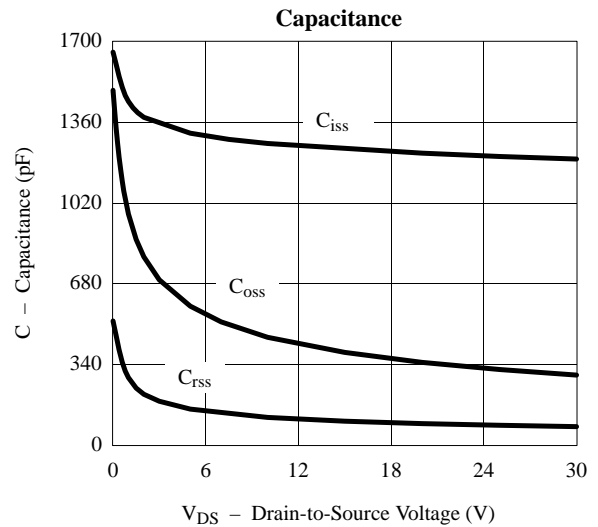
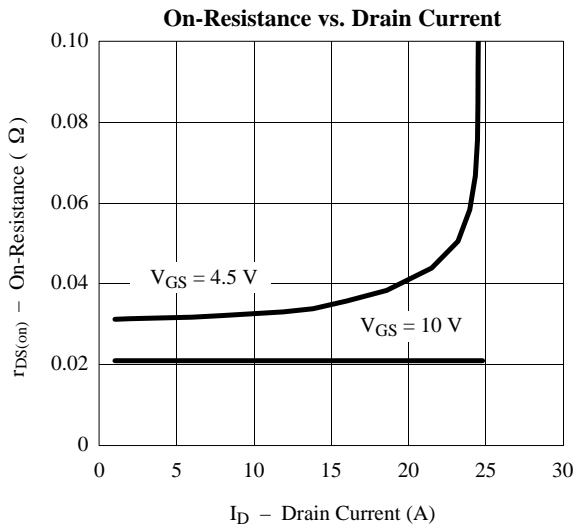
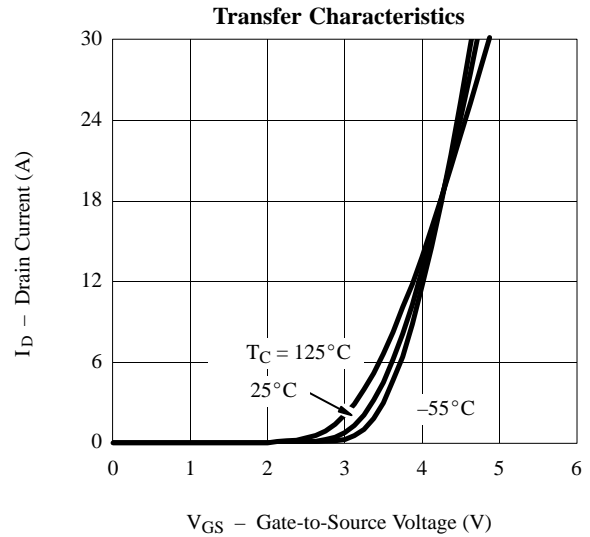
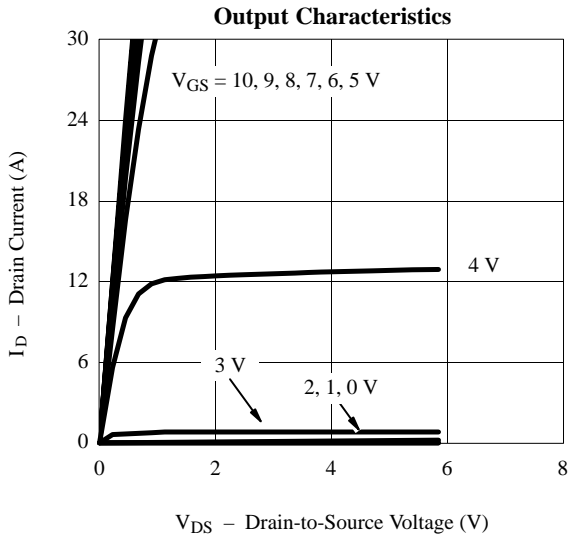
## Typical Characteristics (25°C Unless Noted)

## N-Channel 1



**Typical Characteristics (25°C Unless Noted)**

**N-Channel 2**



## Typical Characteristics (25°C Unless Noted)

## N-Channel 2

