SGS-THOMSON MICROELECTRONICS

SGSP471
SGSP472

N - CHANNEL ENHANCEMENT MODE POWER MOS TRANSISTORS

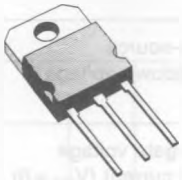
TYPE	V_{DSS}	$R_{DS(on)}$	I_D
SGSP471	100 V	0.075 Ω	30 A
SGSP472	80 V	0.05 Ω	35 A

- HIGH SPEED SWITCHING APPLICATIONS
- 80 - 100 VOLTS - FOR DC/DC CONVERTERS
- HIGH CURRENT > 1V DROP AT 20A
- RATED FOR UNCLAMPED INDUCTIVE SWITCHING (ENERGY TEST) ◆
- ULTRA FAST SWITCHING
- EASY DRIVE FOR REDUCED SIZE AND COST

INDUSTRIAL APPLICATIONS:

- UNINTERRUPTIBLE POWER SUPPLIES
- MOTOR CONTROLS

N - channel enhancement mode POWER MOS field effect transistors. Easy drive and very fast switching times make these POWER MOS transistors ideal for high speed switching applications. Applications include DC/DC converters, UPS, battery chargers, secondary regolators, servo control, power audio amplifiers and robotics.



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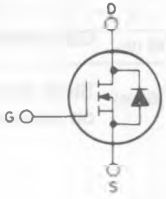
INTERNAL SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS		SGSP471	SGSP472	
V_{DS}	Drain-source voltage ($V_{GS}=0$)	100	80	V
V_{DGR}	Drain-gate voltage ($R_{GS}=20$ KΩ)	100	80	V
V_{GS}	Gate-source voltage	±20		V
I_D	Drain current (cont.) at $T_c=25°C$	30	35	A
I_D	Drain current (cont.) at $T_c=100°C$	19	22	A
I_{DM} (•)	Drain current (pulsed)	120	140	A
P_{tot}	Total dissipation at $T_c<25°C$	150		W
	Derating factor	1.2		W/°C
T_{stg}	Storage temperature	−65 to 150		°C
T_j	Max. operating junction temperature	150		°C

(•) Pulse width limited by safe operating area
◆ Introduced in 1988 week 44

THERMAL DATA

$R_{thj\text{-}case}$	Thermal resistance junction-case	max	0.83	°C/W
T_L	Maximum lead temperature for soldering purpose		275	°C

ELECTRICAL CHARACTERISTICS (T_{case} = 25°C unless otherwise specified)

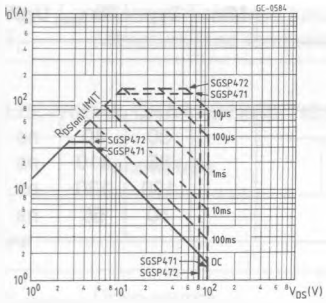
Parameters		Test Conditions	Min.	Typ.	Max.	Unit
OFF						
$V_{(BR)\ DSS}$	Drain-source breakdown voltage	I_D = 250 μA V_{GS} = 0 for **SGSP471** for **SGSP472**	 100 80			 V V
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0)	V_{DS} = Max Rating V_{DS} = Max Rating x 0.8 T_c = 125°C			250 1000	μA μA
I_{GSS}	Gate-body leakage current (V_{DS} = 0)	V_{GS} = ±20 V			±100	nA
ON (*)						
$V_{GS\ (th)}$	Gate threshold voltage	V_{DS} = V_{GS} I_D = 250 μA	2		4	V
$R_{DS\ (on)}$	Static drain-source on resistance	V_{GS} = 10 V I_D = 15 A for **SGSP471** I_D = 17.5 A for **SGSP472** V_{GS} = 10 V T_c = 100°C I_D = 15 A for **SGSP471** I_D = 17.5 A for **SGSP472**			 0.075 0.05 0.15 0.1	 Ω Ω Ω Ω
ENERGY TEST						
I_{UIS}	Unclamped inductive switching current (single pulse)	V_{DD} = 30 V L = 100 μH starting T_j = 25°C for **SGSP471** for **SGSP472**	 30 35			 A A
DYNAMIC						
g_{fs}	Forward transconductance	V_{DS} = 25 V I_D = 17.5 A	9			mho
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	V_{DS} = 25 V f = 1 MHz V_{GS} = 0		1800	2200 810 375	pF pF pF

ELECTRICAL CHARACTERISTICS (Continued)

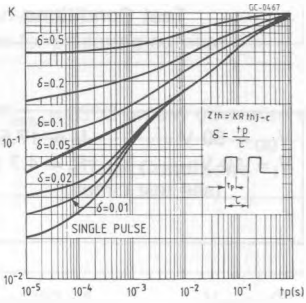
Parameters		Test Conditions	Min.	Typ.	Max.	Unit
SWITCHING						
$t_{d\ (on)}$	Turn-on time	V_{DD} = 50 V I_D = 17.5 A		30	40	ns
t_r	Rise time	V_i = 10 V R_i = 4.7 Ω		85	110	ns
$t_{d\ (off)}$	Turn-off delay time	(see test circuit)		100	130	ns
t_f	Fall time			40	55	ns
SOURCE DRAIN DIODE						
I_{SO}	Source-drain current	for **SGSP471**			30	A
		for **SGSP472**			35	A
I_{SDM} (*)	Source-drain current (pulsed)	for **SGSP471**			120	A
		for **SGSP472**			140	A
V_{SD}	Forward on voltage	V_{GS} = 0				
		I_{SD} = 30 A for **SGSP471**			1.35	V
		I_{SD} = 35 A for **SGSP472**			1.35	V
t_{rr}	Reverse recovery time	I_{SD} = 35 A V_{GS} = 0 di/dt = 25 A/μs		190		ns

(*) Pulsed: Pulse duration = 300 μs, duty cycle 1.5%
(*) Pulse width limited by safe operating area

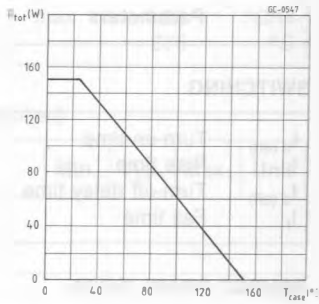
Safe operating areas



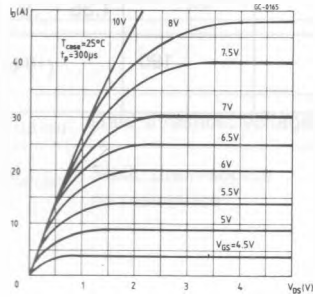
Thermal impedance



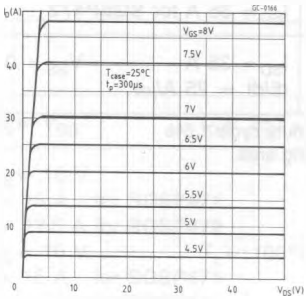
Derating curve



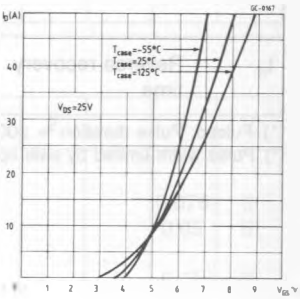
Output characteristics



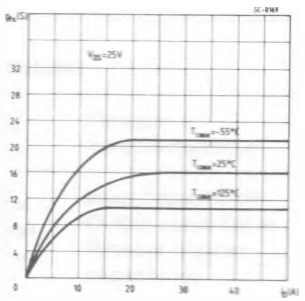
Output characteristics



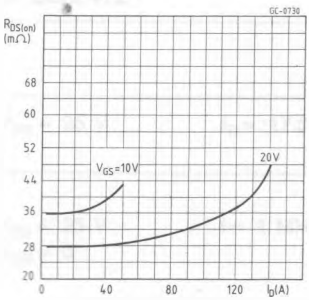
Transfer characteristics



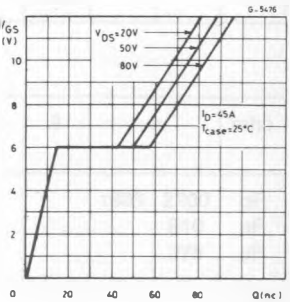
Transconductance



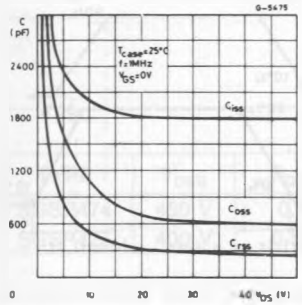
Static drain-source on resistance



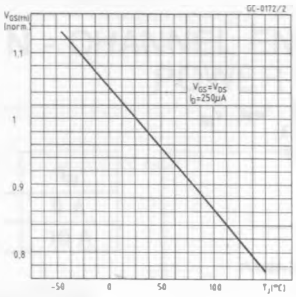
Gate charge vs gate-source voltage



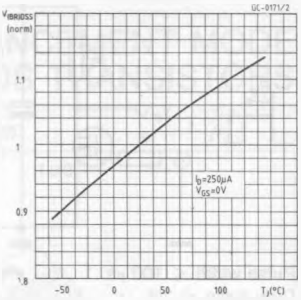
Capacitance variation



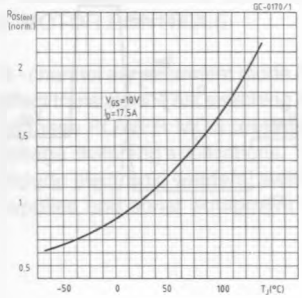
Normalized gate threshold voltage vs temperature



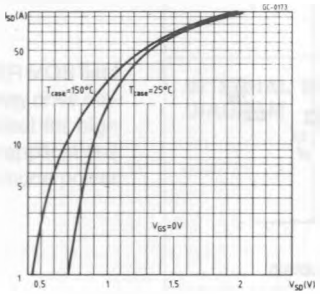
Normalized breakdown voltage vs temperature



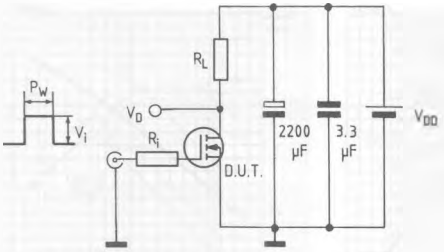
Normalized on resistance vs temperature



Source-drain diode forward characteristics

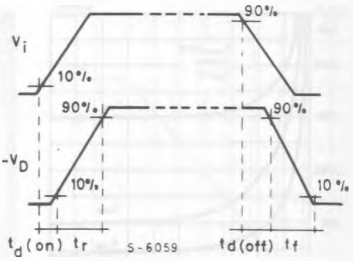


Switching times test circuit for resistive load

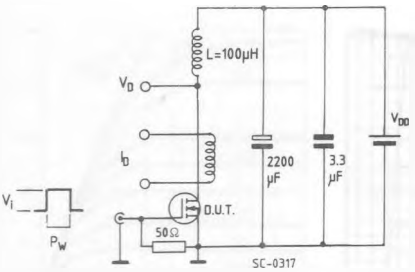


Pulse width ⩽ 100 µs
Duty cycle ⩽ 2%

Switching time waveforms for resistive load

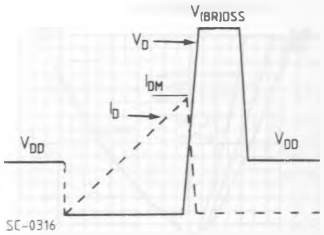


Unclamped inductive load test circuit

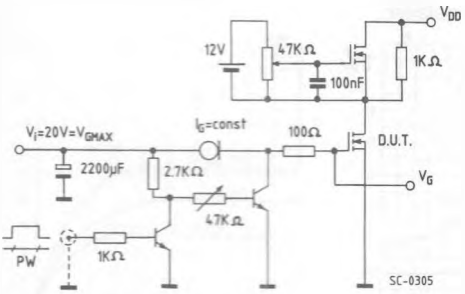


V_i = 12 V - Pulse width: adjusted to obtain specified I_{DM}

Unclamped inductive waveforms



Gate charge test circuit



PW adjusted to obtain required V_G

Body-drain diode t_{rr} measurement
Jedec test circuit