

**N - CHANNEL ENHANCEMENT MODE
POWER MOS TRANSISTORS**

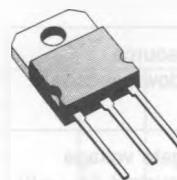
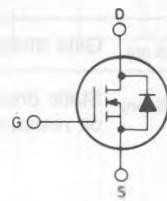
TYPE	V _{DSS}	R _{DS(on)}	I _D
SGSP461	100 V	0.15 Ω	20 A
SGSP462	80 V	0.1 Ω	25 A

- HIGH SPEED SWITCHING APPLICATIONS
- 80 - 100 VOLTS - FOR UPS APPLICATIONS
- RATED FOR UNCLAMPED INDUCTIVE SWITCHING (ENERGY TEST) ♦
- ULTRA FAST SWITCHING
- EASY DRIVE FOR REDUCED COST AND SIZE

INDUSTRIAL APPLICATIONS:

- UNINTERRUPTIBLE POWER SUPPLIES
- MOTOR CONTROLS

N - channel enhancement mode POWER MOS field effect transistors. Easy drive and very fast switching times make these POWER MOS transistors ideal for high speed switching applications. Typical applications include UPS, battery chargers, printer hammer drivers, solenoid drivers and motor control.


TO-218
**INTERNAL SCHEMATIC
DIAGRAM**

ABSOLUTE MAXIMUM RATINGS

		SGSP461	SGSP462
V _{DS}	Drain-source voltage (V _{GS} = 0)	100	80
V _{DGR}	Drain-gate voltage (R _{GS} = 20 kΩ)	100	80
V _{GS}	Gate-source voltage	±20	V
I _D	Drain current (cont.) at T _c = 25°C	20	25
I _D	Drain current (cont.) at T _c = 100°C	13	16
I _{DM} (*)	Drain current (pulsed)	80	100
P _{tot}	Total dissipation at T _c < 25°C	125	W
	Derating factor	1	W/°C
T _{stg}	Storage temperature	– 65 to 150	°C
T _j	Max. operating junction temperature	150	°C

(*) Pulse width limited by safe operating area

♦ Introduced in 1988 week 44

THERMAL DATA

$R_{\text{thj} \cdot \text{case}}$	Thermal resistance junction-case	max	1	$^{\circ}\text{C/W}$
T_L	Maximum lead temperature for soldering purpose	275		$^{\circ}\text{C}$

ELECTRICAL CHARACTERISTICS ($T_{\text{case}} = 25^{\circ}\text{C}$ unless otherwise specified)

Parameters	Test Conditions	Min.	Typ.	Max.	Unit
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OFF

$V_{(\text{BR})\text{DSS}}$	Drain-source breakdown voltage	$I_D = 250 \mu\text{A}$ for SGSP461 for SGSP462	$V_{GS} = 0$	100			V
I_{DSS}	Zero gate voltage drain current ($V_{GS} = 0$)	$V_{DS} = \text{Max Rating}$ $V_{DS} = \text{Max Rating} \times 0.8$	$T_c = 125^{\circ}\text{C}$		250	μA	
I_{GSS}	Gate-body leakage current ($V_{DS} = 0$)	$V_{GS} = \pm 20 \text{ V}$			1000	μA	nA

ON (*)

$V_{GS\text{ (th)}}$	Gate threshold voltage	$V_{DS} = V_{GS}$	$I_D = 250 \mu\text{A}$	2		4	V
$R_{DS\text{ (on)}}$	Static drain-source on resistance	$V_{GS} = 10 \text{ V}$ $I_D = 10 \text{ A}$ for SGSP461 $I_D = 12.5 \text{ A}$ for SGSP462 $V_{GS} = 10 \text{ V}$ $T_c = 100^{\circ}\text{C}$ $I_D = 10 \text{ A}$ for SGSP461 $I_D = 12.5 \text{ A}$ for SGSP462			0.15	Ω	
					0.1	Ω	
					0.3	Ω	
					0.2	Ω	

ENERGY TEST

I_{UIS}	Unclamped inductive switching current (single pulse)	$V_{DD} = 30 \text{ V}$ starting $T_j = 25^{\circ}\text{C}$ for SGSP461 for SGSP462	$L = 100 \mu\text{H}$	20			A
				25			A

DYNAMIC

g_{ts}	Forward transconductance	$V_{DS} = 25 \text{ V}$	$I_D = 12.5 \text{ A}$	4.5			mho
C_{iss}	Input capacitance	$V_{DS} = 25 \text{ V}$	$f = 1 \text{ MHz}$		950	1200	pF
C_{oss}	Output capacitance				480	480	pF
C_{rss}	Reverse transfer capacitance	$V_{GS} = 0$			230	230	pF

ELECTRICAL CHARACTERISTICS (Continued)

Parameters	Test Conditions	Min.	Typ.	Max.	Unit
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SWITCHING

$t_{d(on)}$	Turn-on time	$V_{DD} = 50 \text{ V}$	$I_D = 12.5 \text{ A}$	20	30	ns
t_r	Rise time	$V_i = 10 \text{ V}$	$R_i = 4.7 \Omega$	60	80	ns
$t_d(off)$	Turn-off delay time	(see test circuit)		65	85	ns
t_f	Fall time			25	35	ns

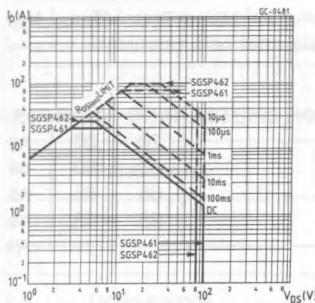
SOURCE DRAIN DIODE

I_{SD}	Source-drain current	for SGSP461		20	A
		for SGSP462		25	A
$I_{SDM} (^*)$	Source-drain current (pulsed)	for SGSP461		80	A
		for SGSP462		100	A
V_{SD}	Forward on voltage	$V_{GS} = 0$ $I_{SD} = 20 \text{ A}$ for SGSP461 $I_{SD} = 25 \text{ A}$ for SGSP462		1.35	V
				1.35	V
t_{rr}	Reverse recovery time	$I_{SD} = 25 \text{ A}$ $di/dt = 25 \text{ A}/\mu\text{s}$	$V_{GS} = 0$	190	

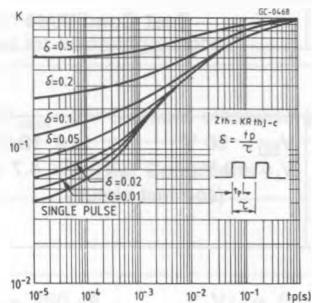
(*) Pulsed: Pulse duration = 300 μs , duty cycle 1.5%

(^*) Pulse width limited by safe operating area

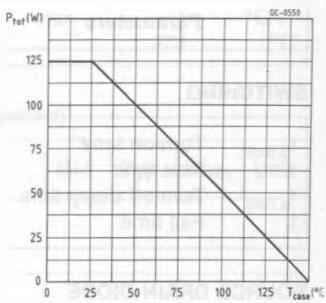
Safe operating areas



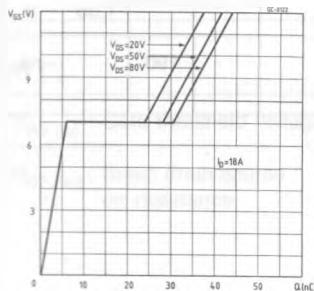
Thermal impedance



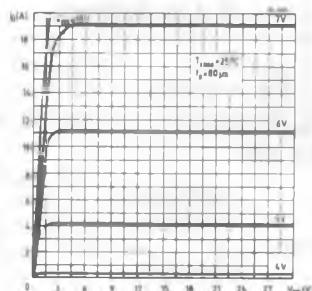
Derating curve



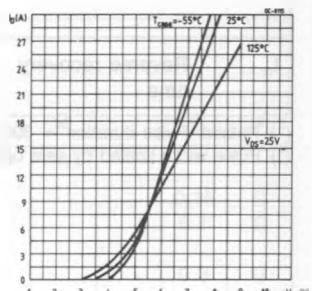
Output characteristics



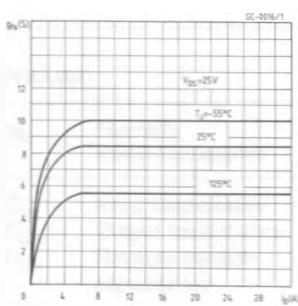
Output characteristics



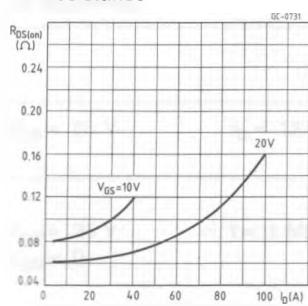
Transfer characteristics



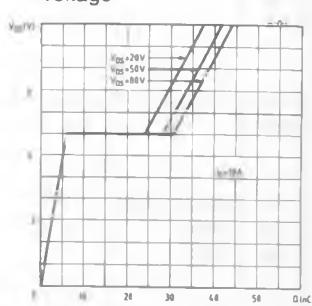
Transconductance



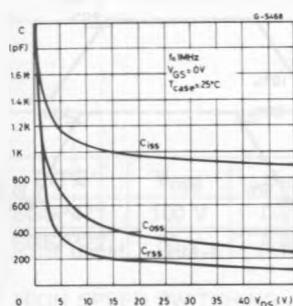
Static drain-source on resistance



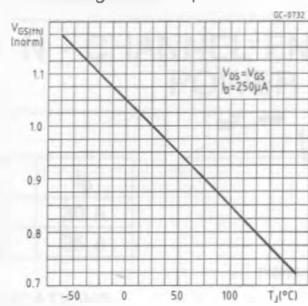
Gate charge vs gate-source voltage



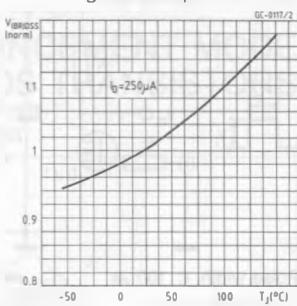
Capacitance variation



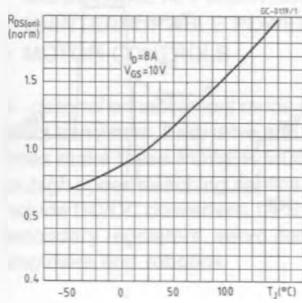
Normalized gate threshold voltage vs temperature



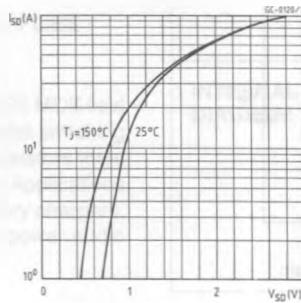
Normalized breakdown voltage vs temperature



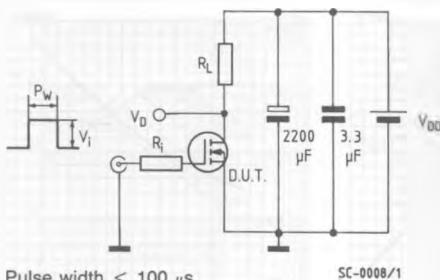
Normalized on resistance vs temperature



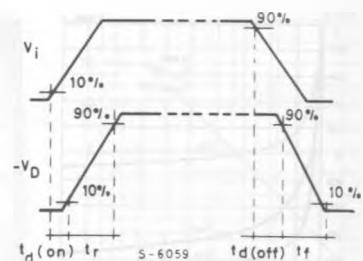
Source-drain diode forward characteristics



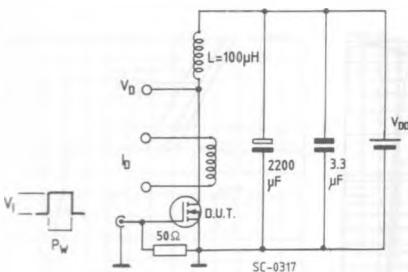
Switching times test circuit for resistive load



Switching time waveforms for resistive load

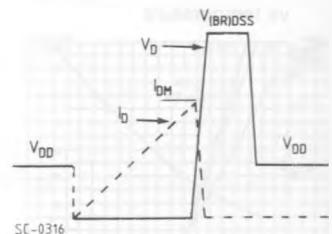


Unclamped inductive load test circuit

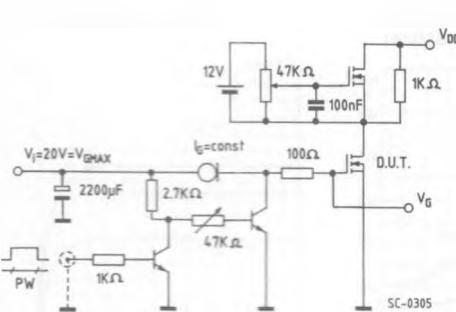


$V_i = 12 \text{ V}$ - Pulse width: adjusted to obtain specified I_{DM}

Unclamped inductive waveforms



Gate charge test circuit



PW adjusted to obtain required V_G

Body-drain diode t_{rr} measurement
Jedec test circuit