

4.8 V OPERATION SILICON RF POWER LD-MOS FET FOR 900 MHz 3 W TRANSMISSION AMPLIFIERS

DESCRIPTION

The NE5510379A is an N-channel silicon power MOS FET specially designed as the transmission power amplifier for 4.8 V GSM 900 handsets. Dies are manufactured using NEC's NEWMOS technology (NEC's 0.6 μm WSi gate lateral-diffusion MOS FET) and housed in a surface mount package. The device can deliver 35.0 dBm output power with 55% power added efficiency at 900 MHz under the 4.8 V supply voltage, or can deliver 33.5 dBm output power at 2.8 V by varying the gate voltage as a power control function.

FEATURES

- High output power : $P_{\text{out}} = 35.0$ dBm TYP. ($V_{\text{DS}} = 4.8$ V, $I_{\text{Dset}} = 600$ mA, $f = 900$ MHz, $P_{\text{in}} = 25$ dBm)
- High power added efficiency : $\eta_{\text{add}} = 55\%$ TYP. ($V_{\text{DS}} = 4.8$ V, $I_{\text{Dset}} = 600$ mA, $f = 900$ MHz, $P_{\text{in}} = 25$ dBm)
- High linear gain : $G_{\text{L}} = 13.0$ dB TYP. ($V_{\text{DS}} = 4.8$ V, $I_{\text{Dset}} = 600$ mA, $f = 900$ MHz, $P_{\text{in}} = 10$ dBm)
- Surface mount package : $5.7 \times 5.7 \times 1.1$ mm MAX.
- Single supply : $V_{\text{DS}} = 2.4$ to 6.0 V

APPLICATIONS

- Digital cellular phones : 4.8 V GSM 900 handsets
- Analog cellular phones : 2.4 V AMPS handsets
- Others : 3.5 V two-way pagers

ORDERING INFORMATION

Part Number	Package	Marking	Supplying Form
NE5510379A-T1	79A	W3	<ul style="list-style-type: none"> • 12 mm wide embossed taping • Gate pin face the perforation side of the tape • Qty 1 kpcs/reel

Remark To order evaluation samples, consult your NEC sales representative.

Part number for sample order: NE5510379A

Caution Please handle this device at static-free workstation, because this is an electrostatic sensitive device.

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Not all devices/types available in every country. Please check with local NEC representative for availability and additional information.

ABSOLUTE MAXIMUM RATINGS (T_A = +25°C)

Parameter	Symbol	Ratings	Unit
Drain to Source Voltage	V _{DS}	8.5	V
Gate to Source Voltage	V _{GSO}	5.0	V
Drain Current	I _D	1.5	A
Drain Current (Pulse Test)	I _D ^{Note}	3.0	A
Total Power Dissipation	P _{tot}	1.6	W
Channel Temperature	T _{ch}	125	°C
Storage Temperature	T _{stg}	-65 to +125	°C

Note Duty Cycle ≤ 50%, T_{on} ≤ 1 ms

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
Drain to Source Voltage	V _{DS}		2.4	4.8	6.0	V
Gate to Source Voltage	V _{GSO}		0	2.5	3.5	V
Drain Current (Pulse Test)	I _D	Duty Cycle ≤ 50%, T _{on} ≤ 1 ms	-	1.45	2.0	A
Input Power	P _{in}	f = 900 MHz, V _{DS} = 4.8 V	25	26	27	dBm

ELECTRICAL CHARACTERISTICS (T_A = +25°C)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
Gate to Source Leak Current	I _{GSO}	V _{GSS} = 5.0 V	-	-	100	nA
Saturated Drain Current (Zero Gate Voltage Drain Current)	I _{DSS}	V _{DSS} = 8.5 V	-	-	100	nA
Gate Threshold Voltage	V _{th}	V _{DS} = 3.5 V, I _{DS} = 1 mA	1.0	1.5	2.0	V
Transconductance	g _m	V _{DS} = 3.5 V, I _{DS1} = 600 mA	-	3	-	S
Drain to Source Breakdown Voltage	BV _{DS}	I _{DSS} = 10 μA	20	24	-	V
Thermal Resistance	R _{th}	Channel to Case	-	5	-	°C/W
Linear Gain	G _L	f = 900 MHz, P _{in} = 10 dBm, V _{DS} = 4.8 V, I _{Dset} = 600 mA, Note 1, 2	12.0	13.0	-	dB
Output Power	P _{out}	f = 900 MHz, P _{in} = 25 dBm, V _{DS} = 4.8 V, I _{Dset} = 600 mA, Note 1, 2	34.0	35.0	-	dBm
Operating Current	I _{op}	V _{DS} = 4.8 V, I _{Dset} = 600 mA, Note 1, 2	-	1 450	-	mA
Power Added Efficiency	η _{add}	V _{DS} = 4.8 V, I _{Dset} = 600 mA, Note 1, 2	50	55	-	%

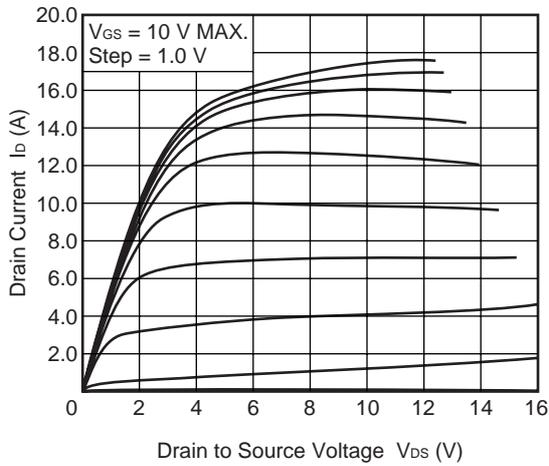
Notes 1. Peak measurement at Duty Cycle ≤ 50%, T_{on} ≤ 1 ms.

2. DC performance is 100% testing. RF performance is testing several samples per wafer.

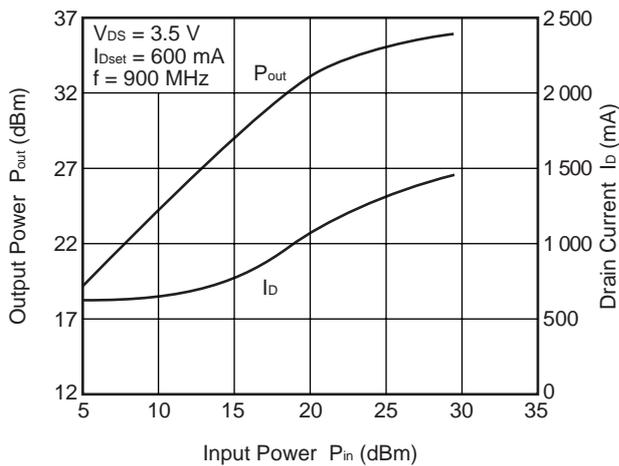
Wafer rejection criteria for standard devices is 1 reject for several samples.

TYPICAL CHARACTERISTICS (T_A = +25°C)

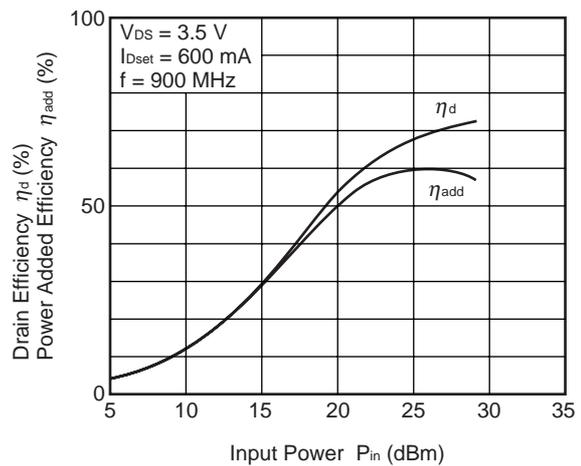
DRAIN CURRENT vs. DRAIN TO SOURCE VOLTAGE



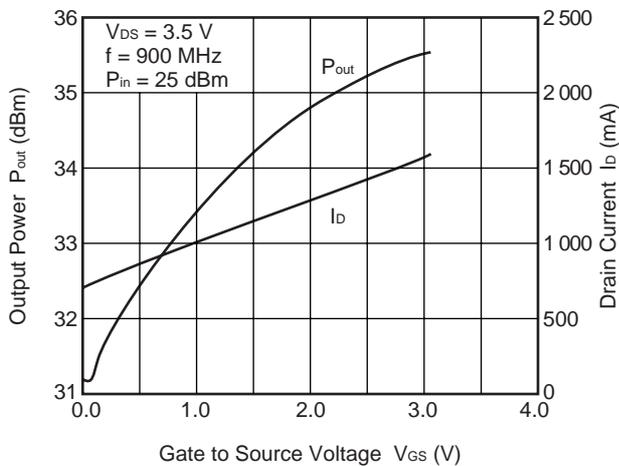
OUTPUT POWER, DRAIN CURRENT vs. INPUT POWER



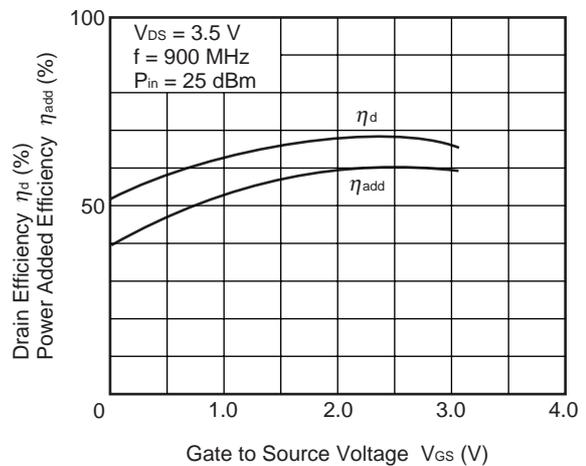
DRAIN EFFICIENCY, POWER ADDED EFFICIENCY vs. INPUT POWER



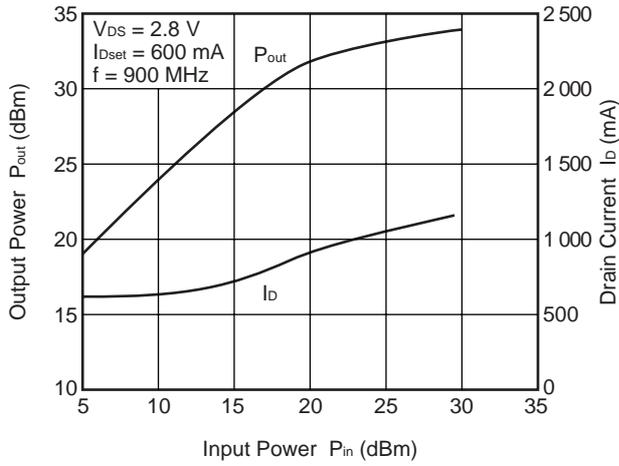
OUTPUT POWER, DRAIN CURRENT vs. GATE TO SOURCE VOLTAGE



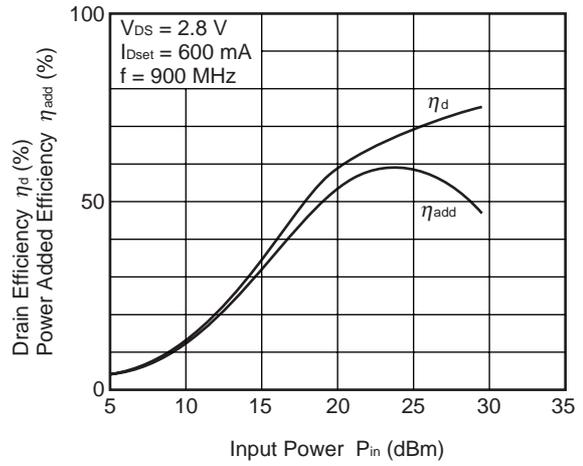
DRAIN EFFICIENCY, POWER ADDED EFFICIENCY vs. GATE TO SOURCE VOLTAGE



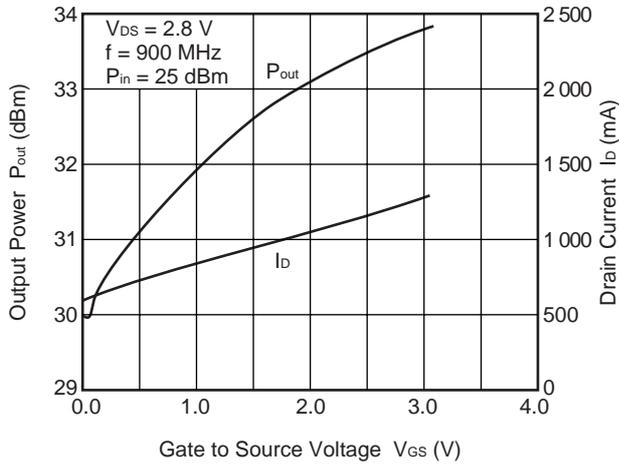
OUTPUT POWER, DRAIN CURRENT vs. INPUT POWER



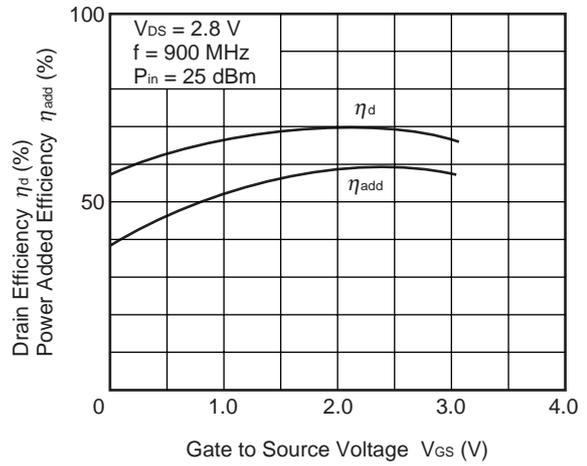
DRAIN EFFICIENCY, POWER ADDED EFFICIENCY vs. INPUT POWER



OUTPUT POWER, DRAIN CURRENT vs. GATE TO SOURCE VOLTAGE



DRAIN EFFICIENCY, POWER ADDED EFFICIENCY vs. GATE TO SOURCE VOLTAGE



Remark The graphs indicate nominal characteristics.

S-PARAMETERS

Test Conditions: $V_{DS} = 3.5\text{ V}$, $I_{Dset} = 600\text{ mA}$

Frequency GHz	S ₁₁			S ₂₁			S ₁₂		S ₂₂		MAG ^{Note}	MSG ^{Note}	K
	MAG.	ANG.	dB	MAG.	ANG.	dB	MAG.	ANG.	MAG.	ANG.	dB	dB	
0.1	0.924	-164.4	15.6	6.01	93.7	-37.1	0.014	8.7	0.895	-177.5		26.3	
0.2	0.913	-173.7	9.6	3.02	84.8	-37.1	0.014	-1.3	0.895	-179.7		23.3	
0.3	0.914	-176.8	6.0	1.99	81.0	-36.5	0.015	0.9	0.911	179.8		21.2	
0.4	0.907	-178.4	3.3	1.46	75.9	-37.7	0.013	-2.7	0.899	179.1		20.5	0.09
0.5	0.910	-179.7	1.4	1.17	72.0	-37.1	0.014	-7.4	0.920	178.2		19.2	
0.6	0.915	179.0	-0.4	0.95	68.8	-37.7	0.013	-7.6	0.912	177.9		18.6	0.28
0.7	0.914	178.2	-1.8	0.81	65.2	-38.4	0.012	-5.5	0.918	177.6		18.3	0.50
0.8	0.928	177.2	-3.2	0.69	62.3	-38.4	0.012	-8.0	0.924	176.7		17.6	0.37
0.9	0.931	176.3	-4.3	0.61	58.5	-40.0	0.010	-7.7	0.935	176.2		17.9	0.51
1.0	0.937	174.8	-5.4	0.54	55.9	-40.0	0.010	-2.5	0.944	174.7		17.3	0.35
1.1	0.949	172.9	-6.2	0.49	51.3	-40.9	0.009	-4.1	0.952	173.9		17.4	0.15
1.2	0.940	171.3	-7.3	0.43	49.2	-40.9	0.009	-5.4	0.940	172.1		16.8	0.87
1.3	0.935	170.1	-8.2	0.39	44.9	-40.9	0.009	-1.2	0.936	171.2	12.8		1.35
1.4	0.935	169.0	-9.1	0.35	43.8	-41.9	0.008	8.0	0.936	170.0	10.9		1.91
1.5	0.933	167.8	-9.9	0.32	40.4	-41.9	0.008	-5.3	0.941	169.5	10.3		2.02
1.6	0.933	166.3	-10.5	0.30	38.7	-43.1	0.007	1.8	0.935	167.9	8.7		3.01
1.7	0.930	164.8	-11.7	0.26	36.3	-43.1	0.007	19.6	0.932	167.6	6.7		4.01
1.8	0.936	163.7	-12.0	0.25	33.6	-41.9	0.008	20.2	0.946	165.5	8.4		2.37
1.9	0.928	161.6	-12.8	0.23	30.1	-43.1	0.007	18.8	0.942	164.7	6.2		3.98
2.0	0.932	159.8	-13.2	0.22	30.3	-41.9	0.008	33.8	0.948	163.0	6.9		2.90
2.1	0.932	157.7	-14.0	0.20	27.0	-43.1	0.007	55.2	0.932	162.2	4.3		5.30
2.2	0.934	156.2	-14.9	0.18	26.0	-44.4	0.006	38.1	0.944	159.8	4.4		5.55
2.3	0.930	154.3	-15.9	0.16	23.4	-41.9	0.008	49.9	0.936	158.1	2.5		5.67
2.4	0.930	152.6	-15.4	0.17	23.3	-40.9	0.009	50.5	0.951	156.4	4.6		3.34
2.5	0.930	149.8	-16.5	0.15	22.1	-44.4	0.006	44.3	0.940	154.9	2.0		7.86
2.6	0.935	148.2	-16.5	0.15	22.5	-40.9	0.009	49.7	0.941	152.9	2.8		4.46
2.7	0.934	146.2	-18.4	0.12	20.2	-40.9	0.009	65.5	0.940	151.0	0.5		6.00
2.8	0.929	144.2	-17.7	0.13	15.1	-40.0	0.010	51.9	0.958	148.9	2.9		3.44
2.9	0.933	142.7	-18.4	0.12	15.3	-39.2	0.011	70.2	0.942	147.7	0.7		4.65
3.0	0.936	140.5	-18.4	0.12	15.0	-38.4	0.012	65.1	0.960	145.7	3.2		2.48

Note When $K \geq 1$, the MAG (Maximum Available Gain) is used. $MAG = \left| \frac{S_{21}}{S_{12}} \right| (K - \sqrt{K^2 - 1})$

When $K < 1$, the MSG (Maximum Stable Gain) is used. $MSG = \left| \frac{S_{21}}{S_{12}} \right|, K = \frac{1 + |\Delta|^2 - |S_{11}|^2 - |S_{22}|^2}{2 \cdot |S_{12}| \cdot |S_{21}|}$,

$$\Delta = S_{11} \cdot S_{22} - S_{21} \cdot S_{12}$$

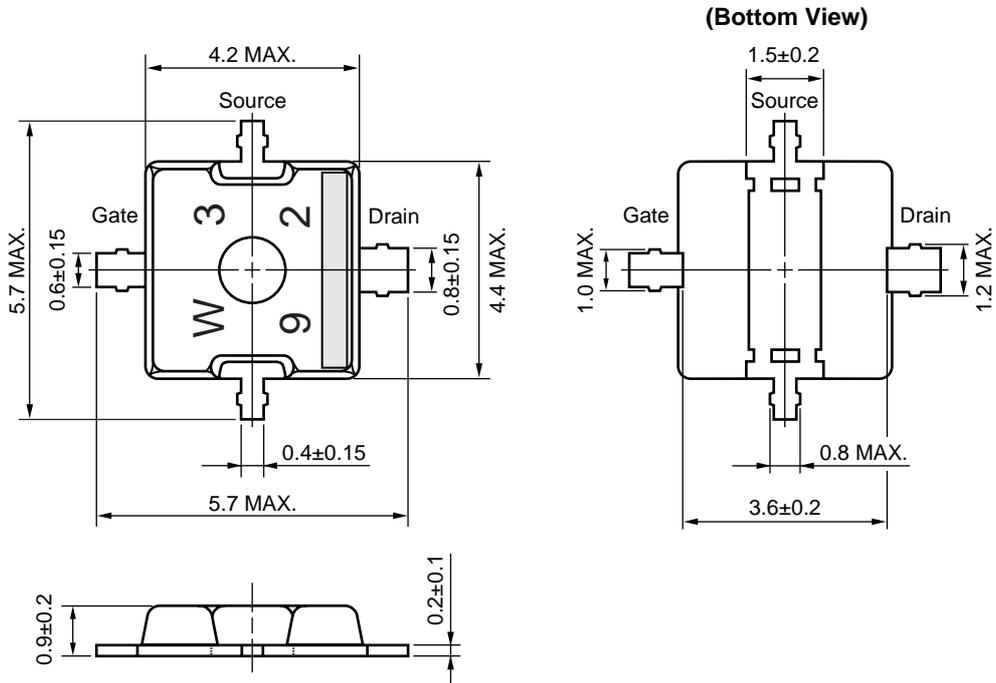
LARGE SIGNAL IMPEDANCE ($V_{DS} = 3.5\text{ V}$, $I_{Dset} = 600\text{ mA}$, $P_{in} = 25\text{ dBm}$)

f (MHz)	Z _{in} (Ω)	Z _{OL} (Ω) ^{Note}
900	TBD	TBD

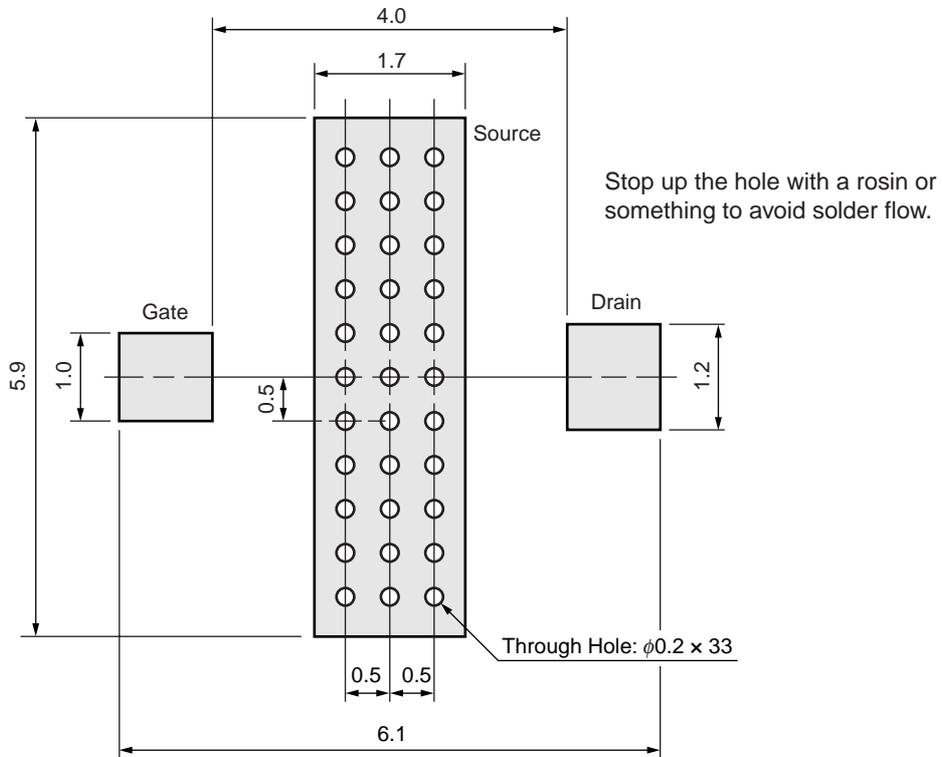
Note Z_{OL} is the conjugate of optimum load impedance at given voltage, idling current, input power and frequency.

PACKAGE DIMENSIONS

79A (UNIT: mm)



79A PACKAGE RECOMMENDED P.C.B. LAYOUT (UNIT: mm)



RECOMMENDED SOLDERING CONDITIONS

This product should be soldered and mounted under the following recommended conditions. For soldering methods and conditions other than those recommended below, contact your NEC sales representative.

Soldering Method	Soldering Conditions	Recommended Condition Symbol
Infrared Reflow	Package peak temperature: 235°C or below, Time: 30 seconds or less (at 210°C or higher), Count: 2 times or less, Exposure: limit: None ^{Note}	IR35-00-2
Partial Heating	Pin temperature: 260°C or below, Time: 5 seconds or less (per pin row) Exposure: limit: None ^{Note}	–

Note After opening the dry pack, store it at 25°C or less and 65% RH or less for the allowable storage period.

Caution Do not use different soldering methods together (except for partial heating).

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