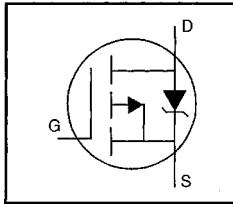


HEXFET® Power MOSFET

- Surface Mount
- Available in Tape & Reel
- Dynamic dv/dt Rating
- P-Channel
- Fast Switching
- Ease of Paralleling
- Simple Drive Requirements



$$V_{DSS} = -200V$$

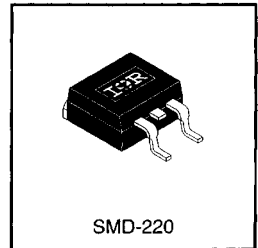
$$R_{DS(on)} = 3.0\Omega$$

$$I_D = -1.8A$$

Description

The HEXFET technology is the key to International Rectifier's advanced line of power MOSFET transistors. The efficient geometry and unique processing of the HEXFET design achieve very low on-state resistance combined with high transconductance and extreme device ruggedness.

The SMD-220 is a surface mount power package capable of accommodating die sizes up to HEX-4. It provides the highest power capability and the lowest possible on-resistance in any existing surface mount package. The SMD-220 is suitable for high current applications because of its low internal connection resistance and can dissipate up to 2.0W in a typical surface mount application.



SMD-220

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Absolute Maximum Ratings

	Parameter	Max.	Units
$I_D @ T_C = 25^\circ C$	Continuous Drain Current, $V_{GS} @ -10 V$	-1.8	A
$I_D @ T_C = 100^\circ C$	Continuous Drain Current, $V_{GS} @ -10 V$	-1.0	
I_{DM}	Pulsed Drain Current ①	-7.0	
$P_D @ T_C = 25^\circ C$	Power Dissipation	20	W
$P_D @ T_A = 25^\circ C$	Power Dissipation (PCB Mount)**	3.0	
	Linear Derating Factor	0.16	
	Linear Derating Factor (PCB Mount)**	0.025	W/°C
V_{GS}	Gate-to-Source Voltage	± 20	V
I_{LM}	Inductive Current, Clamp	-7.0	A
dv/dt	Peak Diode Recovery dv/dt ③	-5.0	V/ns
T_J, T_{STG}	Junction and Storage Temperature Range	-55 to +150	°C
	Soldering Temperature, for 10 seconds	300 (1.6mm from case)	


Thermal Resistance

	Parameter	Min.	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	—	—	6.4	°C/W
$R_{\theta JA}$	Junction-to-Ambient (PCB mount)**	—	—	40	
$R_{\theta JA}$	Junction-to-Ambient	—	—	62	


** When mounted on 1" square PCB (FR-4 or G-10 Material).

For recommended footprint and soldering techniques refer to application note #AN-994.

Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Test Conditions
V _{(BR)DSS}	Drain-to-Source Breakdown Voltage	-200	—	—	V	V _{GS} =0V, I _D =-250μA
ΔV _{(BR)DSS} /ΔT _J	Breakdown Voltage Temp. Coefficient	—	-0.23	—	V/°C	Reference to 25°C, I _D =-1mA
R _{DS(on)}	Static Drain-to-Source On-Resistance	—	—	3.0	Ω	V _{GS} =-10V, I _D =-0.90A ④
V _{GS(th)}	Gate Threshold Voltage	-2.0	—	-4.0	V	V _{DS} =V _{GS} , I _D =-250μA
g _{fs}	Forward Transconductance	0.90	—	—	S	V _{DS} =-50V, I _D =-0.90A ④
I _{DSS}	Drain-to-Source Leakage Current	—	—	-100	μA	V _{DS} =-200V, V _{GS} =0V
		—	—	-500		V _{DS} =-160V, V _{GS} =0V, T _J =125°C
I _{GSS}	Gate-to-Source Forward Leakage	—	—	-100	nA	V _{GS} =-20V
	Gate-to-Source Reverse Leakage	—	—	100		V _{GS} =20V
Q _g	Total Gate Charge	—	—	11	nC	I _D =-3.5A
Q _{gs}	Gate-to-Source Charge	—	—	7.0		V _{DS} =-160V
Q _{gd}	Gate-to-Drain ("Miller") Charge	—	—	4.0		V _{GS} =-10V See Fig. 6 and 12 ④
t _{d(on)}	Turn-On Delay Time	—	8.0	—	ns	V _{DD} =-100V
t _r	Rise Time	—	15	—		I _D =-0.90A
t _{d(off)}	Turn-Off Delay Time	—	10	—		R _G =50Ω
t _f	Fall Time	—	8.0	—		R _D =110Ω See Figure 10 ④
L _D	Internal Drain Inductance	—	4.5	—	nH	Between lead, 6 mm (0.25in.) from package and center of die contact
L _S	Internal Source Inductance	—	7.5	—		
C _{iss}	Input Capacitance	—	170	—	pF	V _{GS} =0V
C _{oss}	Output Capacitance	—	50	—		V _{DS} =-25V
C _{rss}	Reverse Transfer Capacitance	—	15	—		f=1.0MHz See Figure 5

Source-Drain Ratings and Characteristics

	Parameter	Min.	Typ.	Max.	Units	Test Conditions
I _S	Continuous Source Current (Body Diode)	—	—	-1.8	A	MOSFET symbol showing the integral reverse p-n junction diode. 
I _{SM}	Pulsed Source Current (Body Diode) ①	—	—	-7.0		
V _{SD}	Diode Forward Voltage	—	—	-5.8	V	T _J =25°C, I _S =-1.8A, V _{GS} =0V ④
t _{rr}	Reverse Recovery Time	—	240	360	ns	T _J =25°C, I _F =-1.8A
Q _{rr}	Reverse Recovery Charge	—	1.7	2.6	μC	di/dt=100A/μs ④
t _{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by L _S +L _D)				

Notes:

- ① Repetitive rating; pulse width limited by max. junction temperature (See Figure 11)
- ② Not Applicable
- ③ I_{SD} ≤ -1.8A, di/dt ≤ 70A/μs, V_{DD} ≤ V_{(BR)DSS}, T_J ≤ 150°C
- ④ Pulse width ≤ 300 μs; duty cycle ≤ 2%.

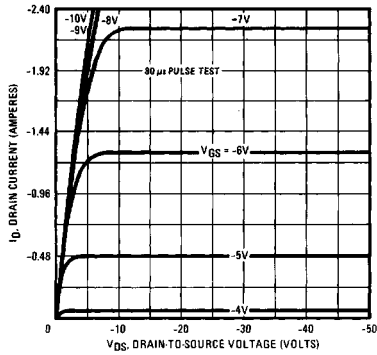


Fig. 1 — Typical Output Characteristics

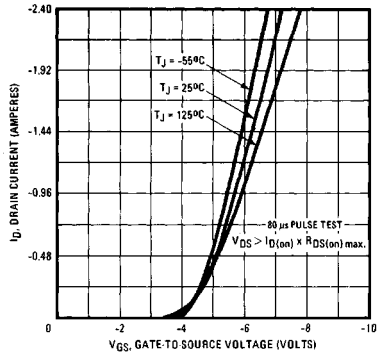


Fig. 2 — Typical Transfer Characteristics

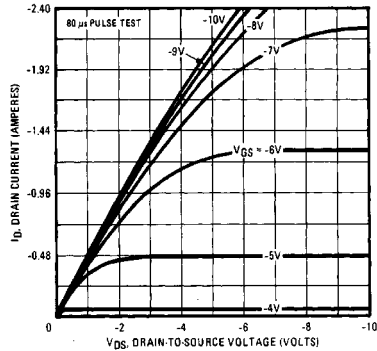


Fig. 3 — Typical Saturation Characteristics

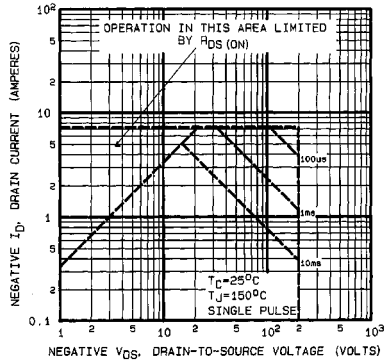


Fig. 4 — Maximum Safe Operating Area

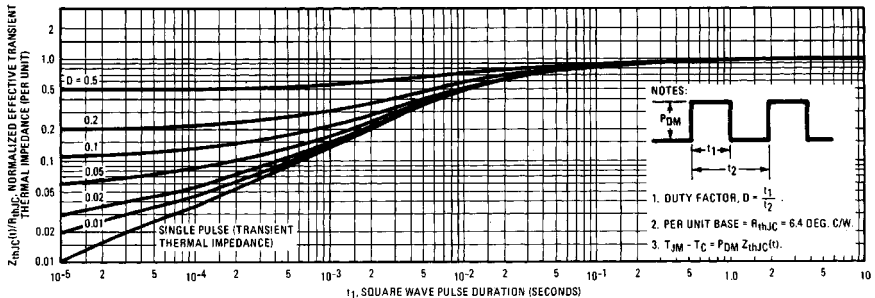


Fig. 5 — Maximum Effective Transient Thermal Impedance, Junction-to-Case Vs. Pulse Duration

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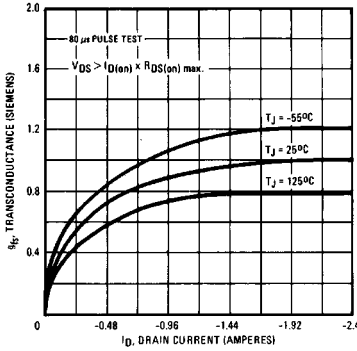


Fig. 6 — Typical Transconductance Vs. Drain Current

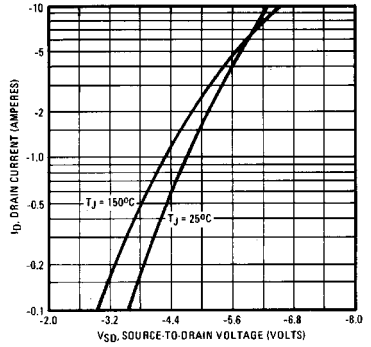


Fig. 7 — Typical Source-Drain Diode Forward Voltage

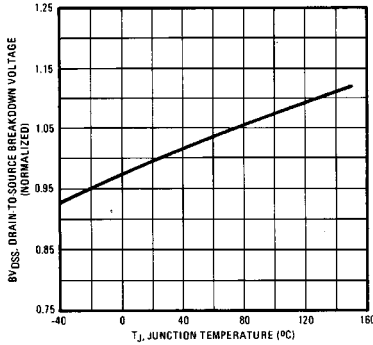


Fig. 8 — Breakdown Voltage Vs. Temperature

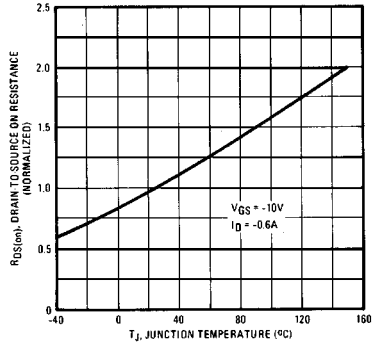


Fig. 9 — Normalized On-Resistance Vs. Temperature

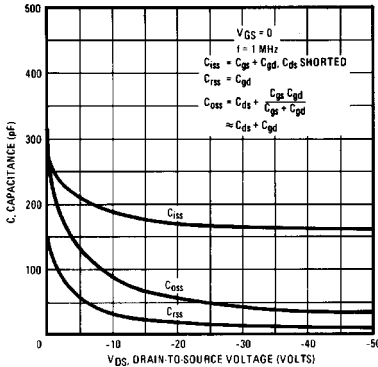


Fig. 10 — Typical Capacitance Vs. Drain-to-Source Voltage

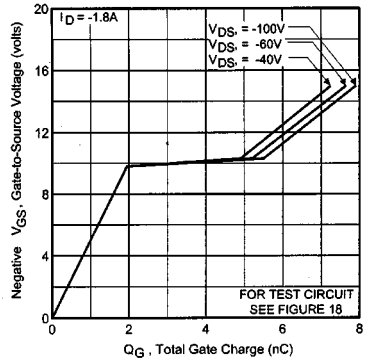


Fig. 11 — Typical Gate Charge Vs. Gate-to-Source Voltage

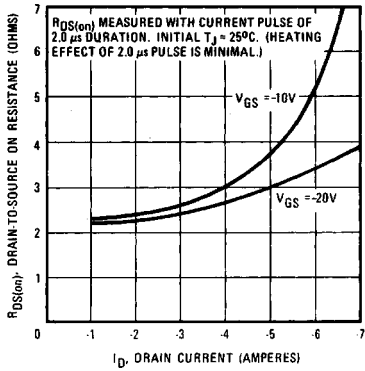


Fig. 12 — Typical On-Resistance Vs. Drain Current

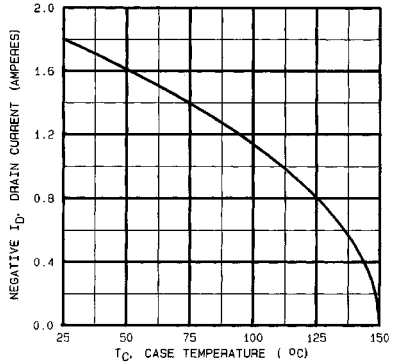


Fig. 13 — Maximum Drain Current Vs. Case Temperature

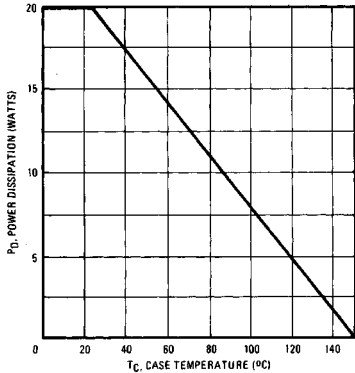


Fig. 14 — Power Vs. Temperature Derating Curve

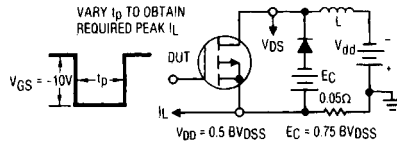


Fig. 15 — Clamped Inductive Test Circuit

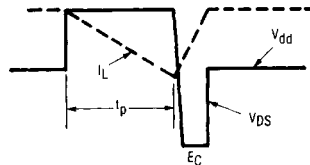


Fig. 16 — Clamped Inductive Waveforms

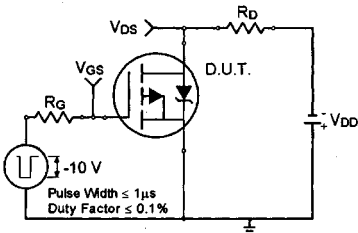


Fig. 17a — Switching Time Test Circuit

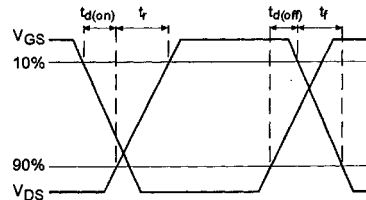


Fig. 17b — Switching Time Waveforms

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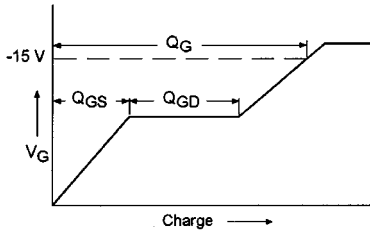


Fig. 18a — Basic Gate Charge Waveform

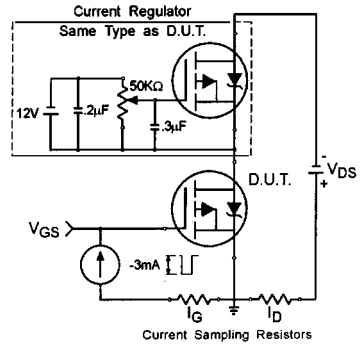


Fig. 18b — Gate Charge Test Circuit

Appendix A: Figure 14, Peak Diode Recovery dv/dt Test Circuit – See page 1506

Appendix B: Package Outline Mechanical Drawing – See page 1507

Appendix C: Part Marking Information – See page 1515

Appendix D: Tape & Reel Information – See page 1519