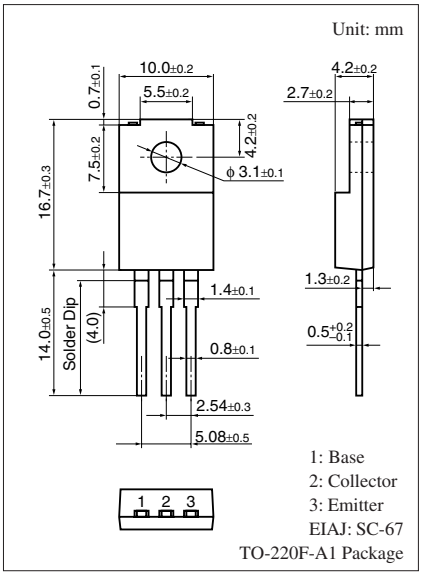
2SD1535

Silicon NPN triple diffusion planar type darlington

For high power amplification

■ Features

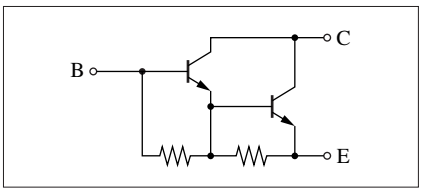
- Excellent collector current I_C characteristics of forward current transfer ratio h_{FE}
- High collector-base voltage (Emitter open) V_{CBO}
- Wide safe operation area
- Full-pack package which can be installed to the heat sink with one screw



■ Absolute Maximum Ratings $T_C = 25°C$

Parameter		Symbol	Rating	Unit
Collector-base voltage (Emitter open)		V_{CBO}	500	V
Collector-emitter voltage (Base open)		V_{CEO}	400	V
Emitter-base voltage (Collector open)		V_{EBO}	12	V
Collector current		I_C	7	A
Peak collector current		I_{CP}	14	A
Base current		I_B	0.5	A
Collector power dissipation		P_C	50	W
	$T_a = 25°C$		2.0	
Junction temperature		T_j	150	°C
Storage temperature		T_{stg}	−55 to +150	°C

Internal Connection

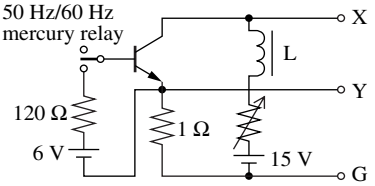


■ Electrical Characteristics $T_C = 25°C \pm 3°C$

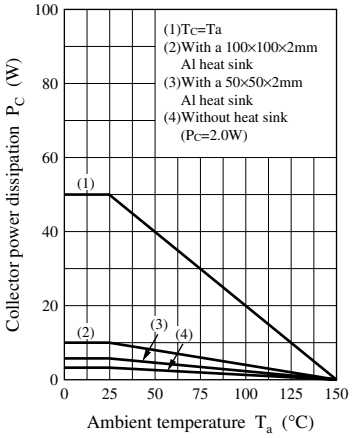
Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Collector-emitter sustaining voltage *	$V_{CEO(SUS)}$	I_C = 100 mA, R_{BE} = ∞, L = 25 mH	400			V
Collector-base cutoff current (Emitter open)	I_{CBO}	V_{CB} = 500 V, I_E = 0			100	μA
Collector-emitter cutoff current (Base open)	I_{CEO}	V_{CE} = 400 V, I_B = 0			100	μA
Emitter-base cutoff current (Collector open)	I_{EBO}	V_{EB} = 12 V, I_C = 0			100	mA
Forward current transfer ratio	h_{FE1}	V_{CE} = 2 V, I_C = 2 A	500			—
	h_{FE2}	V_{CE} = 2 V, I_C = 6 A	200			
Collector-emitter saturation voltage	$V_{CE(sat)}$	I_C = 7 A, I_B = 70 mA			2.0	V
Base-emitter saturation voltage	$V_{BE(sat)}$	I_C = 7 A, I_B = 70 mA			2.5	V
Transition frequency	f_T	V_{CE} = 10 V, I_C = 0.5 A, f = 1 MHz		20		MHz
Collector output capacitance (Common base, input open circuited)	C_{ob}	V_{CB} = 10 V, I_E = 0, f = 1 MHz		70		pF
Turn-on time	t_{on}	I_C = 7 A, I_{B1} = 70 mA, I_{B2} = −70 mA, V_{CC} = 300 V		1.5		μs
Storage time	t_{stg}			5.0		μs
Fall time	t_f			6.5		μs

Note) 1. Measuring methods are based on JAPANESE INDUSTRIAL STANDARD JIS C 7030 measuring methods for transistors.

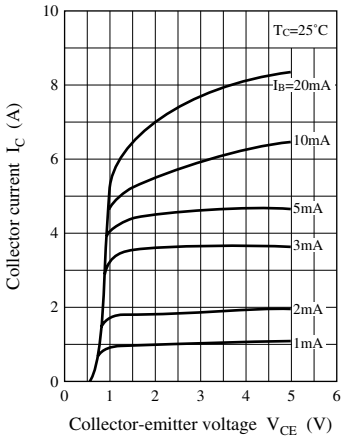
2. *: $V_{CEO(SUS)}$ Test circuit



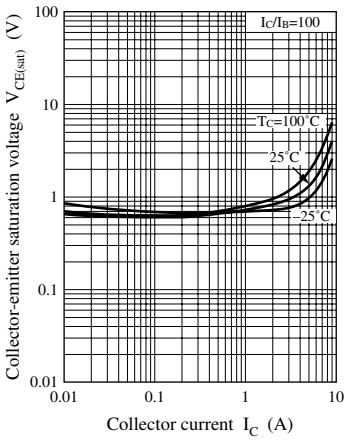
P_C — T_a



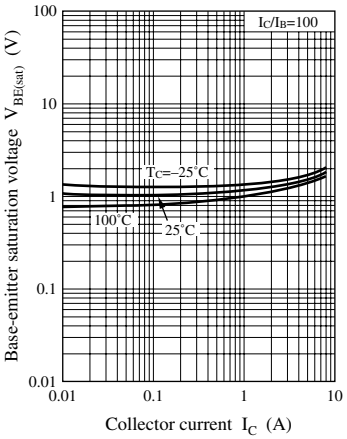
I_C — V_{CE}



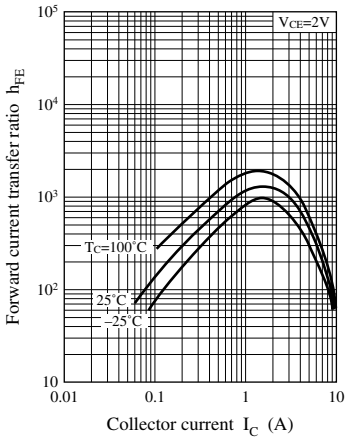
$V_{CE(sat)}$ — I_C



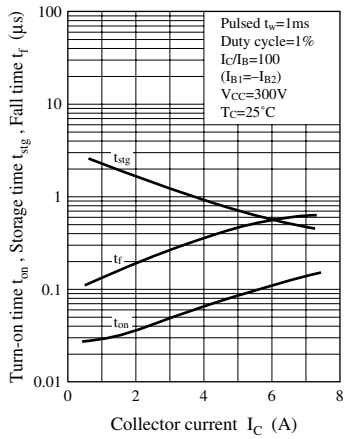
$V_{BE(sat)}$ — I_C



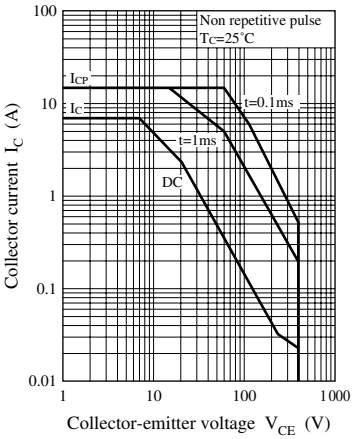
h_{FE} — I_C



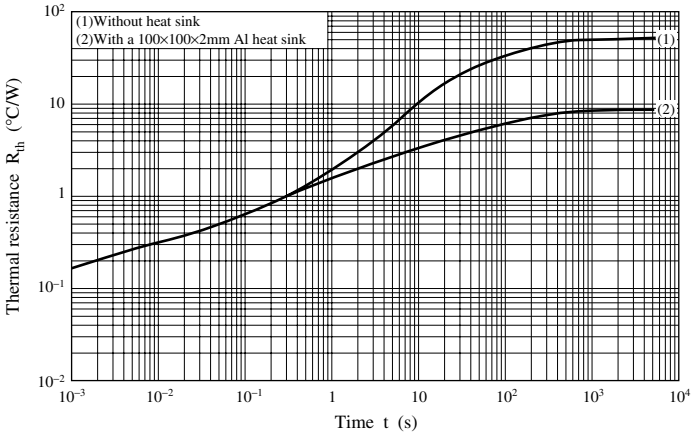
t_{on}, t_{stg}, t_f — I_C



Safe operation area



R_{th} — t



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