



SANYO Semiconductors

# DATA SHEET

An ON Semiconductor Company

## 2SA2112 — PNP Epitaxial Planar Silicon Transistor High Current Switching Applications

### Applications

- DC-DC converter, relay drivers, lamp drivers, motor drivers, strobes

### Features

- Adoption of MBIT process
- Low collector-to-emitter saturation voltage
- Large current capacity
- High-speed switching

### Specifications

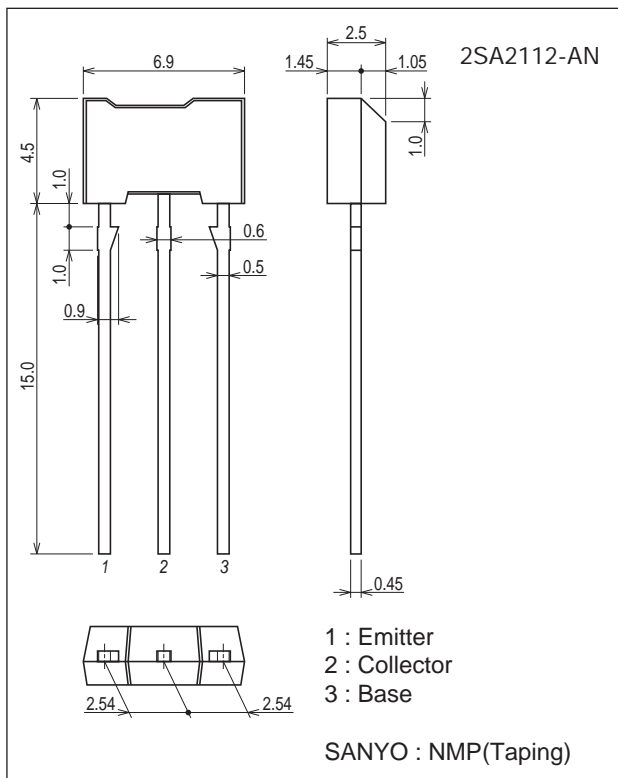
Absolute Maximum Ratings at Ta=25°C

Parameter	Symbol	Conditions	Ratings	Unit
Collector-to-Base Voltage	VCBO		-50	V
Collector-to-Emitter Voltage	VCES		-50	V
Collector-to-Emitter Voltage	VCEO		-50	V
Emitter-to-Base Voltage	VEBO		-6	V
Collector Current	IC		-3	A
Collector Current (Pulse)	ICP		-6	A
Base Current	IB		-600	mA
Collector Dissipation	PC		1	W
Junction Temperature	Tj		150	°C
Storage Temperature	Tstg		-55 to +150	°C

### Package Dimensions

unit : mm (typ)

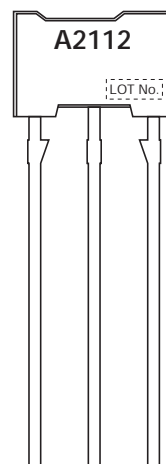
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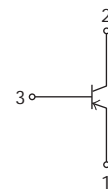
### Product & Package Information

- Package : NMP(Taping)
- JEITA, JEDEC : SC-71
- Minimum Packing Quantity : 2,500 pcs./box

### Marking(NMP(Taping))



### Electrical Connection

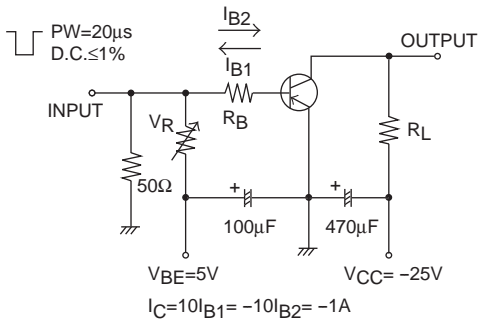


## 2SA2112

### Electrical Characteristics at $T_a=25^\circ\text{C}$

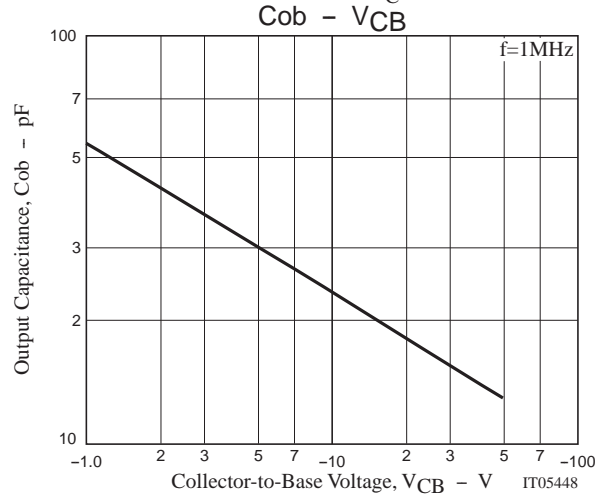
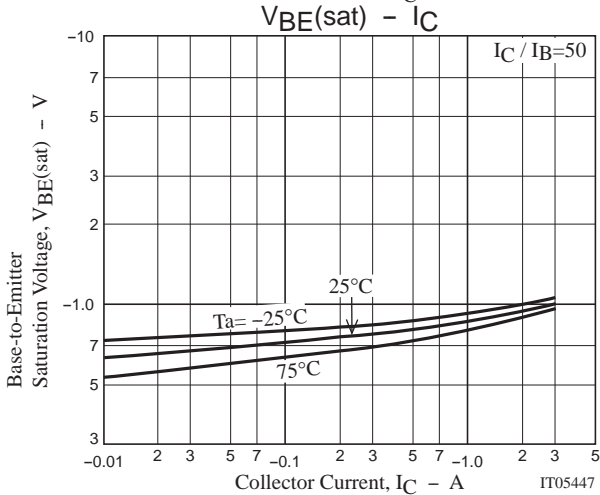
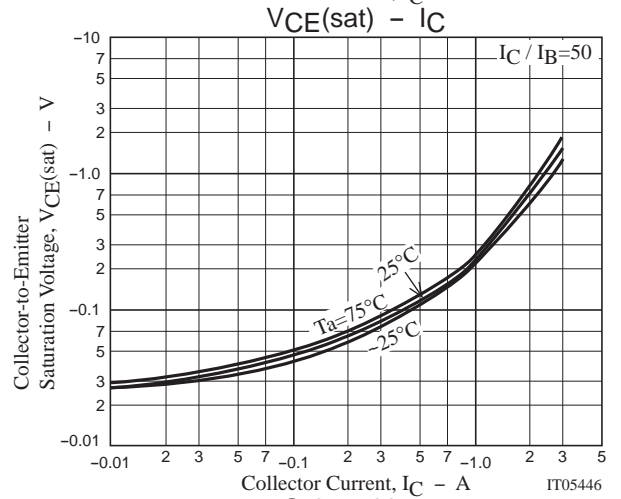
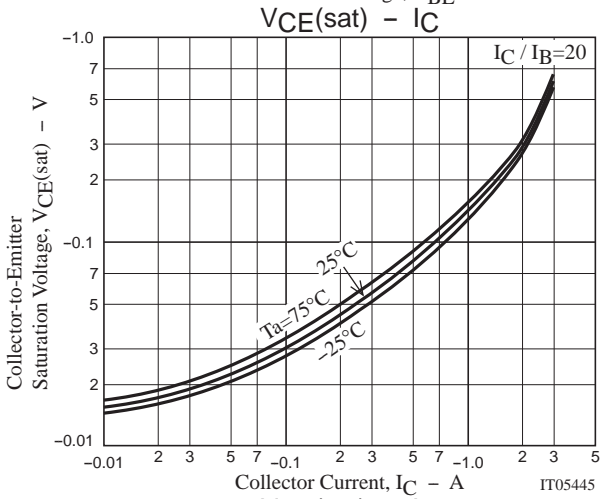
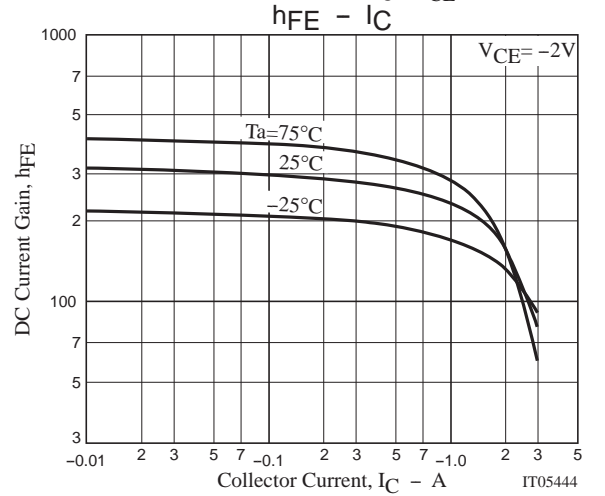
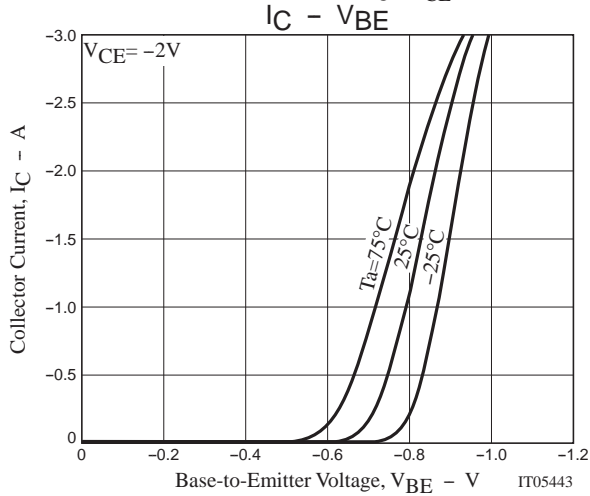
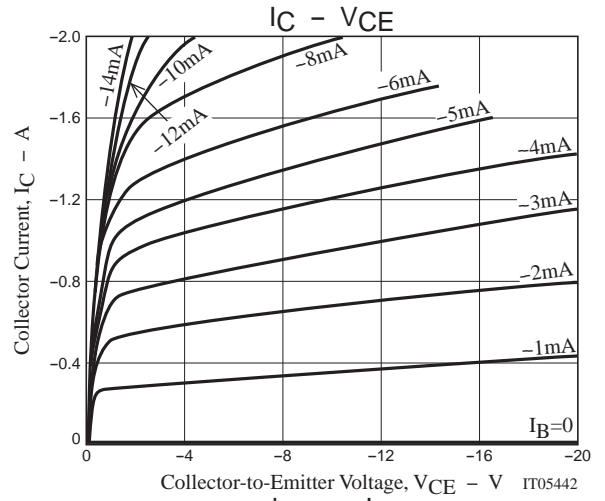
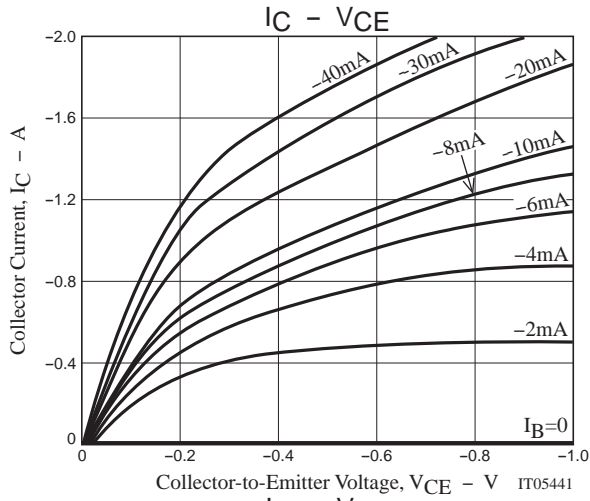
Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Collector Cutoff Current	$I_{CBO}$	$V_{CB}=-40\text{V}, I_E=0\text{A}$			-1	$\mu\text{A}$
Emitter Cutoff Current	$I_{EBO}$	$V_{EB}=-4\text{V}, I_C=0\text{A}$			-1	$\mu\text{A}$
DC Current Gain	$h_{FE}$	$V_{CE}=-2\text{V}, I_C=-100\text{mA}$	200		560	
Gain-Bandwidth Product	$f_T$	$V_{CE}=-10\text{V}, I_C=-500\text{mA}$		390		MHz
Output Capacitance	$C_{ob}$	$V_{CB}=-10\text{V}, f=1\text{MHz}$		24		pF
Collector-to-Emitter Saturation Voltage	$V_{CE(sat)1}$	$I_C=-1\text{A}, I_B=-50\text{mA}$		-135	-270	mV
	$V_{CE(sat)2}$	$I_C=-2\text{A}, I_B=-100\text{mA}$		-260	-700	mV
Base-to-Emitter Saturation Voltage	$V_{BE(sat)}$	$I_C=-2\text{A}, I_B=-100\text{mA}$		-0.88	-1.2	V
Collector-to-Base Breakdown Voltage	$V_{(BR)CBO}$	$I_C=-10\mu\text{A}, I_E=0\text{A}$	-50			V
Collector-to-Emitter Breakdown Voltage	$V_{(BR)CES}$	$I_C=-100\mu\text{A}, R_{BE}=0\text{A}$	-50			V
	$V_{(BR)CEO}$	$I_C=-1\text{mA}, R_{BE}=\infty$	-50			V
Emitter-to-Base Breakdown Voltage	$V_{(BR)EBO}$	$I_E=-10\mu\text{A}, I_C=0\text{A}$	-6			V
Turn-ON Time	$t_{on}$	See specified Test Circuit.		30		ns
Storage Time	$t_{stg}$			230		ns
Fall Time	$t_f$			18		ns

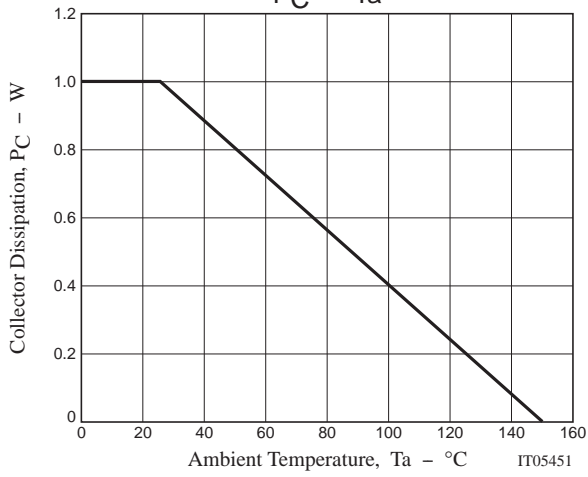
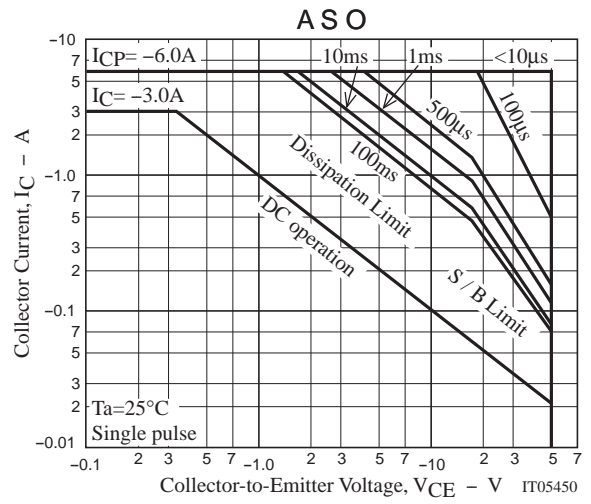
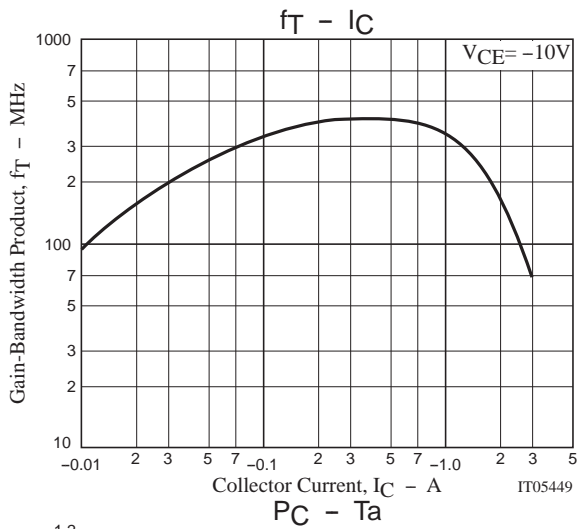
### Switching Time Test Circuit



### Ordering Information

Device	Package	Shipping	memo
2SA2112-AN	NMP(Taping)	2,500pcs./box	Pb Free





Bag Packing Specification

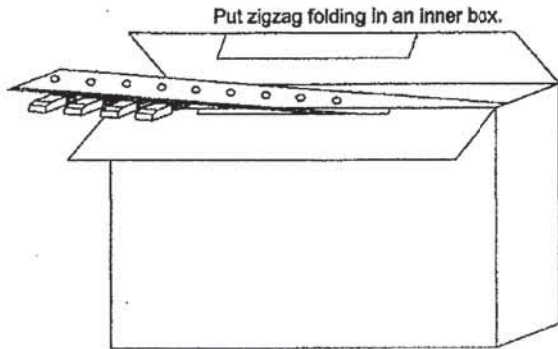
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NMP (Zigzag folding)

Storage package Outline name	Package type	Maximum Number of devices contained (pcs.)		Packing format	
		Inner box No.	Storage quantity	Outer box (C-6)	Outer box (C-8)
NMP	AN/AZ	C-3 Inner box Dimensions :mm(external) 330×45×125	2,500	8 inner boxes contained(20,000pcs.) Outer box Dimensions:mm(external) 585×345×195	4 inner boxes contained(10,000pcs.) Outer box Dimensions:mm(external) 345×300×195

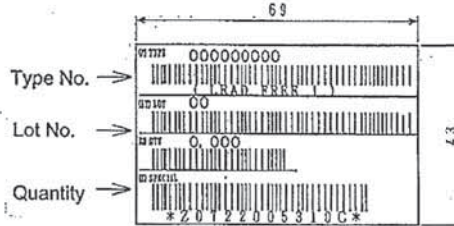
1. Packing format

Packing method



2. Bar code label

(Unit : mm)

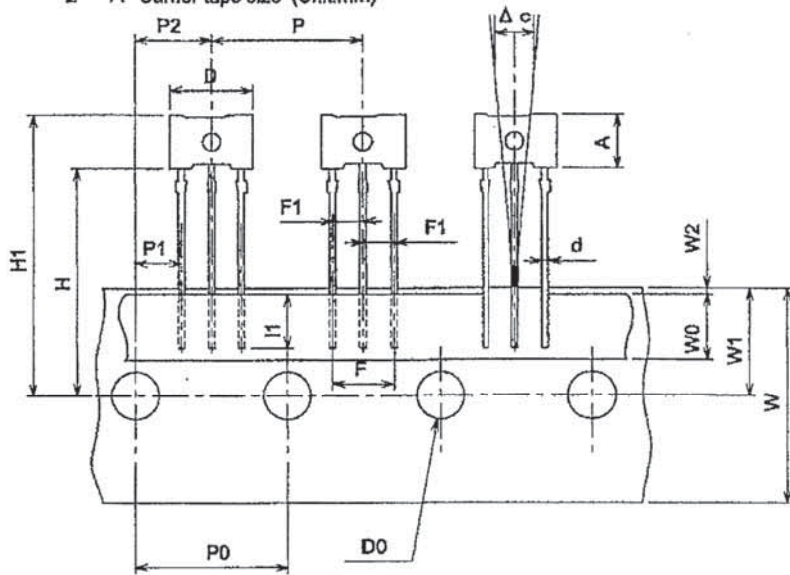


\*LEAD FREE 1:

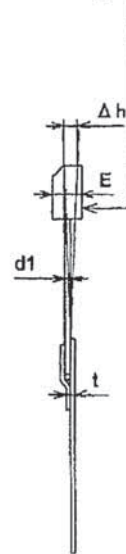
Lead-free External terminal surface treatment product.

2. Taping specifications

2-1. Carrier tape size (Unit:mm)



Marking surface



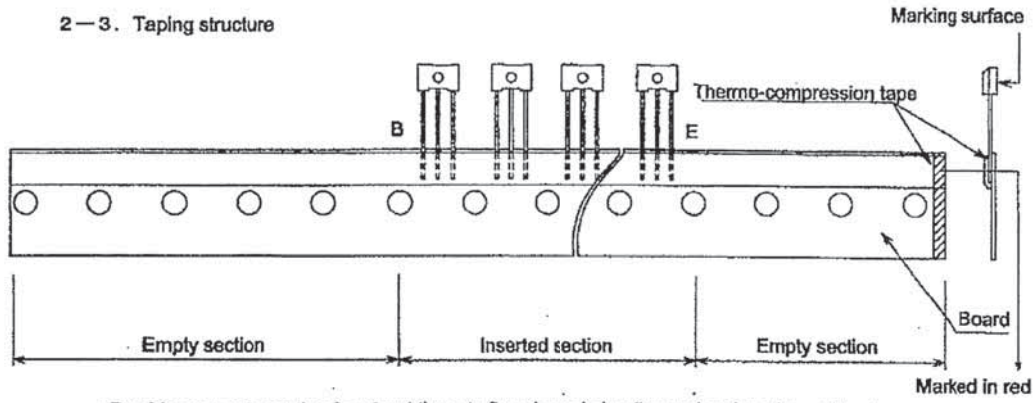
2-2. Taping size standard

Item	Symbol	Standard	Tolerance
Work piece outside diameter	D	6.9	±0.2
	E	2.5	±0.2
Work piece height	A	4.5	±0.2
Lead wire diameter	d	0.5	±0.1
Lead wire thickness	d1	0.45	±0.1
Bonded lead wire	I1	3.0MIN	
Pitch between products	P	12.7	±0.5
Pitch between perforations	P0	12.7	±0.2
Total pitch for 21 perforations	P0×20	254.0	±1.0
Distance between lead wire	F	5.0	+0.8 -0.2
Lead wire pitch distance	F1	2.54	+0.4 -0.1
Displacement of perforations	P1	3.81	±0.3
	P2	6.35	±0.3
Displacement of tape	W2	0~0.5	

Unit:mm

Item	Symbol	Standard	Tolerance
Tape width	W	18.0	±0.5
Adhesive tape	W0	6.0	±0.5
Displacement of perforations	W1	9.0	±0.5
Work piece bottom surface position	H	19.0	+1.0 -0.5
Work piece upper limit position	H1	23.5	±1.0
Perforations diameter	D0	φ4.0	±0.2
Tape thickness (total thickness)	t	0.6	±0.2
Product inclination	Δc	0	±0.7
Product inclination	Δh	0	±1.0

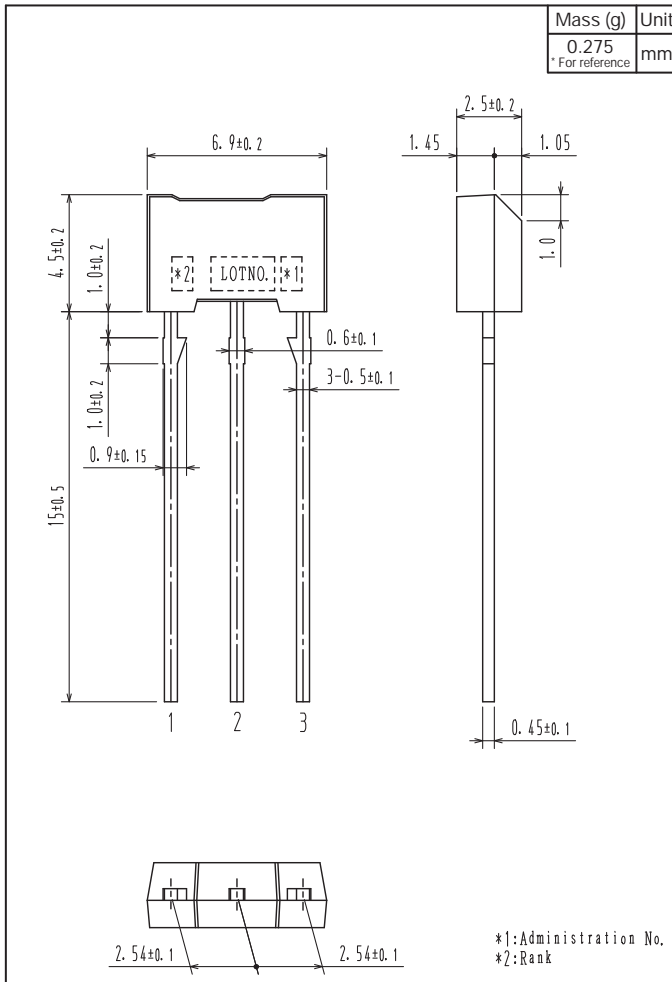
2—3. Taping structure



- Provide an empty section for about three to five pieces in leading and end portions of the tape.
- Provide an empty section in the fold-back portion.
- Provide marking in red to the E-side end of the board.

Outline Drawing

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