

2N6497

High Voltage NPN Silicon Power Transistors

These devices are designed for high voltage inverters, switching regulators and line-operated amplifier applications. Especially well suited for switching power supply applications.

Features

- High Collector–Emitter Sustaining Voltage –
 $V_{CEO(sus)} = 250 \text{ Vdc (Min)}$
- Excellent DC Current Gain –
 $h_{FE} = 10\text{--}75 @ I_C = 2.5 \text{ Adc}$
- Low Collector–Emitter Saturation Voltage @ $I_C = 2.5 \text{ Adc}$ –
 $V_{CE(sat)} = 1.0 \text{ Vdc (Max)}$
- Pb–Free Packages are Available*

MAXIMUM RATINGS (Note 1)

Rating	Symbol	Value	Unit
Collector–Emitter Voltage	V_{CEO}	250	Vdc
Collector–Base Voltage	V_{CB}	350	Vdc
Emitter–Base Voltage	V_{EB}	6.0	Vdc
Collector Current – Continuous – Peak	I_C	5.0 10	Adc
Base Current	I_B	2.0	Adc
Total Power Dissipation @ $T_C = 25^\circ\text{C}$ Derate above 25°C	P_D	80 0.64	W W/ $^\circ\text{C}$
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–65 to +150	$^\circ\text{C}$

THERMAL CHARACTERISTICS

Characteristics	Symbol	Max	Unit
Thermal Resistance, Junction–to–Case	$R_{\theta JC}$	1.56	$^\circ\text{C/W}$

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. Indicates JEDEC Registered Data.

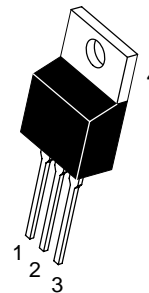


ON Semiconductor®

<http://onsemi.com>

**5 AMPERE
POWER TRANSISTORS
NPN SILICON
250 VOLTS – 80 WATTS**

MARKING DIAGRAM



TO-220AB
CASE 221A
STYLE 1



2N6497 = Device Code
G = Pb–Free Package
A = Assembly Location
Y = Year
WW = Work Week

ORDERING INFORMATION

Device	Package	Shipping
2N6497	TO-220AB	50 Units / Rail
2N6497G	TO-220AB (Pb–Free)	50 Units / Rail

*For additional information on our Pb–Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

2N6497

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted) (Note 2)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector–Emitter Sustaining Voltage (Note 3) ($I_C = 25\text{ mAdc}$, $I_B = 0$)	$V_{CE(sus)}$	250	–	–	Vdc
Collector Cutoff Current ($V_{CE} = 350\text{ Vdc}$, $V_{BE(off)} = 1.5\text{ Vdc}$) ($V_{CE} = 175\text{ Vdc}$, $V_{BE(off)} = 1.5\text{ Vdc}$, $T_C = 100^\circ\text{C}$)	I_{CEX}	–	–	1.0 10	mAdc
Emitter Cutoff Current ($V_{BE} = 6.0\text{ Vdc}$, $I_C = 0$)	I_{EBO}	–	–	1.0	mAdc
ON CHARACTERISTICS (Note 3)					
DC Current Gain ($I_C = 2.5\text{ Adc}$, $V_{CE} = 10\text{ Vdc}$) ($I_C = 5.0\text{ Adc}$, $V_{CE} = 10\text{ Vdc}$)	h_{FE}	10 3.0	– –	75 –	–
Collector–Emitter Saturation Voltage ($I_C = 2.5\text{ Adc}$, $I_B = 500\text{ mAdc}$) ($I_C = 5.0\text{ Adc}$, $I_B = 2.0\text{ Adc}$)	$V_{CE(sat)}$	– –	– –	1.0 5.0	Vdc
Base–Emitter Saturation Voltage ($I_C = 2.5\text{ Adc}$, $I_B = 500\text{ mAdc}$) ($I_C = 5.0\text{ Adc}$, $I_B = 2.0\text{ Adc}$)	$V_{BE(sat)}$	– –	– –	1.5 2.5	Vdc
DYNAMIC CHARACTERISTICS					
Current–Gain – Bandwidth Product ($I_C = 250\text{ mAdc}$, $V_{CE} = 10\text{ Vdc}$, $f = 1.0\text{ MHz}$)	f_T	5.0	–	–	MHz
Output Capacitance ($V_{CB} = 10\text{ Vdc}$, $I_E = 0$, $f = 100\text{ kHz}$)	C_{ob}	–	–	150	pF
SWITCHING CHARACTERISTICS					
Rise Time ($V_{CC} = 125\text{ Vdc}$, $I_C = 2.5\text{ Adc}$, $I_{B1} = 0.5\text{ Adc}$)	t_r	–	0.4	1.0	μs
Storage Time ($V_{CC} = 125\text{ Vdc}$, $I_C = 2.5\text{ Adc}$, $V_{BE} = 5.0\text{ Vdc}$, $I_{B1} = I_{B2} = 0.5\text{ Adc}$)	t_s	–	1.4	2.5	μs
Fall Time ($V_{CC} = 125\text{ Vdc}$, $I_C = 2.5\text{ Adc}$, $I_{B1} = I_{B2} = 0.5\text{ Adc}$)	t_f	–	0.45	1.0	μs

- Indicates JEDEC Registered Data.
- Pulse Test: Pulse Width $\leq 300\ \mu\text{s}$, Duty Cycle $\leq 2.0\%$.

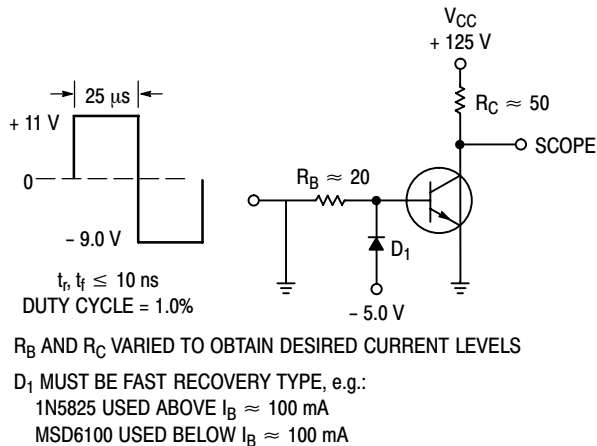


Figure 1. Switching Time Test Circuit

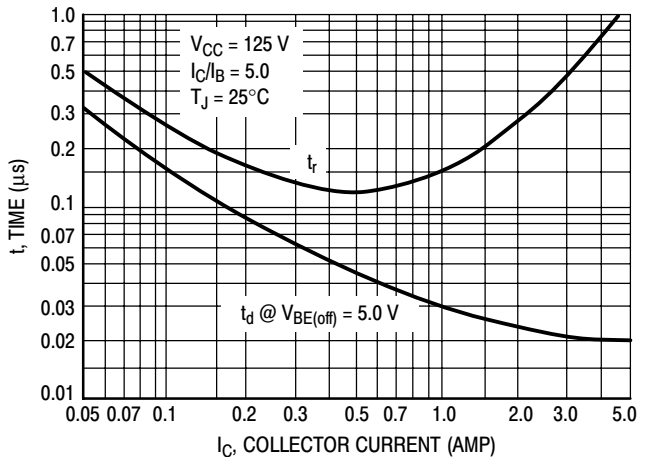


Figure 2. Turn–On Time

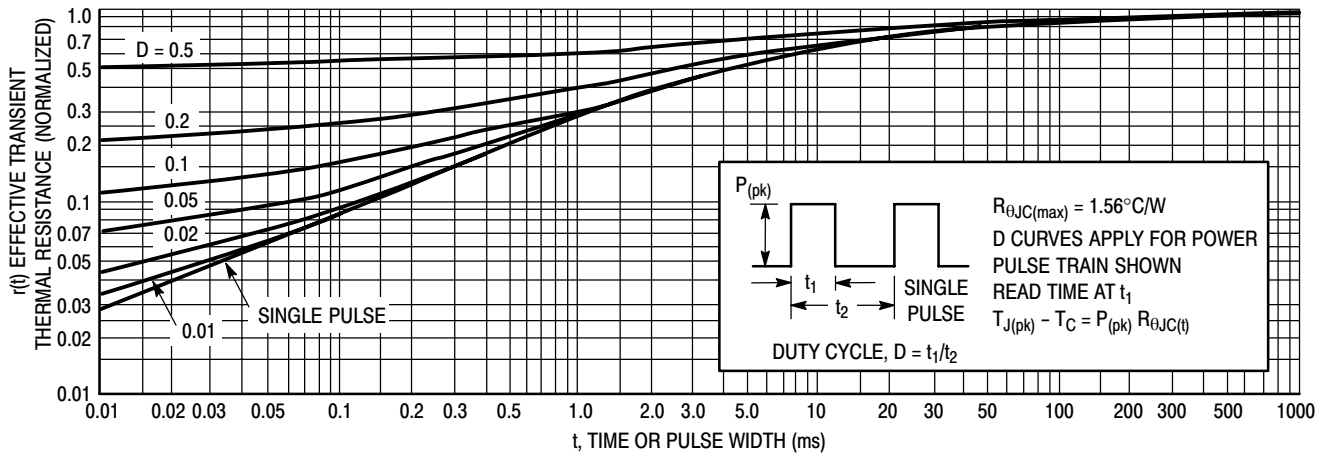


Figure 3. Thermal Response

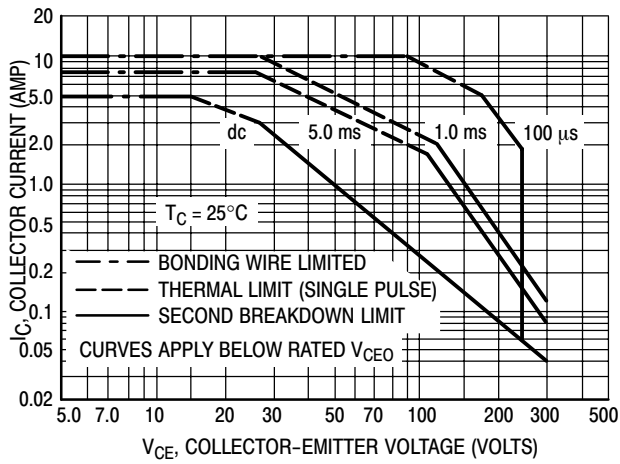


Figure 4. Active-Region Safe Operating Area

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 4 is based on $T_C = 25^\circ\text{C}$; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq 150^\circ\text{C}$. $T_{J(pk)}$ may be calculated from the data in Figure 3. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltage shown on Figure 4 may be found at any case temperature by using the appropriate curve on Figure 6.

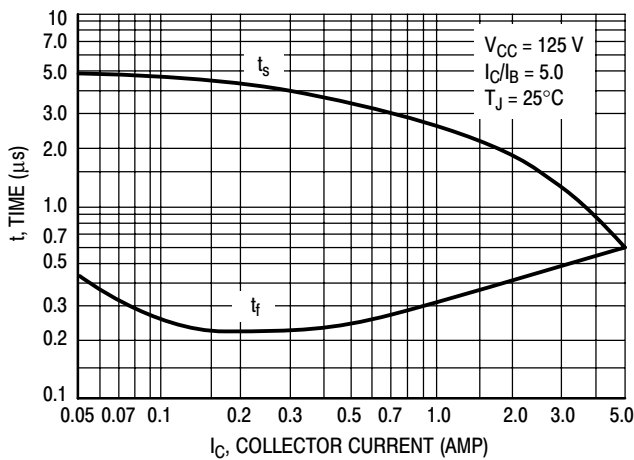


Figure 5. Turn-Off Time

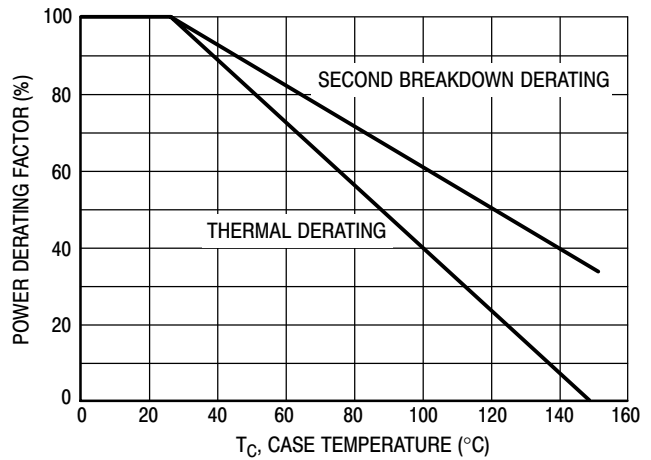


Figure 6. Power Derating

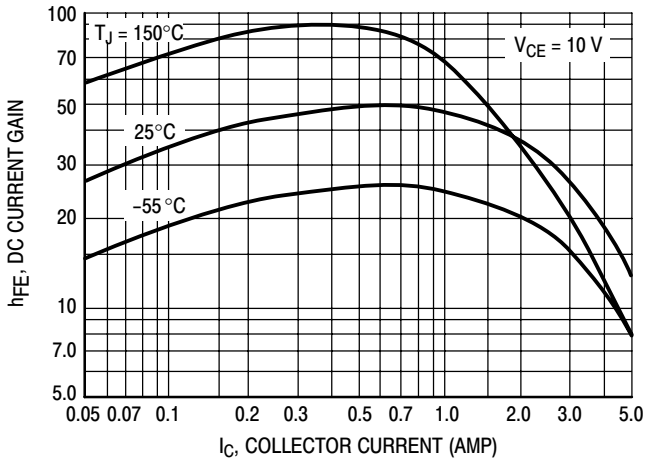


Figure 7. DC Current Gain

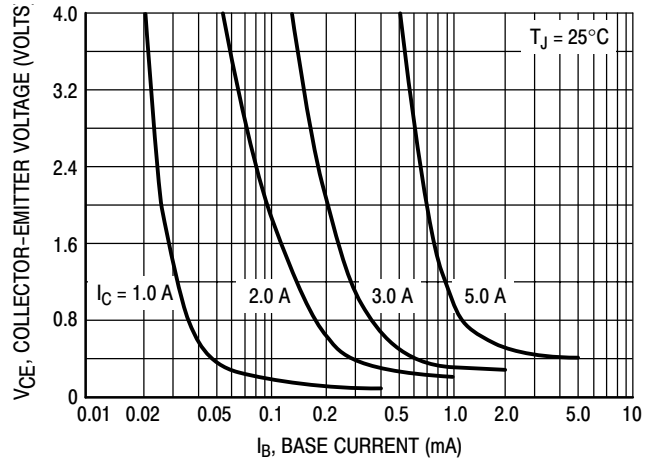


Figure 8. Collector Saturation Region

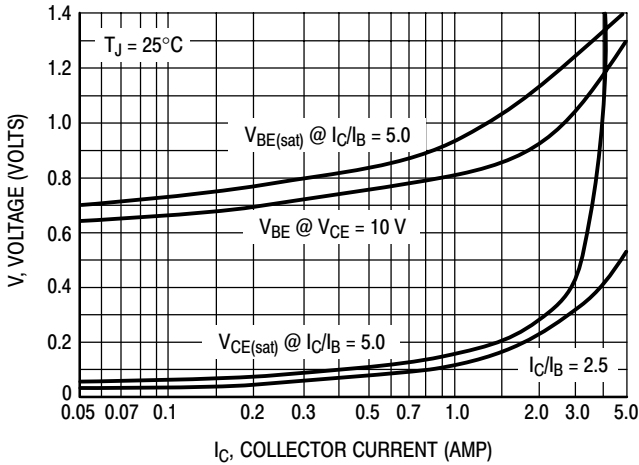


Figure 9. "On" Voltages

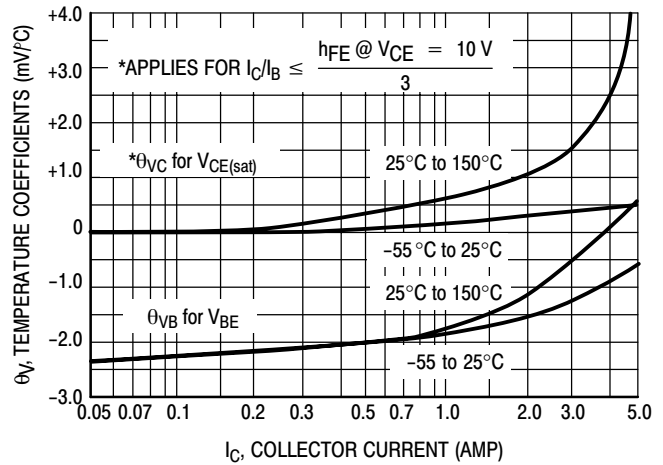


Figure 10. Temperature Coefficients

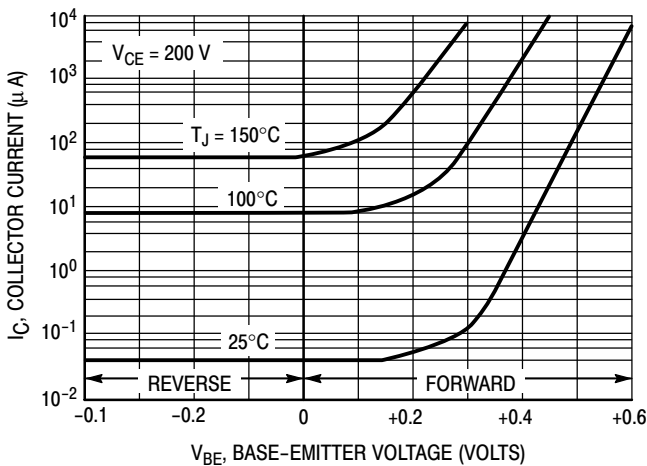


Figure 11. Collector Cutoff Region

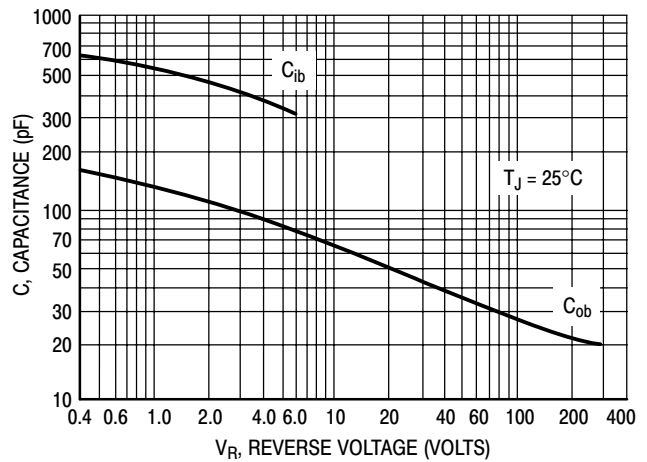
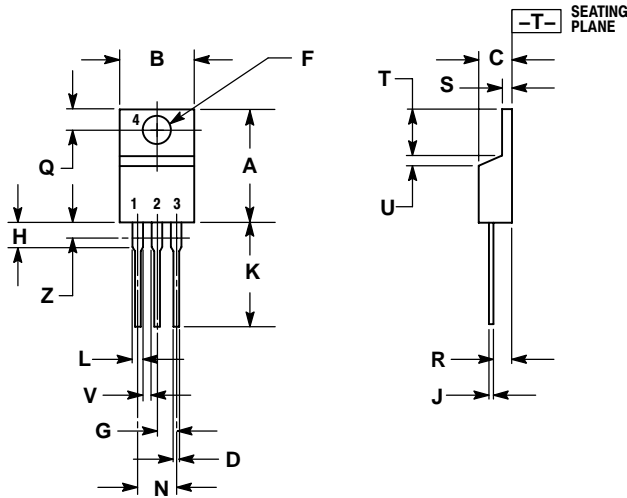


Figure 12. Capacitance

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PACKAGE DIMENSIONS

TO-220AB CASE 221A-09 ISSUE AD



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.570	0.620	14.48	15.75
B	0.380	0.405	9.66	10.28
C	0.160	0.190	4.07	4.82
D	0.025	0.035	0.64	0.88
F	0.142	0.147	3.61	3.73
G	0.095	0.105	2.42	2.66
H	0.110	0.155	2.80	3.93
J	0.018	0.025	0.46	0.64
K	0.500	0.562	12.70	14.27
L	0.045	0.060	1.15	1.52
N	0.190	0.210	4.83	5.33
Q	0.100	0.120	2.54	3.04
R	0.080	0.110	2.04	2.79
S	0.045	0.055	1.15	1.39
T	0.235	0.255	5.97	6.47
U	0.000	0.050	0.00	1.27
V	0.045	---	1.15	---
Z	---	0.080	---	2.04

STYLE 1:

- PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

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