



2K

X25C02

256 x 8 Bit

**SPI Serial E<sup>2</sup>PROM**

**FEATURES**

- 1MHz Clock Rate
- 256 X 8 Bits
  - 4 Byte Page Mode
- Low Power CMOS
  - 150µA Standby Current
  - 2mA Active Current
- 5V Power Supply
- Built-in Inadvertent Write Protection
  - Power-Up/Power-Down protection circuitry
  - Write Latch
  - Write Protect Pin
- Self-Timed Write Cycle
  - 5ms Write Cycle Time (Typical)
- High Reliability
  - Endurance: 100,000 cycles per byte
  - Data Retention: 100 Years
  - ESD protection: 2000V on all pins
- Available Packages
  - 8-Lead MSOP
  - 8-Lead PDIP
  - 8-Lead SOIC

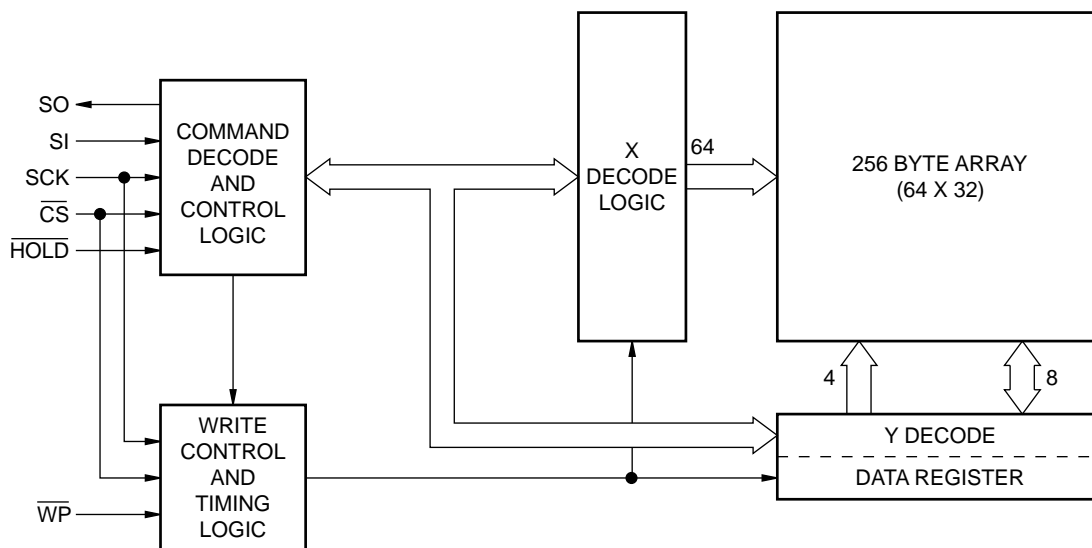
**DESCRIPTION**

The X25C02 is a CMOS 2048-bit serial E<sup>2</sup>PROM, internally organized as 256 x 8. The X25C02 features a serial interface and software protocol allowing operation on a simple three-wire bus. The bus signals are a clock input (SCK) plus separate data in (SI) and data out (SO) lines. Access to the device is controlled through a chip select ( $\overline{CS}$ ) input, allowing any number of devices to share the same bus.

The X25C02 also features two additional inputs that provide the end user with added flexibility. By asserting the  $\overline{HOLD}$  input, the X25C02 will ignore transitions on its inputs, thus allowing the host to service higher priority interrupts. The  $\overline{WP}$  input can be used as a hardwire input to the X25C02 disabling all write attempts, thus providing a mechanism for limiting end user capability of altering the memory.

The X25C02 utilizes Xicor's proprietary Direct Write™ cell, providing a minimum endurance of 100,000 cycles per byte and a minimum data retention of 100 years.

**FUNCTIONAL DIAGRAM**



3843 FHD F01

# X25C02

## PIN DESCRIPTIONS

### Serial Output (SO)

SO is a push/pull serial data output pin. During a read cycle, data is shifted out on this pin. Data is clocked out by the falling edge of the serial clock.

### Serial Input (SI)

SI is the serial data input pin. All data, opcodes, byte addresses, and data to be written to the memory are input on this pin. Data is latched by the rising edge of the serial clock.

### Serial Clock (SCK)

The Serial Clock controls the serial bus timing for data input and output. Opcodes, addresses, or data present on the SI pin are sampled or latched on the rising edge of the clock input, while data on the SO pin change after the falling edge of the clock input.

### Chip Select ( $\overline{CS}$ )

When  $\overline{CS}$  is HIGH, the X25C02 is deselected and the SO output pin is at HIGH impedance and unless an internal write operation is underway, the X25C02 will be

in the standby power mode.  $\overline{CS}$  LOW enables the X25C02, placing it in the active power mode. It should be noted that after power-up, a HIGH to LOW transition on  $\overline{CS}$  is required prior to the start of any operation.

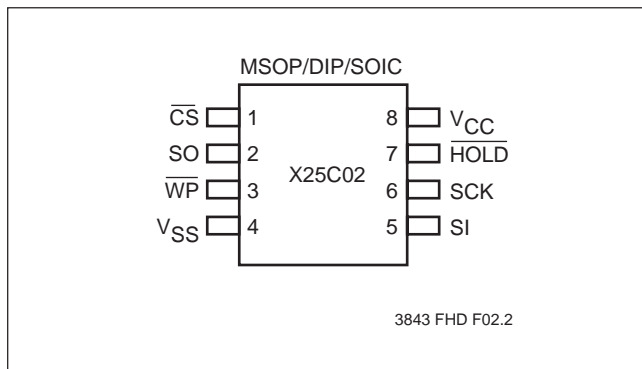
### Write Protect ( $\overline{WP}$ )

When  $\overline{WP}$  is LOW, nonvolatile writes to the X25C02 are disabled, but the part otherwise functions normally. When  $\overline{WP}$  is held HIGH, all functions, including nonvolatile writes operate normally.  $\overline{WP}$  going LOW while  $\overline{CS}$  is still LOW will interrupt a write to the X25C02. If the internal write cycle has already been initiated,  $\overline{WP}$  going LOW will have no affect on a write.

### Hold ( $\overline{HOLD}$ )

$\overline{HOLD}$  is used in conjunction with the  $\overline{CS}$  pin to select the device. Once the part is selected and a serial sequence is underway,  $\overline{HOLD}$  may be used to pause the serial communication with the controller without resetting the serial sequence. To pause,  $\overline{HOLD}$  must be brought LOW while SCK is LOW. To resume communication,  $\overline{HOLD}$  is brought HIGH, again while SCK is LOW. If the pause feature is not used,  $\overline{HOLD}$  should be held HIGH at all times.

## PIN CONFIGURATION



## PIN NAMES

Symbol	Description
$\overline{CS}$	Chip Select Input
SO	Serial Output
SI	Serial Input
SCK	Serial Clock Input
$\overline{WP}$	Write Protect Input
V <sub>SS</sub>	Ground
V <sub>CC</sub>	Supply Voltage
$\overline{HOLD}$	Hold Input

3843 PGM T01

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## PRINCIPLES OF OPERATION

The X25C02 is a 256 x 8 E<sup>2</sup>PROM designed to interface directly with the synchronous serial peripheral interface (SPI) of many popular microcontroller families.

The X25C02 contains an 8-bit instruction register. It is accessed via the SI input, with data being clocked in on the rising SCK.  $\overline{CS}$  must be LOW and the  $\overline{HOLD}$  and  $\overline{WP}$  inputs must be HIGH during the entire operation.

Table 1 contains a list of the instructions and their opcodes. All instructions, addresses and data are transferred MSB first.

Data input is sampled on the first rising edge of SCK after  $\overline{CS}$  goes LOW. SCK is static, allowing the user to stop

the clock and then resume operations. If the clock line is shared with other peripheral devices on the SPI bus, the user can assert the  $\overline{HOLD}$  input to place the X25C02 into a "PAUSE" condition. After releasing  $\overline{HOLD}$ , the X25C02 will resume operation from the point when  $\overline{HOLD}$  was first asserted.

### Write Enable (WREN) and Write Disable (WRDI)

The X25C02 contains a "write enable" latch. This latch must be SET before a write operation will be completed internally. The WREN instruction will set the latch and the WRDI instruction will reset the latch. This latch is automatically reset upon a power-up condition and after the completion of a byte or page write cycle. The latch is also reset if  $\overline{WP}$  is brought LOW.

**Table 1. Instruction Set**

Instruction Name	Instruction Format*	Operation
WREN	0000 0110	Set the Write Enable Latch (Enable Write Operations)
WRDI	0000 0100	Reset the Write Enable Latch (Disable Write Operations)
READ	0000 0011	Read Data from Memory Array beginning at selected address
WRITE	0000 0010	Write Data to Memory Array beginning at Selected Address (1 to 4 Bytes)

\*Instructions are shown MSB in leftmost position. Instructions are transferred MSB first.

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## DEVICE OPERATION

### Clock and Data Timing

Data input on the SI line is sampled and latched on the rising edge of SCK. Data is output on the SO line by the falling edge of SCK.

### Read Sequence

The  $\overline{CS}$  line is first pulled LOW to select the device. The 8-bit read opcode is transmitted to the X25C02, followed by the 8-bit address. After the READ opcode and byte address are sent, the data stored in the memory at the selected address is shifted out on the SO line. The data stored in memory at the next address can be read sequentially by continuing to provide clock pulses. The byte address is automatically incremented to the next higher address after each byte of data is shifted out. When the highest address is reached (\$FF) the address counter rolls over to address \$00 allowing the read cycle to be continued indefinitely. The read operation is terminated by taking  $\overline{CS}$  HIGH. Refer to the read operation sequence illustrated in Figure 1.

### Write Sequence

Prior to any attempt to write data into the X25C02, the “write enable” latch must first be set by issuing the WREN instruction (See Fig. 2).  $\overline{CS}$  is first taken LOW, then the instruction is clocked into the X25C02. After all eight bits of the instruction are transmitted,  $\overline{CS}$  must then be taken HIGH. If the user continues the write operation without taking  $\overline{CS}$  HIGH after issuing the WREN instruction, the write operation will be ignored.

Once the “write enable” latch is set, the user may proceed by issuing the write instruction, followed by the address and then the data to be written. This is minimally a twenty-four clock operation.  $\overline{CS}$  must go LOW and remain LOW for the duration of the operation. The host may continue to write up to four bytes of data to the X25C02. The only restriction is the four bytes must reside on the same page. A page address begins with address XXXX XX00 and ends with XXXX XX11. If the byte address counter reaches XXXX XX11 and the clock continues the counter will “roll over” to the first address of the page and overwrite any data that may have been written.

For the write operation (byte or page write) to be completed,  $\overline{CS}$  can only be brought HIGH after the twenty-fourth, thirty-second, fortieth or forty-eighth clock. If it is brought HIGH at any other time, the write operation will not be completed. Refer to Figure 4 for a detailed illustration of the page write sequence and time frames in which  $\overline{CS}$  going HIGH are valid.

### Hold Operation

The  $\overline{HOLD}$  input should be HIGH (at  $V_{IH}$ ) under normal operation. If a data transfer is to be interrupted  $\overline{HOLD}$  can be pulled LOW to suspend the transfer until it can be resumed. The only restriction is the SCK input must be LOW when  $\overline{HOLD}$  is first pulled low and SCK must also be LOW when  $\overline{HOLD}$  is released.

The  $\overline{HOLD}$  input may be tied HIGH either directly to  $V_{CC}$  or tied to  $V_{CC}$  through a resistor.

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## Operational Notes

The X25C02 powers-up in the following state:

- The device is in the low power standby state.
- A HIGH to LOW transition on  $\overline{CS}$  is required to enter an active state and receive an instruction.
- SO pin is high impedance.
- The “write enable” latch is reset.

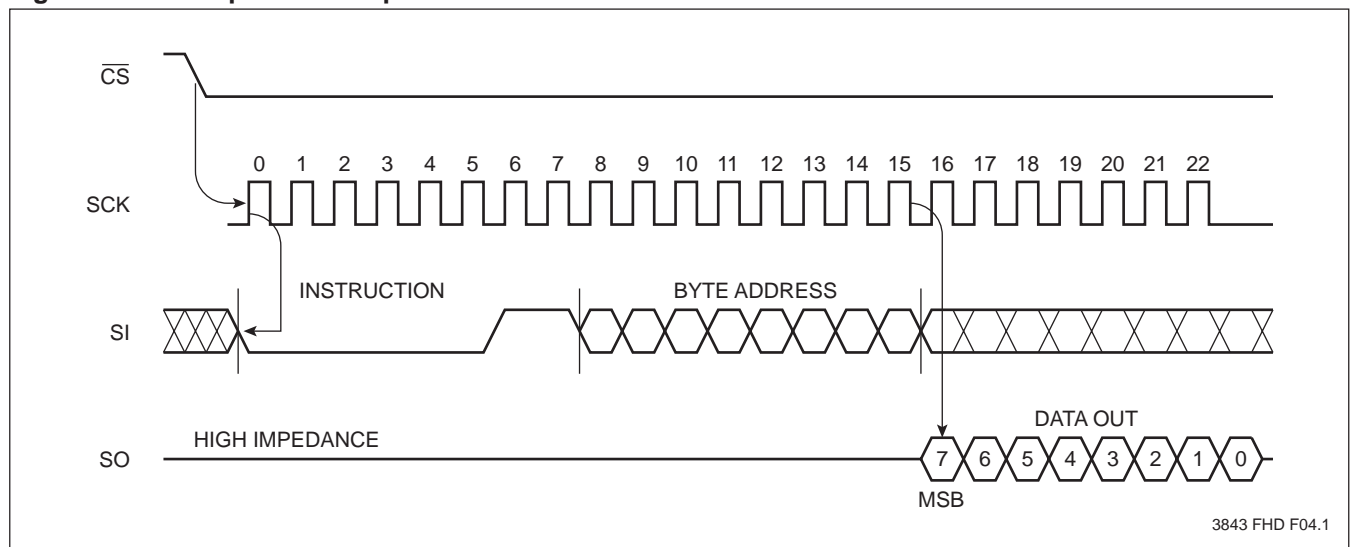
## Data Protection

The following circuitry has been included to prevent inadvertent writes:

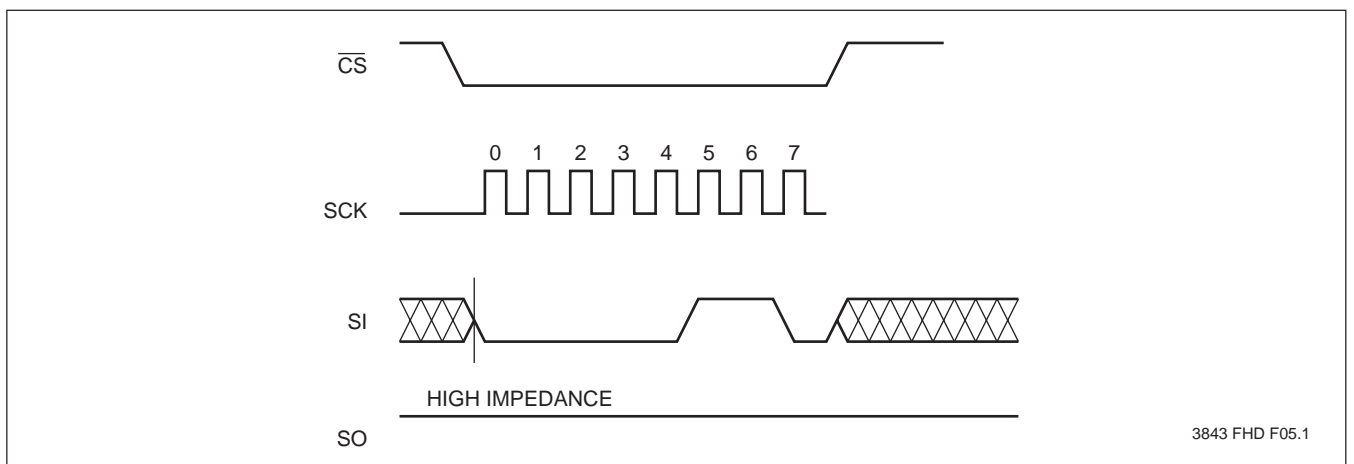
- The “write enable” latch is reset upon power-up.
- A WREN instruction must be issued to set the “write enable” latch.
- $\overline{CS}$  must come HIGH at the proper clock count in order to start a write cycle.

The “write enable” latch is reset when  $\overline{WP}$  is brought LOW.

**Figure 1. Read Operation Sequence**

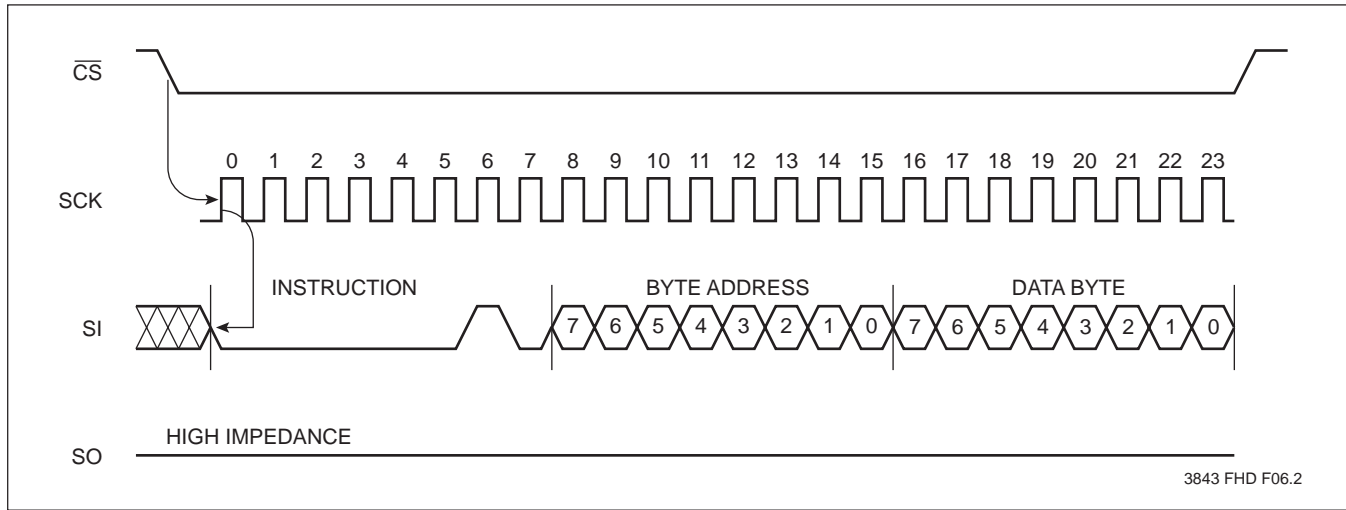


**Figure 2. Set Write Enable Latch Sequence**

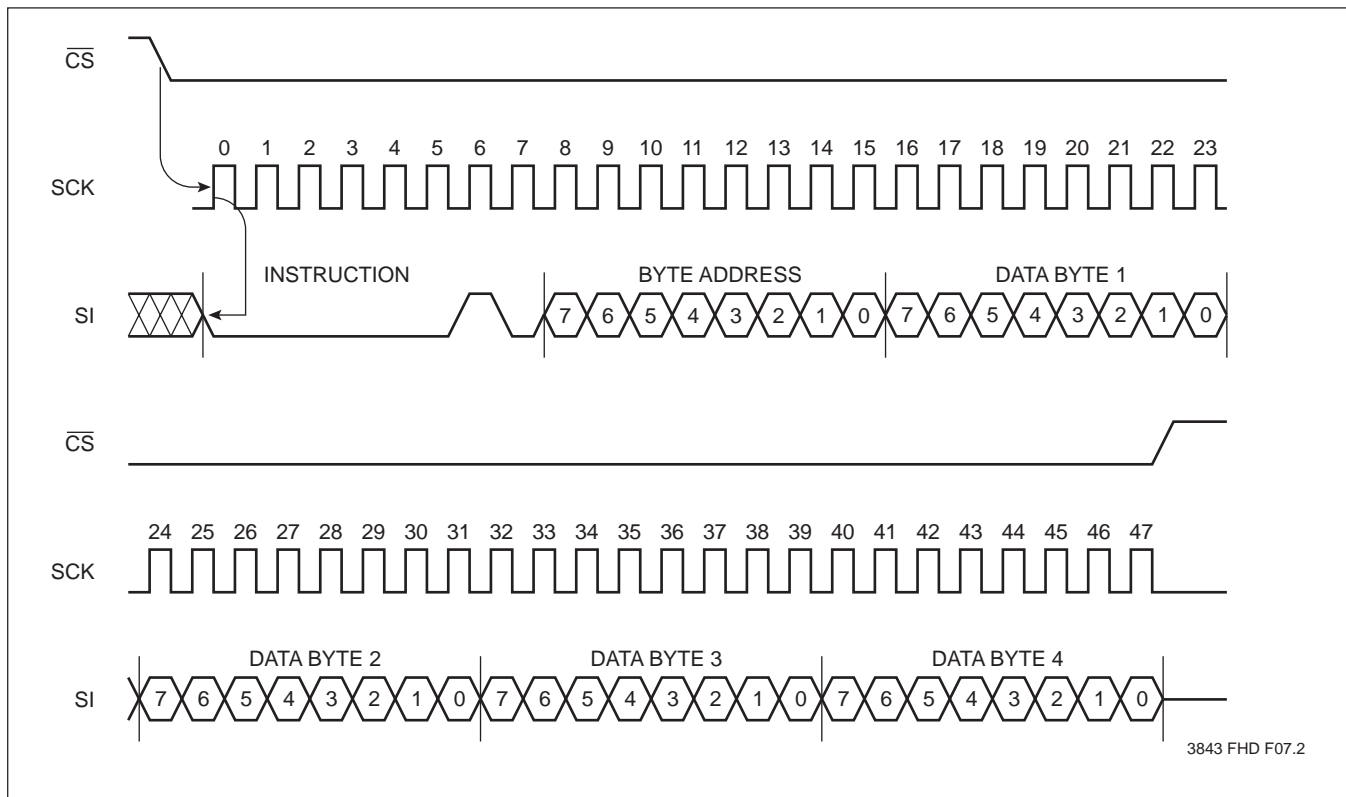


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**Figure 3. Byte Write Operation Sequence**



**Figure 4. Page Write Operation Sequence**



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## ABSOLUTE MAXIMUM RATINGS\*

Temperature under Bias .....	-65°C to +135°C
Storage Temperature .....	-65°C to +150°C
Voltage on any Pin with Respect to V <sub>SS</sub> .....	-1V to +7V
D.C. Output Current .....	5mA
Lead Temperature (Soldering, 10 seconds) .....	300°C

## \*COMMENT

Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and the functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## RECOMMENDED OPERATING CONDITIONS

Temp	Min.	Max.
Commercial	0°C	+70°C
Industrial	-40°C	+85°C
Military	-55°C	+125°C

3843 PGM T03.1

Supply Voltage	Limits
X25C02	5V ±10%

3843 PGM T04.1

## D.C. OPERATING CHARACTERISTICS (Over the recommended operating conditions unless otherwise specified.)

Symbol	Parameter	Limits		Units	Test Conditions
		Min.	Max.		
I <sub>CC</sub>	V <sub>CC</sub> Supply Current (Active)		2	mA	SCK = V <sub>CC</sub> × 0.1/V <sub>CC</sub> × 0.9 @ 1MHz, SO = Open
I <sub>SB</sub>	V <sub>CC</sub> Supply Current (Standby)		150	µA	$\overline{CS} = V_{CC}$ , V <sub>IN</sub> = V <sub>SS</sub> or V <sub>CC</sub> - 0.3V
I <sub>LI</sub>	Input Leakage Current		10	µA	V <sub>IN</sub> = V <sub>SS</sub> to V <sub>CC</sub>
I <sub>LO</sub>	Output Leakage Current		10	µA	V <sub>OUT</sub> = V <sub>SS</sub> to V <sub>CC</sub>
V <sub>IL</sub> <sup>(1)</sup>	Input LOW Voltage	-1	V <sub>CC</sub> × 0.3	V	
V <sub>IH</sub> <sup>(1)</sup>	Input HIGH Voltage	V <sub>CC</sub> × 0.7	V <sub>CC</sub> + 0.5	V	
V <sub>OL</sub>	Output LOW Voltage		0.4	V	I <sub>OL</sub> = 2mA
V <sub>OH</sub>	Output HIGH Voltage	V <sub>CC</sub> -0.8		V	I <sub>OH</sub> = -1mA

3843 PGM T05.3

## POWER-UP TIMING

Symbol	Parameter	Min.	Max.	Units
t <sub>PUR</sub> <sup>(1)</sup>	Power-up to Read Operation		1	ms
t <sub>PUW</sub> <sup>(1)</sup>	Power-up to Write Operation		5	ms

3843 PGM T09

## CAPACITANCE T<sub>A</sub> = +25°C, f = 1MHz, V<sub>CC</sub> = 5V.

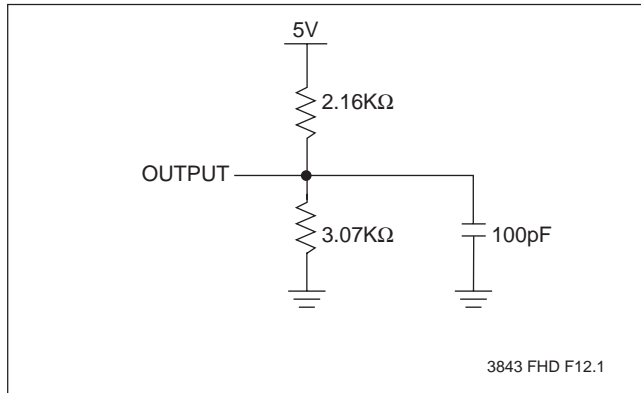
Symbol	Test	Max.	Units	Conditions
C <sub>OUT</sub> <sup>(2)</sup>	Output Capacitance (SO)	8	pF	V <sub>OUT</sub> = 0V
C <sub>IN</sub> <sup>(2)</sup>	Input Capacitance (SCK, SI, $\overline{CS}$ , $\overline{WP}$ , HOLD)	6	pF	V <sub>IN</sub> = 0V

3843 PGM T06.1

- Notes:** (1) V<sub>IL</sub> min. and V<sub>IH</sub> max. are for reference only and are not tested.  
 (2) This parameter is periodically sampled and not 100% tested.

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## EQUIVALENT A.C. LOAD CIRCUIT



## A.C. TEST CONDITIONS

Input Pulse Levels	$V_{CC} \times 0.1$ to $V_{CC} \times 0.9$
Input Rise and Fall Times	10ns
Input and Output Timing Level	$V_{CC} \times 0.5$

3843 PGM T07

## A.C. CHARACTERISTICS (Over recommended operating conditions, unless otherwise specified)

### Data Input Timing

Symbol	Parameter	Min.	Max.	Units
f <sub>SCK</sub>	Clock Frequency	0	1	MHz
t <sub>CYC</sub>	Cycle Time	1000		ns
t <sub>LEAD</sub>	$\overline{CS}$ Lead Time	500		ns
t <sub>LAG</sub>	$\overline{CS}$ Lag Time	500		ns
t <sub>WH</sub>	Clock HIGH Time	400		ns
t <sub>WL</sub>	Clock LOW Time	400		ns
t <sub>SU</sub>	Data Setup Time	100		ns
t <sub>H</sub>	Data Hold Time	100		ns
t <sub>RI</sub>	Data In Rise Time		2	μs
t <sub>FI</sub>	Data In Fall Time		2	μs
t <sub>HD</sub>	$\overline{HOLD}$ Setup Time	200		ns
t <sub>CD</sub>	$\overline{HOLD}$ Hold Time	200		ns
t <sub>CS</sub>	$\overline{CS}$ Deselect Time	500		ns
t <sub>WC</sub> <sup>(3)</sup>	Write Cycle Time		10	ms

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### Data Output Timing

Symbol	Parameter	Min.	Max.	Units
f <sub>SCK</sub>	Clock Frequency	0	1	MHz
t <sub>DIS</sub>	Output Disable Time		500	ns
t <sub>v</sub>	Output Valid from clock Low		400	ns
t <sub>HO</sub>	Output Hold Time	0		ns
t <sub>RO</sub> <sup>(1)</sup>	Output Rise Time		300	ns
t <sub>FO</sub> <sup>(1)</sup>	Output Fall Time		300	ns
t <sub>LZ</sub>	$\overline{HOLD}$ HIGH to Output in Low Z	100		ns
t <sub>HZ</sub>	$\overline{HOLD}$ LOW to Output in High Z	100		ns

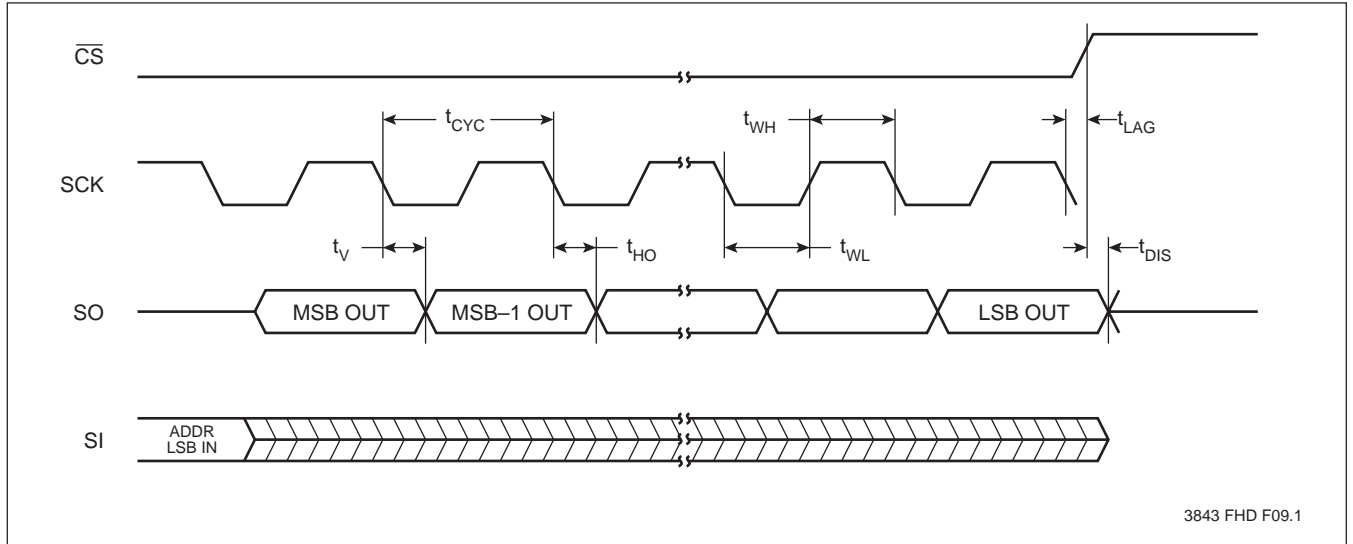
3843 PGM T09.1

**Notes:** (3) t<sub>WC</sub> is the time from the rising edge of  $\overline{CS}$  after a valid write sequence has been sent to the end of the self-timed internal nonvolatile write cycle.

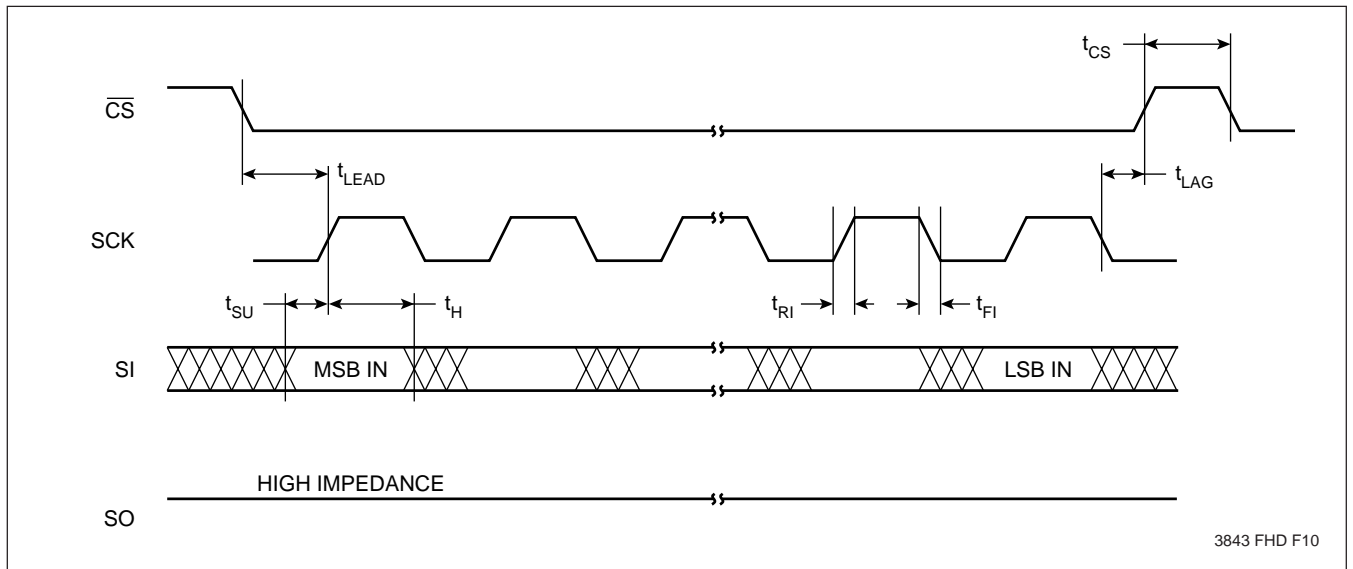


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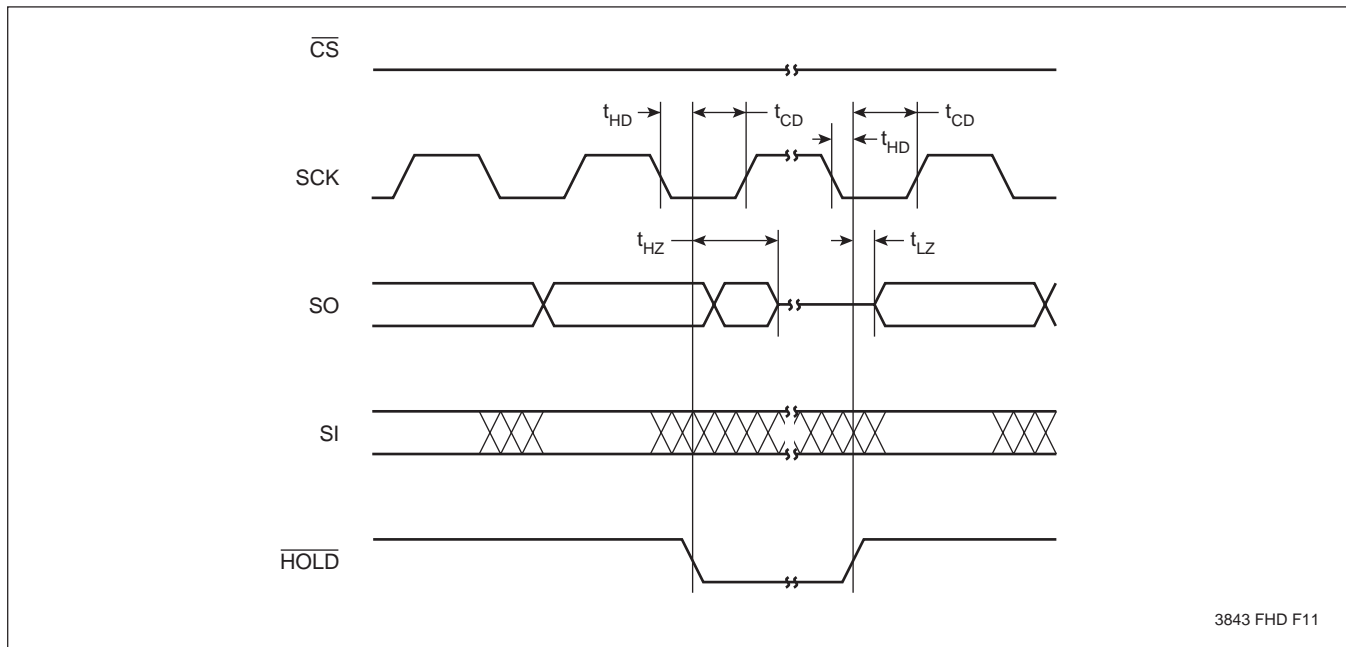
## Serial Output Timing



## Serial Input Timing



# X25C02



3843 FHD F11

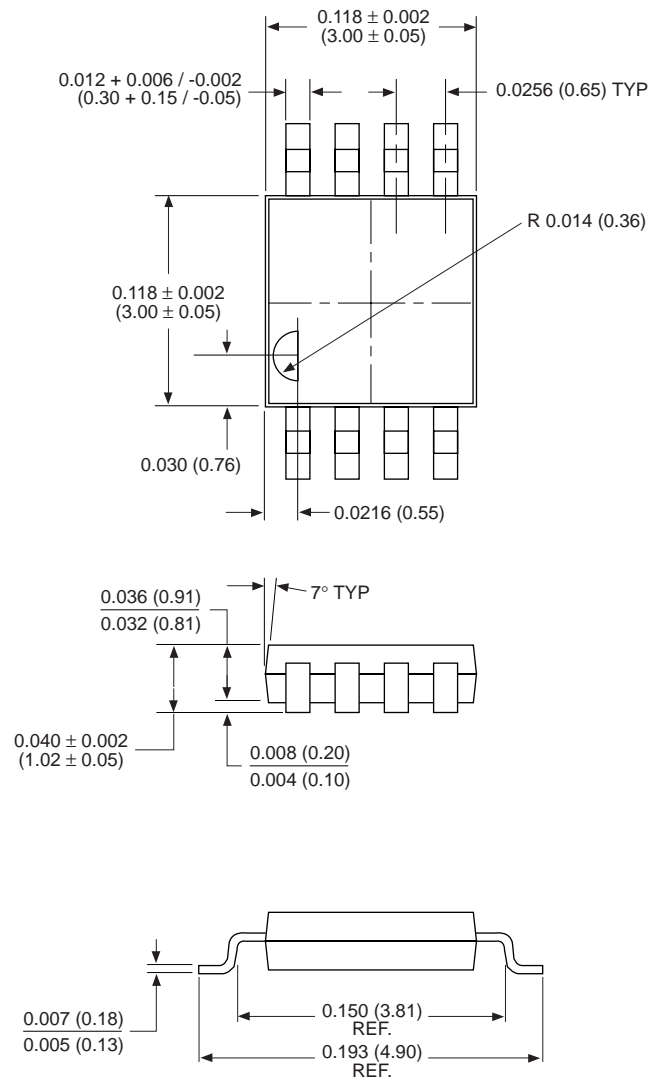
## SYMBOL TABLE

WAVEFORM	INPUTS	OUTPUTS
	Must be steady	Will be steady
	May change from LOW to HIGH	Will change from LOW to HIGH
	May change from HIGH to LOW	Will change from HIGH to LOW
	Don't Care: Changes Allowed	Changing: State Not Known
	N/A	Center Line is High Impedance

# X25C02

## PACKAGING INFORMATION

### 8-LEAD MINIATURE SMALL OUTLINE GULL WING PACKAGE TYPE M



**NOTE:**

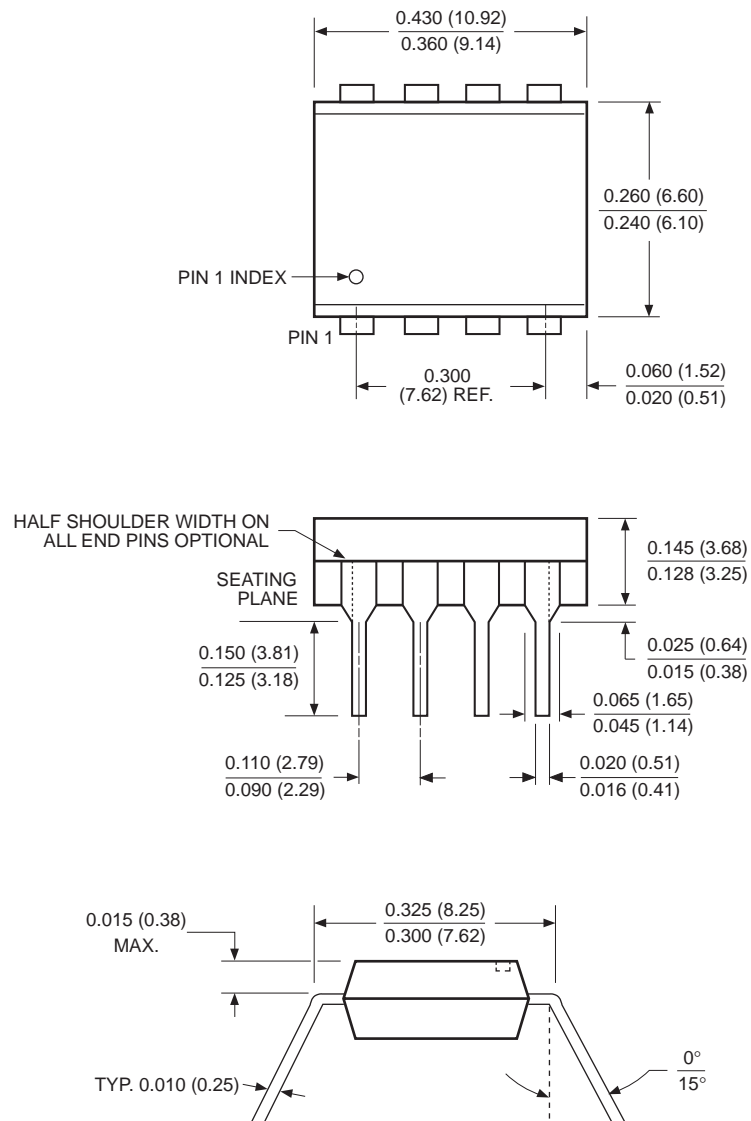
1. ALL DIMENSIONS IN INCHES AND (MILLIMETERS)

3926 ILL F49

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## PACKAGING INFORMATION

### 8-LEAD PLASTIC DUAL IN-LINE PACKAGE TYPE P



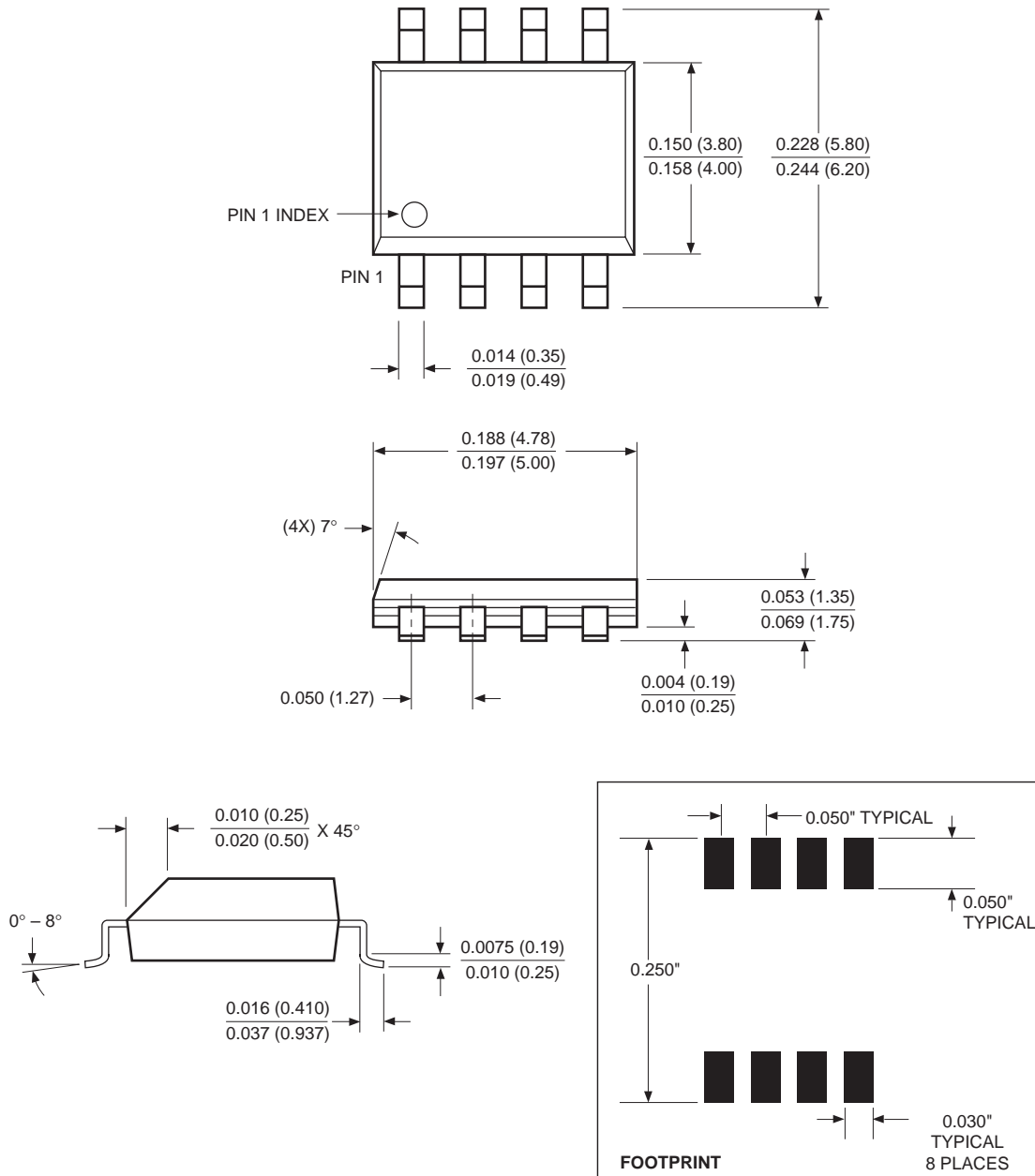
**NOTE:**

1. ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)
2. PACKAGE DIMENSIONS EXCLUDE MOLDING FLASH

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## PACKAGING INFORMATION

### 8-LEAD PLASTIC SMALL OUTLINE GULL WING PACKAGE TYPE S

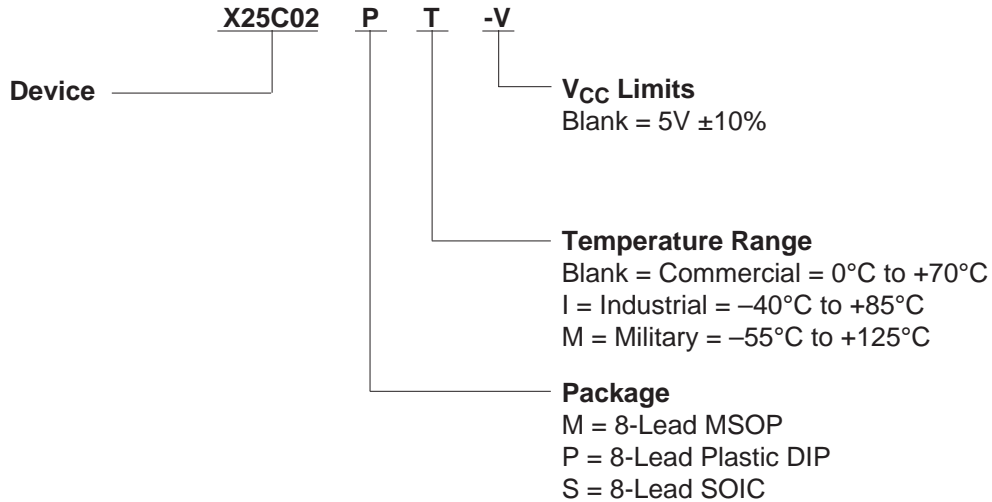


NOTE: ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)

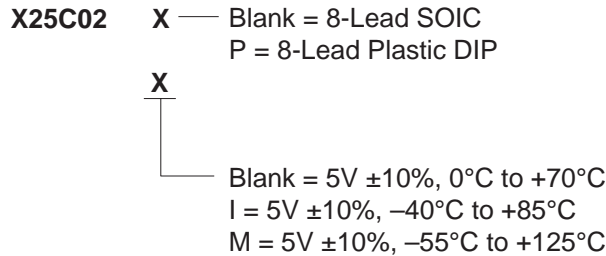
# X25C02

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## ORDERING INFORMATION



## Part Mark Convention



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## LIMITED WARRANTY

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Xicor products are covered by one or more of the following U.S. Patents: 4,263,664; 4,274,012; 4,300,212; 4,314,265; 4,326,134; 4,393,481; 4,404,475; 4,450,402; 4,486,769; 4,488,060; 4,520,461; 4,533,846; 4,599,706; 4,617,652; 4,668,932; 4,752,912; 4,829, 482; 4,874, 967; 4,883, 976. Foreign patents and additional patents pending.

## LIFE RELATED POLICY

In situations where semiconductor component failure may endanger life, system designers using this product should design the system with appropriate error detection and correction, redundancy and back-up features to prevent such an occurrence.

Xicor's products are not authorized for use in critical components in life support devices or systems.

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform, when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.