12-BIT 30 MSPS DUAL CHANNEL CCD SIGNAL FRONT END FOR DIGITAL COPIER

FEATURES

- **Dual Channel CCD Signal Processing:**
  - **Correlated Double Sampler (CDS)**
  - **Sample Hold Mode**
  - **Digital Programmable Amplifier**
  - **CCD Offset Correction (OB loop)**
- **High Performance A/D:**
  - **12-Bit Resolution**
  - **INL: ±2 LSB**
  - **DNL: ±0.5 LSB**
  - **No Missing Codes**
- **High-Speed Operation**
  - **Sample Rate: 30 MHz (Minimum)**
- **78-dB Signal-To-Noise Ratio (at 0-dB Gain)**
- **Low Power Consumption:**
  - **Low Voltage: 3 V to 3.6 V**
  - **Low Power: 290 mW (Typ) at 3.3 V**
  - **Standby Mode: 20 mW (Typ)**

APPLICATIONS

- **Copiers**
- **Scanners**
- **Facsimiles**

DESCRIPTION

The VSP5000 device is a complete application specific standard product (ASSP) for charge-coupled device (CCD) line sensor applications such as copiers, scanners, and facsimiles. The VSP5000 device provides two independent channels of processing lines and performs analog front-end processing and analog-to-digital (A/D) conversion. Each channel has a correlated double sampler (CDS)/sample hold (SH) circuit, a 14-bit analog-to-digital converter (ADC), a digital programmable gain amplifier (DPGA), and an optical black (OB) correction loop. Data output is 12 bits in length and the 2-channel A/D data is multiplexed and output.

The VSP5000 is available in a 64-lead LQFP package and operates from a single 3.3-V supply.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ORDERING INFORMATION

PRODUCT	PACKAGE	PACKAGE OUTLINE DESIGNATOR(1)	SPECIFIED TEMPERATURE RANGE	PACKAGE MARKING	ORDERING NUMBER	TRANSPORT MEDIA
VSP5000	64-Lead LQFP	PM	–25°C to 85°C	VSP5000PM	VSP5000PM	Tray
					VSP5000PMR	Tape and reel

(1) A detailed drawing and a dimension table are located at the end of the data sheet.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range unless otherwise noted(1)

	UNITS
Supply voltage, V_{CC}, V_{DD}	4 V
Supply voltage differences, among V_{CC} terminals	±0.1 V
Ground voltage differences, AGND, DGND	±0.1 V
Digital input voltage	–0.3 V to V_{DD} + 0.3 V
Analog input voltage	–0.3 V to V_{CC} + 0.3 V
Input current (any leads except supplies)	±10 mA
Ambient temperature under bias	–40°C to 125°C
Storage temperature	–55°C to 150°C
Junction temperature	150°C
Lead temperature (soldering, 5 sec)	260°C
Package temperature (IR reflow, peak)	250°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

all specifications at T_A = 25°C, all power supply voltages = 3.3 V, and conversion rate (f_{ADCCK}) = 30 MHz (unless otherwise noted)

PARAMETER		TEST CONDITIONS	VSP5000			UNIT
			MIN	TYP	MAX	
Resolution				12		Bits
Signal pass				2		ch
Maximum conversion rate			30			MHz
DIGITAL INPUTS						
V_{T+}	Input low-to-high threshold voltage			1.8		V
V_{T-}	Input high-to-low threshold voltage			1.1		V
I_{IH}	Input logic high current	V_I = 3 V			±20	µA
I_{IL}	Input logic low current	V_I = 0 V			±20	µA
	Input limit		–0.3		V_{CC}+0.3	
	SYSCLK clock duty cycle			50%		
	Input capacitance			5		pF
DIGITAL OUTPUTS (even and odd channels)						
	Logic coding			Straight binary		
	Multiplex frequency		60			MHz
V_{OH}	Output logic high voltage	I_{OH} = –2 mA	2.5			V
V_{OL}	Output logic low voltage	I_{OL} = 2 mA			0.4	V

ELECTRICAL CHARACTERISTICS (CONTINUED)

all specifications at T_A = 25°C, all power supply voltages = 3.3 V, and conversion rate (f_{ADCCK}) = 30 MHz (unless otherwise noted)

PARAMETER		TEST CONDITIONS	VSP5000			UNIT
			MIN	TYP	MAX	
ANALOG INPUT (CCDIN)						
	Input signal level for full-scale output	DPGA gain = 0 dB	1400			mV
	Allowable feed-through level			1		V
	Input capacitance			15		pF
	Input limit		–0.3		3.3	V
TRANSFER CHARACTERISTICS						
DNL	Differential nonlinearity	CDS mode, DPGA gain = 0 dB		±0.5	±1	LSB
		SH mode, DPGA gain = 0 dB		±0.5	±1	LSB
INL	Integral nonlinearity	CDS mode, DPGA gain = 0 dB		±2	±4	LSB
		SH mode, DPGA gain = 0 dB		±4		LSB
	No missing codes	DPGA gain = 0 dB		Assured		
	Step input settling time	Full-scale step input		1		pixel
	Overload recovery time	Step input from 2 V to 0 V		2		pixels
	Data latency			9 (fixed)		Clock Cycles
	Signal-to-noise ratio(1)	DPGA gain = 0 dB		78		dB
		DPGA gain = 24 dB		54		
	Channel mismatch				±3%	
CORRELATED DOUBLE SAMPLER (CDS)						
	Reference level sample settling time	Within 1 LSB, driver impedance = 50 Ω		8.3		ns
	Data level sample settling time	Within 1 LSB, driver impedance = 50 Ω		8.3		ns
INPUT CLAMP						
	Clamp-on resistance			400		Ω
	Clamp level			1.5		V
OPTICAL BLACK CLAMP LOOP						
	CCD offset correction range		–300		300	mV
	DAC resolution			10		Bits
	Minimum DAC output current	COB pin		±0.15		µA
	Maximum DAC output current	COB pin		±153		µA
	Loop time constant	C_{COB} = 0.1 µF		40.7		µs
	Slew rate	C_{COB} = 0.1 µF, at current DAC full scale output		1530		V/s
	Optical black clamp level	Program range	0		510	LSB
		OB clamp code = 0101 0000		160		
REFERENCE						
	Positive reference voltage			1.85		V
	Negative reference voltage			1.1		V
DIGITAL PROGRAMMABLE GAIN AMPLIFIER (DPGA)						
	Gain program resolution			10		Bits
	Gain	Gain code = 11 1111 1111 24 dB		16		V/V
		Gain code = 10 0000 0000 18 dB		8		
		Gain code = 00 0100 0000 0 dB		1		
		Gain code = 00 0000 0000 –		0		
	Gain error			±0.5		dB

(1) SNR = 20 log (16384 / output rms noise in LSB), input connected to ground through a capacitor.

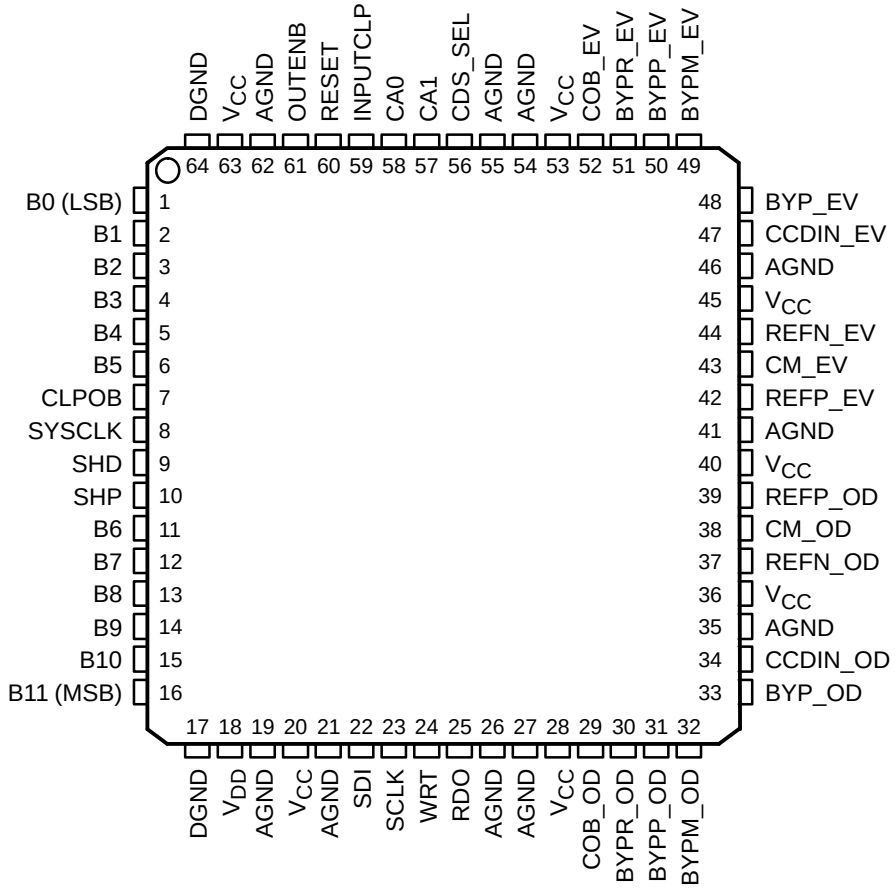
ELECTRICAL CHARACTERISTICS (CONTINUED)

all specifications at T_A = 25°C, all power supply voltages = 3.3 V, and conversion rate (f_{ADCCK}) = 30 MHz (unless otherwise noted)

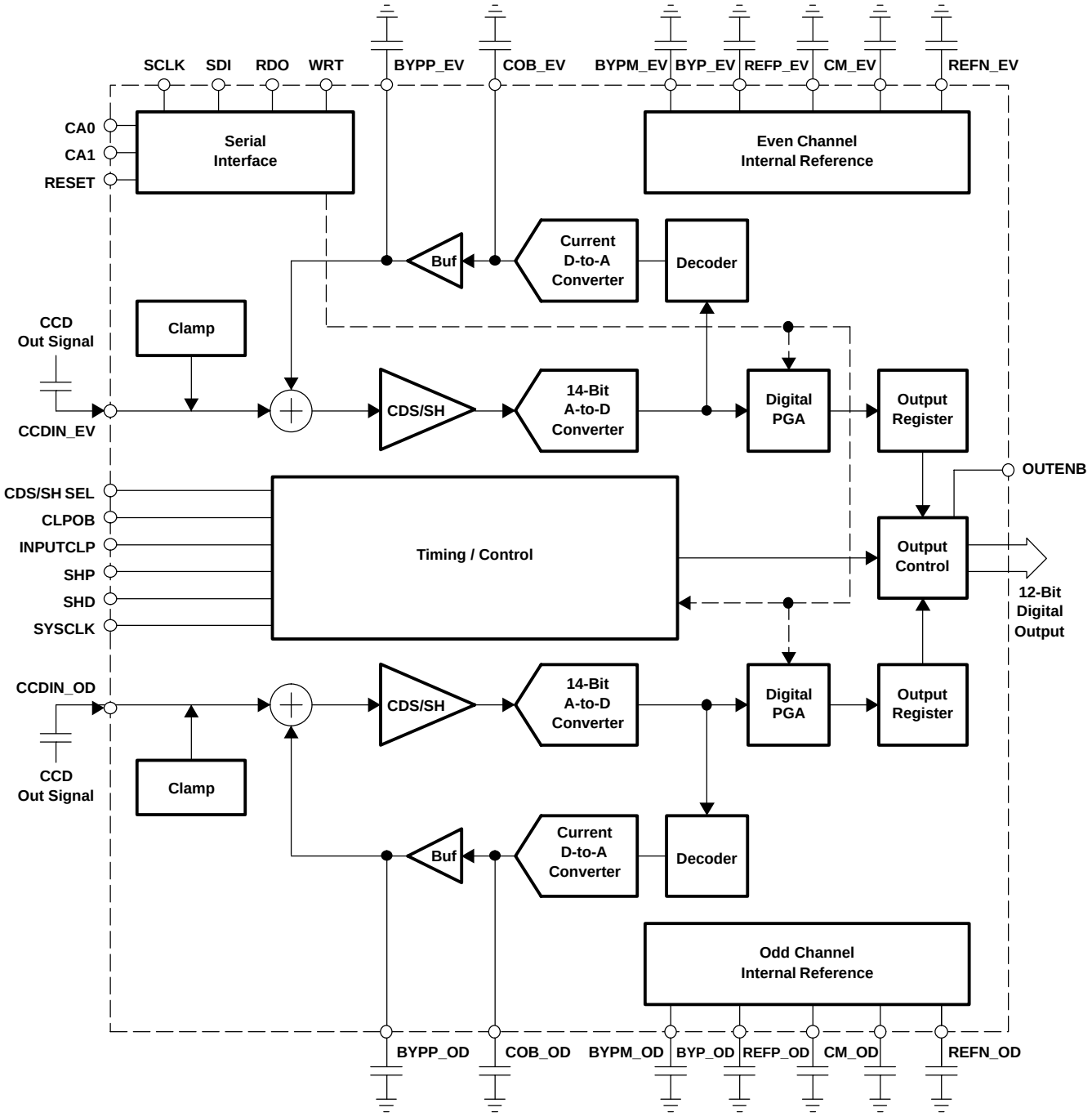
PARAMETER		TEST CONDITIONS	VSP5000			UNIT
			MIN	TYP	MAX	
SERIAL INTERFACE						
	Data length	Chip address: 2 bits Register address: 4 bits Data: 10 bits		2		byte
	Serial clock frequency				10	MHz
POWER SUPPLY						
V_{CC} , V_{DD}	Supply voltage		3	3.3	3.6	V
	Power dissipation	V_{CC} = V_{DD} = 3.3 V, f_{SYSCLK} = 30 MHz, Load = 10 pF		290		mW
		Stand-by mode		20		
TEMPERATURE RANGE						
	Operating temperature		–25		85	°C
	Storage temperature		–55		125	°C
θ_{JA}	Thermal resistance	64-lead LQFP		83		°C/W

PIN ASSIGNMENTS

PM PACKAGE
(TOP VIEW)



FUNCTIONAL BLOCK DIAGRAM



Terminal Functions

TERMINAL NO.	TERMINAL NAME	TYPE(1)	DESCRIPTION
1	B0 (LSB)	DO	A/D converter output, bit 0 (LSB)
2	B1	DO	A/D converter output, bit 1
3	B2	DO	A/D converter output, bit 2
4	B3	DO	A/D converter output, bit 3
5	B4	DO	A/D converter output, bit 4
6	B5	DO	A/D converter output, bit 5
7	CLPOB	DI	Optical black clamp pulse
8	SYSCLK	DI	System clock input
9	SHD	DI	CCD data sampling pulse
10	SHP	DI	CCD reference sampling pulse
11	B6	DO	A/D converter output, bit 6
12	B7	DO	A/D converter output, bit 7
13	B8	DO	A/D converter output, bit 8
14	B9	DO	A/D converter output, bit 9
15	B10	DO	A/D converter output, bit 10
16	B11 (MSB)	DO	A/D converter output, bit 11 (MSB)
17	DGND	P	Digital ground for digital outputs (B0–B11)
18	V_{DD}	P	Digital power supply for digital outputs (B0–B11)
19	AGND	P	Analog ground
20	V_{CC}	P	Analog power supply
21	AGND	P	Analog ground
22	SDI	DI	Serial interface data input
23	SCLK	DI	Serial interface data shift clock (triggered at the rising edge)
24	WRT	DI	Serial interface data write pulse (triggered at the rising edge)
25	RDO	DO	Serial interface register read output
26	AGND	P	Analog ground
27	AGND	P	Analog ground
28	V_{CC}	P	Analog power supply
29	COB_OD	AO	Optical black loop output voltage (odd), connect a 0.1-μF capacitor from terminal to ground
30	BYPR_OD	AO	Input buffer reference bypass (odd)
31	BYPP_OD	AO	CDS positive reference bypass (odd), leave open or bypass to ground through a 0.1-μF capacitor
32	BYPM_OD	AO	CDS negative reference bypass (odd), leave open or bypass to ground through a 0.1-μF capacitor
33	BYP_OD	AO	CDS common reference bypass (odd), bypass to ground through a 0.1-μF capacitor
34	CCDIN_OD	AI	CCD signal input (odd)
35	AGND	P	Analog ground
36	V_{CC}	P	Analog power supply
37	REFN_OD	AO	A/D converter negative reference bypass (odd), bypass to ground through a 0.1-μF capacitor
38	CM_OD	AO	A/D converter common reference bypass (odd), bypass to ground through a 0.1-μF capacitor
39	REFP_OD	AO	A/D converter positive reference bypass (odd), bypass to ground through a 0.1-μF capacitor
40	V_{CC}	P	Analog power supply
41	AGND	P	Analog ground

(1) Designators in TYPE: P: power supply and ground, DI: digital input, DO: digital output, AI: analog input, AO: analog output

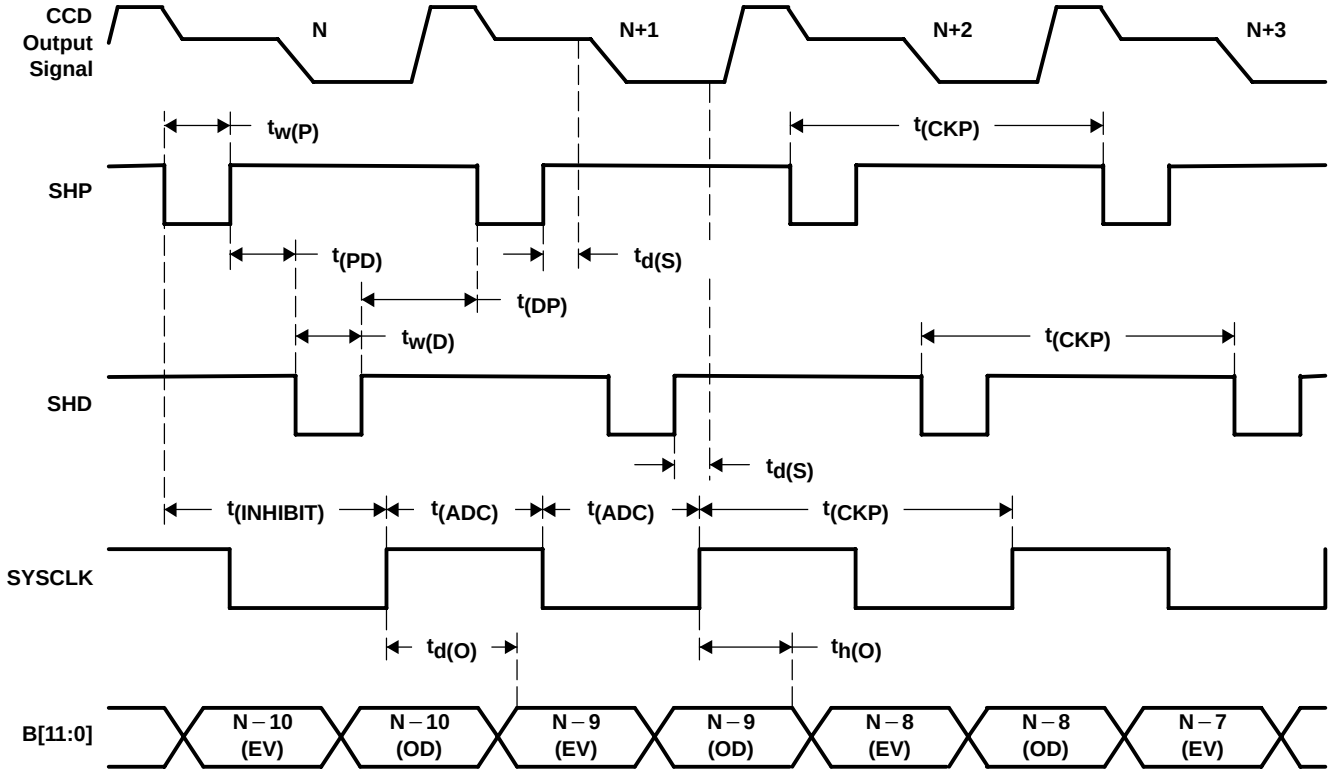
Terminal Functions (Continued)

TERMINAL NO.	TERMINAL NAME	TYPE(1)	DESCRIPTION
42	REFP_EV	AO	A/D converter positive reference bypass (even), bypass to ground through a 0.1-μF capacitor
43	CM_EV	AO	A/D converter common reference bypass (even), bypass to ground through a 0.1-μF capacitor
44	REFN_EV	AO	A/D converter negative reference bypass (even), bypass to ground through a 0.1-μF capacitor
45	V_{CC}	P	Analog power supply
46	AGND	P	Analog ground
47	CCDIN_EV	AI	CCD signal input (even)
48	BYP_EV	AO	CDS common reference bypass (even), bypass to ground through a 0.1-μF capacitor
49	BYPM_EV	AO	CDS negative reference bypass (even), bypass to ground through a 0.1-μF capacitor
50	BYPP_EV	AO	CDS positive reference bypass (even), bypass to ground through a 0.1-μF capacitor
51	BYPR_EV	AO	Input buffer reference bypass (even), bypass to ground through a 0.1-μF capacitor
52	COB_EV	AO	Optical black loop output voltage (even), connect a 0.1-μF capacitor from terminal to ground
53	V_{CC}	P	Analog power supply
54	AGND	P	Analog ground
55	AGND	P	Analog ground
56	CDS_SEL	DI	CDS/SH mode select: High = CDS mode Low = SH mode
57	CA1	DI	Chip address 1
58	CA0	DI	Chip address 0
59	INPUTCLP	DI	Input clamp control (active low)
60	RESET	DI	Asynchronous register reset (active low)
61	OUTENB	DI	Outputenable/disable: High = High impedance Low = Output enable
62	AGND	P	Analog ground
63	V_{CC}	P	Analog power supply
64	DGND	P	Digital ground for digital outputs (B0–B11)

(2) Designators in TYPE: P: power supply and ground, DI: digital input, DO: digital output, AI: analog input, AO: analog output

TIMING SPECIFICATION

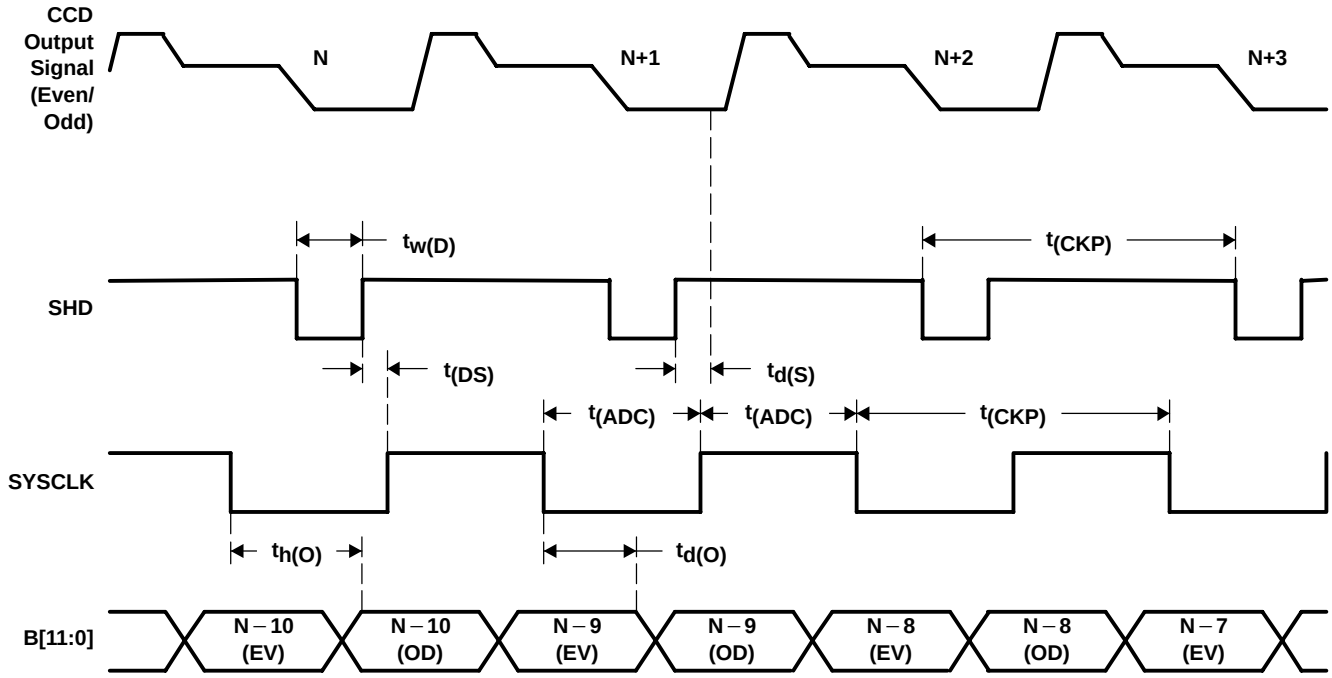
VSP5000 CDS Mode Timing Specification (Even and Odd Channels)



SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT
$t_{(CKP)}$	Clock period	33			ns
$t_{(ADC)}$	SYSCLK pulse width		16.7		ns
$t_{w(P)}$	SHP pulse width	6	8.3		ns
$t_{w(D)}$	SHD pulse width	6	8.3		ns
$t_{(PD)}$	SHP trailing edge to SHD leading edge	8			ns
$t_{(DP)}$	SHD trailing edge to SHP leading edge	8			ns
$t_{d(S)}$	Sampling delay		3.5		ns
$t_{(INHIBIT)}$	Inhibited clock period	10			ns
$t_{h(O)}$	Output hold time(1)	6			ns
$t_{d(O)}$	Output delay at data output delay = 0 ns(1)			9	ns
	Output delay at data output delay = 3 ns(2)			13	ns
DL	Data latency		9		Clock Cycles

(1) Load = 25 pF, data output delay = 0 ns, meaning the delay time setting by configuration register of the serial interface.
(2) Load = 25 pF, data output delay = 3 ns, meaning the delay time setting by configuration register of the serial interface.

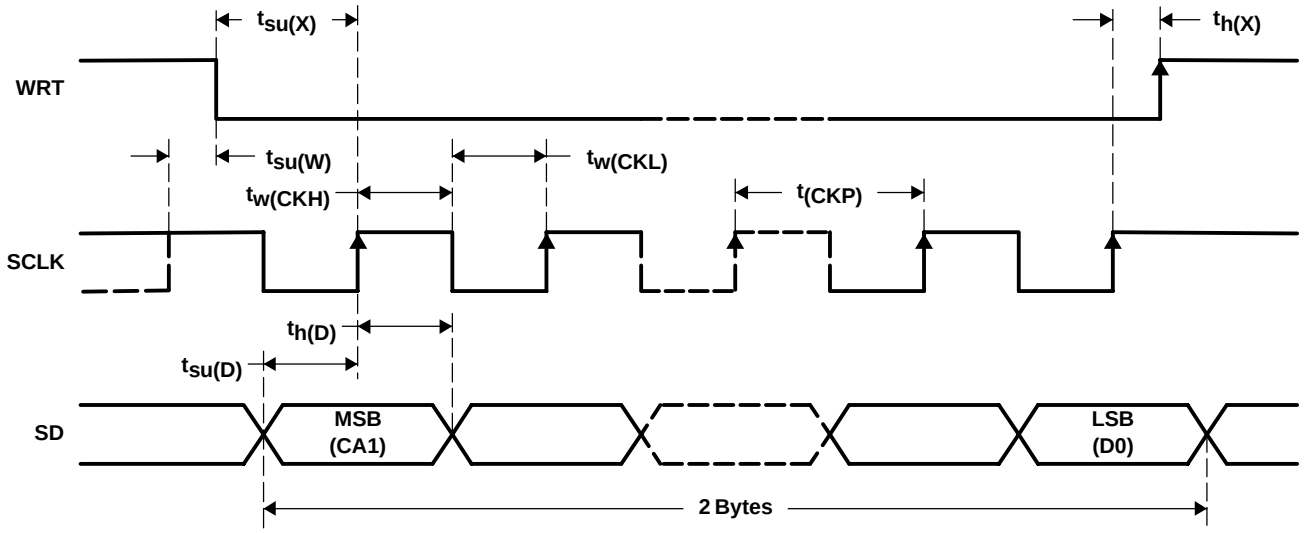
VSP5000 SH Mode Timing Specification (Even and Odd Channels)



SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT
$t_{(CKP)}$	Clock period	33			ns
$t_{(ADC)}$	SYSCLK pulse width		16.7		ns
$t_{w(D)}$	SHD pulse width	6	8.3		ns
$t_{d(S)}$	Sampling delay		3.5		ns
$t_{(DS)}$	SHD trailing edge to SYSCLK leading edge	–8		6	ns
$t_{h(O)}$	Output hold time(1)	6			ns
$t_{d(O)}$	Output delay at data output delay = 0 ns(1)			9	ns
	Output delay at data output delay = 3 ns(2)			13	ns
DL	Data latency		9		Clock Cycles

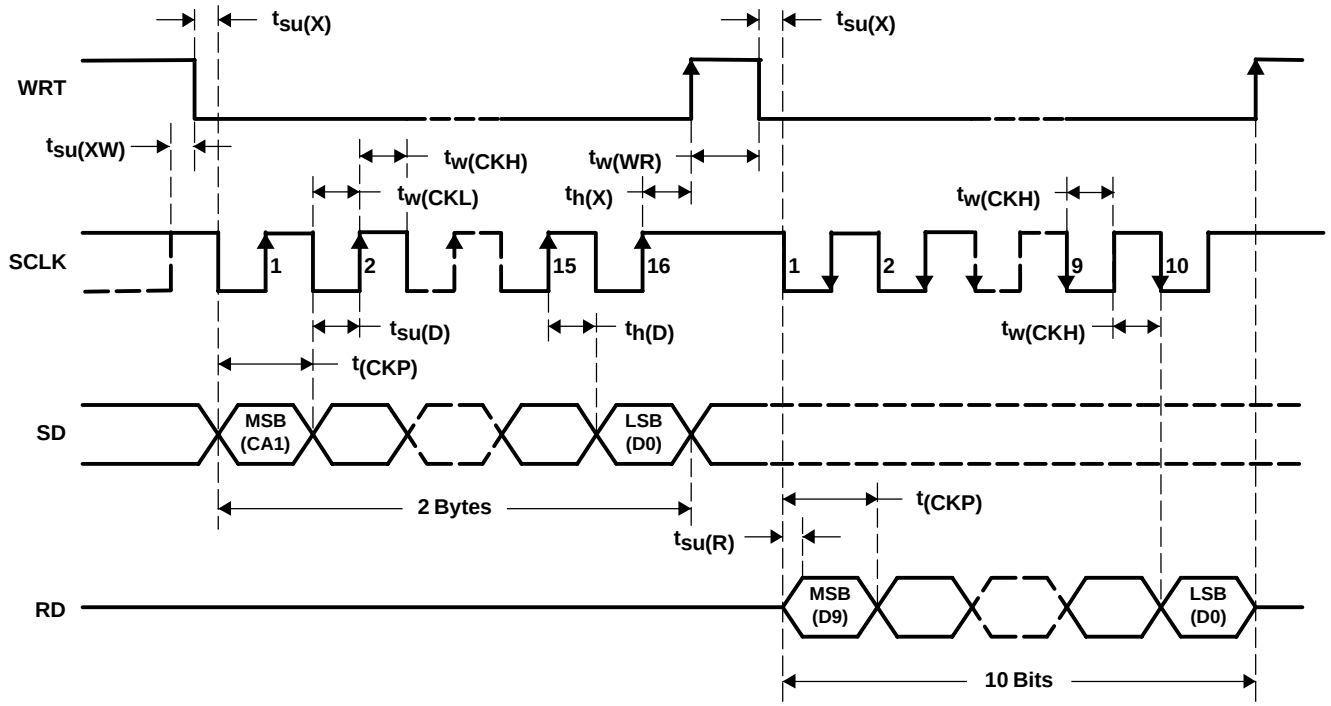
(1) Load = 25 pF, data output delay = 0 ns, meaning the delay time setting by configuration register of the serial interface.
(2) Load = 25 pF, data output delay = 3 ns, meaning the delay time setting by configuration register of the serial interface.

VSP5000 Serial Interface Timing Specification 1 (Write)



SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT
$t_{(CKP)}$	Clock period	100			ns
$t_{w(CKH)}$	Clock high pulse width	40			ns
$t_{w(CKL)}$	Clock low pulse width	40			ns
$t_{su(D)}$	Data setup time	30			ns
$t_{h(D)}$	Data hold time	30			ns
$t_{su(X)}$	WRT to SCLK setup time	15			ns
$t_{h(X)}$	SCLK to WRT hold time	15			ns
$t_{su(W)}$	WRT setup time	15			ns

VSP5000 Serial Interface Timing Specification 2 (Read)



SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT
$t_{(CKP)}$	Clock period	100			ns
$t_{w(CKH)}$	Clock high pulse width	40			ns
$t_{w(CKL)}$	Clock low pulse width	40			ns
$t_{su(D)}$	Data setup time (write)	30			ns
$t_{h(D)}$	Data hold time (write)	30			ns
$t_{su(X)}$	WRT to SCLK setup time	15			ns
$t_{h(X)}$	SCLK to WRT hold time	15			ns
$t_{su(XW)}$	WRT setup time	15			ns
$t_{w(WR)}$	Minimum WRT width	10			ns
$t_{su(R)}$	Data setup time (read)			30	ns

PRINCIPLES OF OPERATION

INTRODUCTION

The VSP5000 device was developed for an analog front-end of CCD line image sensor applications such as copiers, facsimiles, and scanners. The VSP5000 device provides two independent even/odd channels of processing line, each operating at 30 MHz.

The output signals from each even/odd channel of the CCD image sensor are sampled by a correlated double sampling (CDS) circuit and then transmitted to a 14-bit high-precision analog-to-digital converter (ADC). The ADC output is amplified to the required gain in the digital programmable gain amplifier (DPGA), then rounded to 12-bit data, and output sequentially as even/odd data, which synchronizes with SYSCLK. The CDS can be used as a sample/hold (SH) circuit by setting terminal 56 (CDS_SEL) low.

Each channel has an optical black level clamp circuit (OB loop) and automatically compensates for offsets of the CCD and CDS/SH during the OB pixel period (CLPOB). The OB level output value can be set at the required value by the serial interface. DC bias lost in ac-coupling is reproduced as an input clamp voltage, which is at a necessary level for internal operation. The input clamp voltage charges a capacitor connected to CCDIN during the dummy pixel period (INPUTCLP) by SHP.

Gain setting, operation polarity of each clock, and selection of operation mode are accomplished through a serial interface by accessing an internal register.

All register bits are reset to their default values by setting terminal 60 (RESET) to low.

CORRELATED DOUBLE SAMPLER (CDS) AND SAMPLE HOLD (SH) CIRCUIT

The CDS circuit removes low frequency and common-mode noise from the CCD image sensor output as it fluctuates per pixel. Noise longer than one pixel in duration among the input signals is rejected by the subtraction operation at the CDS circuit. Figure 1 shows a simplified CDS block graphic.

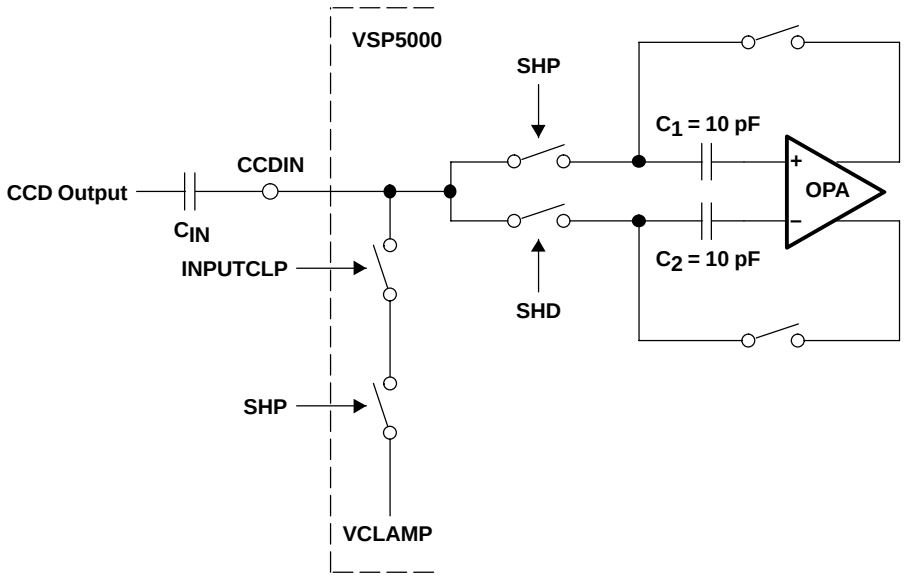


Figure 1. Simplified Block Diagram of CDS and Input Clamp

The CDS can be configured as a sample hold (SH) circuit by setting terminal 56 (CDS_SEL) low. Figure 2 shows a simplified SH circuit block graphic.

In the SH mode, the input clamp voltage (V_{CLAMP}) is charged by the INPUTCLP signal and the sampling signal (SHD) to the C_{IN} capacitor. INPUTCLP is activated at the dummy pixel (or OB pixel) of the CCD. By these operations, the dummy pixel (or OB pixel) level voltage is fixed to V_{CLAMP} at the CCDIN terminal.

At the sampling for the OB pixel and effective pixel, V_{CLAMP} voltage is charged to capacitor C_1. The voltage lower than V_{CLAMP}, according to the signal voltage from the CCD, is charged to capacitor C_2. As the voltage difference in C_1 and C_2 is acquired at the hold period, the signals from the CCD are acquired as the voltage based on V_{CLAMP}.

In the CDS mode, signal voltage takes as voltage difference between sampled voltage by SHP (reference level) and SHD (data level), the signal level is not affected, even when V_{CLAMP} changes or fluctuates in some degree due to leakage, etc. However, when operated as SH, V_{CLAMP} fluctuation causes an offset error, because the signal is acquired based on V_{CLAMP}. In order to prevent V_{CLAMP} leakage, a buffer is inserted to input in the SH mode.

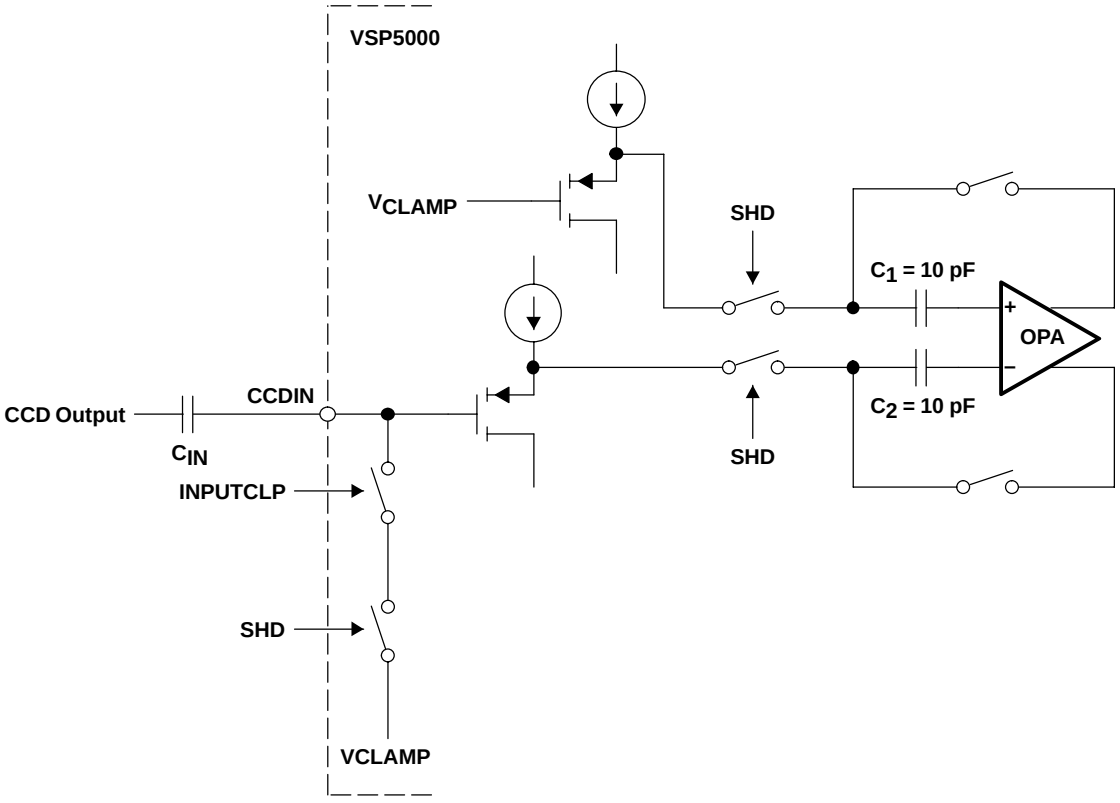


Figure 2. Simplified Sample Hold (SH) Circuit

INPUT CLAMP (DUMMY PIXEL CLAMP)

Output from the CCD image sensor is ac-coupled with the VSP5000 device through a capacitor. The input clamp reproduces the dc bias lost by ac-coupling and supplies optimum dc bias for proper operation of the CDS/SH circuit. Simplified block diagrams of the input clamp circuit are shown in Figure 1 and Figure 2.

The input signal level is clamped to the internal reference voltage by activating both SHP (when at CDS mode or SHD when at SH mode) and INPUTCLP during the CCD dummy pixel output period.

HIGH PERFORMANCE ANALOG-TO-DIGITAL CONVERTER (ADC)

The analog-to-digital converter of the VSP5000 device is composed of pipeline architecture. The ADC converter has complete differential circuit configuration, error correction circuit, and 14-bit resolution is assured.

Circuits which generate the necessary reference voltage at the ADC are built inside the device and are shown as REFP (high-potential reference), REFN (low-potential reference), and CM (common-mode voltage) terminals outside the device. In order to assure ADC accuracy, these reference voltage terminals need to be sufficiently decoupled by capacitors.

DIGITAL PROGRAMMABLE GAIN AMPLIFIER (DPGA)

The digital programmable gain amplifier (DPGA) circuit controls the gain value in the range of 0 fold to 16 fold (24 dB) by inputting the digital code through the serial interface. See the *serial interface* section for details. Gain changes linearly in proportion to the setting code.

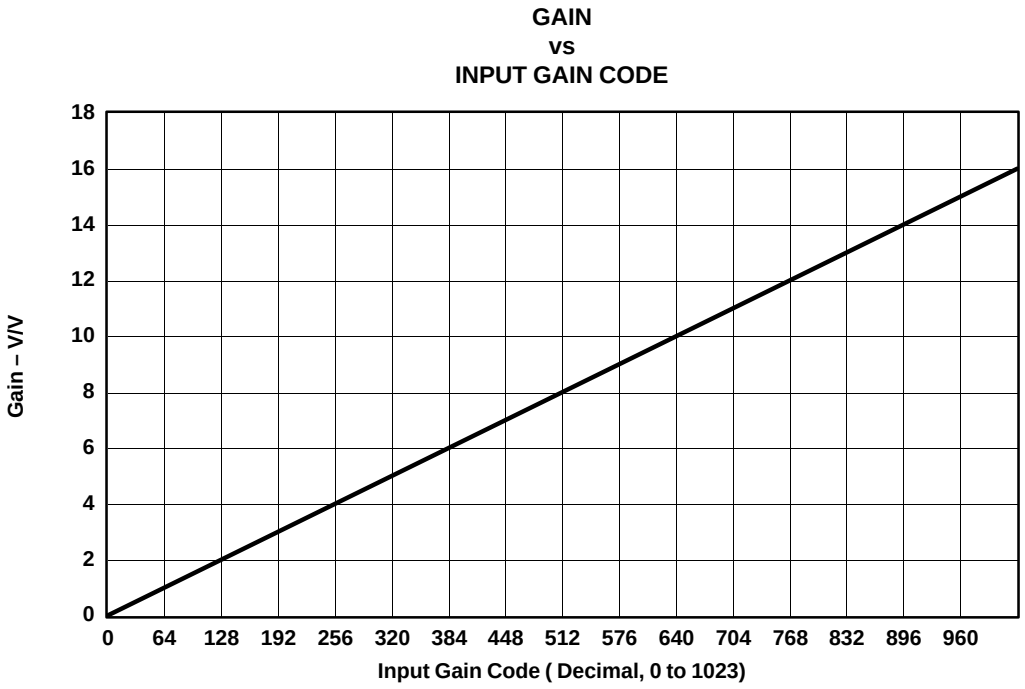


Figure 3. Setting Code vs Gain

OPTICAL BLACK (OB) LEVEL LOOP AND OB CLAMP LEVEL

The VSP5000 device has a built-in self calibration circuit (OB loop), which compensates the OB level by using the optical black (OB) pixels that are output from the CCD image sensor. Figure 4 shows a block diagram of the OB loop and OB clamp circuit.

The CCD offset is compensated by converging the calibration circuit, while activating CLPOB during a period when the OB pixels are output from the CCD.

In the CDS mode, the CCD offset is compensated as a difference between the reference level and data level of an OB pixel. In the SH mode, V_{CLAMP} is compensated by INPUTCLP as a difference between the fixed dummy pixel and the OB pixel.

These compensated signal levels are recognized as actual OB levels and the outputs are clamped to the OB levels set by the serial interface. These OB levels are the black base for the effective pixel period thereafter.

Since the DPGA is a gain stage outside the OB loop, the OB levels are not affected even when the gain is changed.

The converging time of the OB loop is determined based on the capacitor value connected to the COB terminal and the output from the current output DAC of the loop. The time constant can be obtained from the following equation:

$$T = \frac{C}{\left(16384 \times I_{MIN}\right)}$$

where, C is the capacitor value connected to COB, I_{MIN} is the minimum current (0.15 μA) of the current DAC, and 0.15 μA is equivalent to 1 LSB of the DAC output. When C = 0.1 μF, T is 40.7 μs. Slew rate (SR) can be obtained from following equation:

$$SR = \frac{I_{MAX}}{C}$$

where, C is the capacitor value connected to COB, I_{MAX} is the maximum current (153 μA) of the current DAC, and 153 μA is equivalent to 1023 LSB of the DAC output.

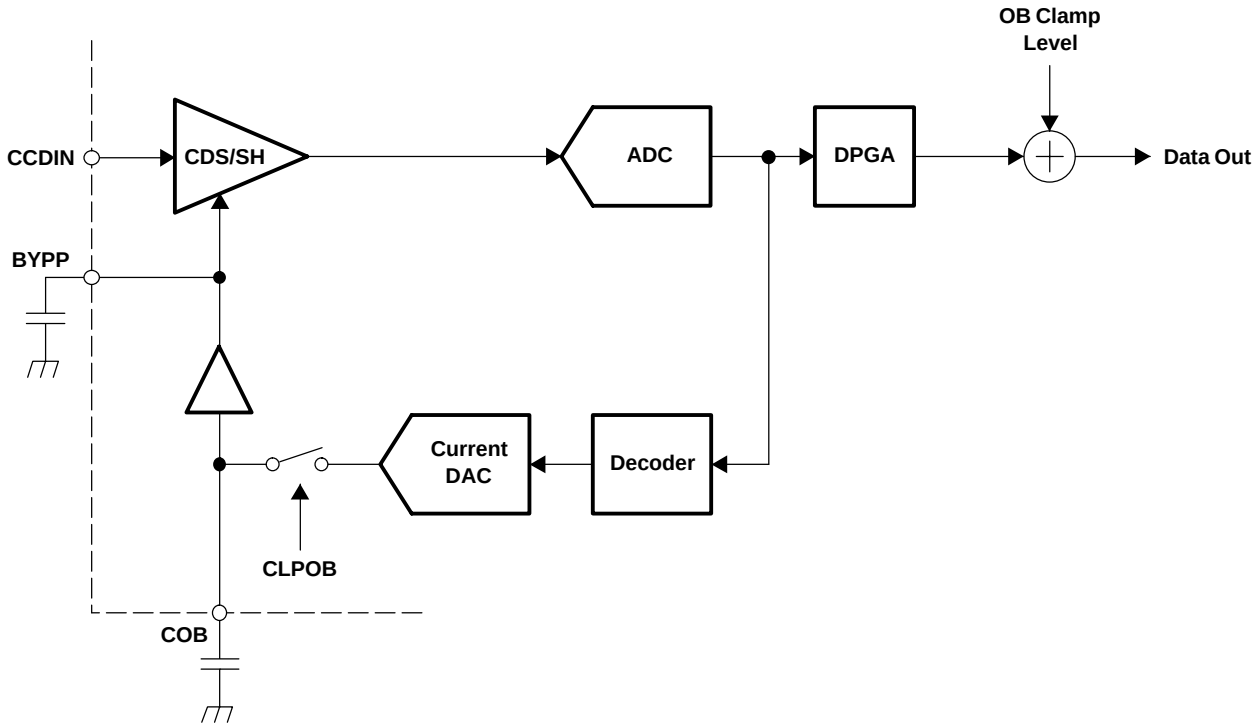


Figure 4. OB Loop and OB Level Clamp

The OB clamp level (digital output value) can be set through the serial interface by inputting a digital code to the OB clamp level register. Table 1 shows the digital code and the corresponding OB clamp level.

Table 1. Input Code and OB Clamp Level To Be Set

INPUT CODE	OB CLAMP LEVEL (12-BIT)
0000 0000	0 LSB
0000 0001	2 LSB
⋮	⋮
0100 1111	158 LSB
0101 0000 (default)	160 LSB
0101 0001	162 LSB
⋮	⋮
1011 1111	508 LSB
1111 1111	510 LSB

SETTLING OF OB LOOP AND INPUT CLAMP

As the input clamp voltage of the capacitor connected to CCDIN and the voltage of the OB loop COB capacitor are completely discharged at start-up and after a long standby state, these two capacitors need to be charged to the proper operational voltage.

The charging time for the input clamp voltage is logical AND of SHP (SHD when in SH mode) and INPUTCLP. Actual charging time per line is only the width of the numbers of the SHP in the dummy pixel period. Equally, COB is only charged during the OB pixel period. Therefore, some time is necessary to bring the VSP5000 device to normal operation status at start-up.

Though start-up time depends on the number of dummy and pixels per line, 500 ms to 1 s must be kept to be on the safe side.

STANDBY MODE

Normal operation mode and standby mode can be switched by the serial interface.

In standby mode, power consumption can be reduced as operation is suspended, except for the interface circuit and reference voltage supply. During standby mode, further power reduction may be obtained by suspending SYSCLK. When restoring SYSCLK, which was suspended during standby mode, more than two clocks of SYSCLK must be acquired before inputting the first command.

OUTPUT DATA DELAY

At the timing when the output data changes, large transient noise occurs due to many logic lines changing at one time. When this transient noise timing overlaps the analog signal sampling timing, it may affect the A/D converting value. To avoid this, changing the timing of the VSP5000 output data can be delayed in approximately 3-ns steps by the serial control.

Delayed value, in this case, means the time addition for the default time between SYSCLK and the data output of the timing specification.

TEST MODE AND TEST PATTERN

The VSP5000 device can be set to the test mode by setting the configuration register. During the test mode, the test pattern generated inside the device is output with or without input.

There are two test patterns. One is a pattern which outputs code that is OB level +128 LSB per specific number of pixels (stripe pattern) and the other is a pattern which increments code from 1 to 4095 in specified LSB per pixel (gradation pattern). These can be selected by the serial interface setting the configuration register.

CHIP ADDRESS

The VSP5000 device has two chip address terminals, CA0 and CA1. The setting of these terminals gives a particular address for the device and the data-writing device can be selected by the address in the serial interface data. By using this function, the serial interface can be used as a common line for up to four devices.

REGISTER READING

Each register data can be read from the RDO terminal by setting the A3 bit of the serial interface data to 1 and setting the reading register address to A[2:0].

After writing data which specifies the register, pulldown WRT and pullup SCLK and the output reading register value will be output sequentially on RDO. See the *serial interface* section for details.

While reading the register, the writing function is disabled.

SERIAL INTERFACE

The serial interface of the VSP5000 device is composed of three signals: SDI, SCLK, and WRT. SDI data is sequentially stored in the shift register at the SCLK rising edge and shift register data is stored to parallel latch at the WRT rising edge.

Serial data is 2-bytes fixed length and is composed of a 2-bit chip address, a 4-bit register address, and 10-bit data. The chip address can only write to a register in a device that matches its value to the address set by CA0 and CA1. By using this 2-bit chip address, the serial interface can be shared by other devices.

Both address and data store from MSB data first and LSB data last. When data with more than 2 bytes is applied, the final 2 bytes immediately before the WRT rising edge are effective and data stored first is lost.

Table 2 shows the register configuration and serial data format.

Each register value is defined at the time of power on. Resetting to the default value by the RESET signal or setting to the desired value by the serial interface is necessary.

Table 2. Serial Interface Data Format

	MSB															LSB
REGISTERS	**CA1**	**CA0**	**A3**	**A2**	**A1**	**A0**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
Configuration	X	X	0	0	0	0	0	0	C7	C6	0	C4	0	C2	C1	C0
Standby mode	X	X	0	0	0	1	0	0	0	0	0	0	0	0	0	S0
DPGA gain even	X	X	0	0	1	0	G9	G8	G7	G6	G5	G4	G3	G2	G1	G0
DPGA gain odd	X	X	0	0	1	1	G9	G8	G7	G6	G5	G4	G3	G2	G1	G0
OB clamp level even	X	X	0	1	0	0	0	0	O7	O6	O5	O4	O3	O2	O1	O0
OB clamp level odd	X	X	0	1	0	1	0	0	O7	O6	O5	O4	O3	O2	O1	O0
Test mode	X	X	0	1	1	0	0	0	0	0	T5	T4	0	T2	0	T0
Reserved	X	X	0	1	1	1	0	0	0	0	0	0	0	0	0	0
Read out	X	X	1	R2	R1	R0	X	X	X	X	X	X	X	X	X	X

REGISTER DEFINITION

Configuration Register (address = 00h)

C[2:0]: Clock polarity select (default = 000)

C0: INPUTCLP polarity — 0 = active low, 1 = active high
C1: CLPOB polarity — 0 = active low, 1 = active high
C2: SHP/SHD polarity — 0 = active low, 1 = active high

C4: Data output order (default = 0)

0 = Even/Odd, 1 = Odd/Even

C[7:6]: Data output delay (default = 00)

C7 = 0, C6 = 0 — Delay time = 0 ns (typ)
C7 = 0, C6 = 1 — Delay time = 3 ns (typ)
C7 = 1, C6 = 0 — Delay time = 6 ns (typ)
C7 = 1, C6 = 1 — Delay time = 9 ns (typ)

Standby Mode (address = 01h)

S0: Standby/normal operation select (default = 0)

0 = Normal operation mode, 1 = standby mode

Even Channel gain Register (address = 02h)

G[9:0]: Gain value = GAIN[9:0] /64 (default = 00 0100 0000)

Odd Channel Gain Register (address = 03h)

G[9:0]: Gain value = GAIN[9:0] /64 (default = 00 0100 0000)

Even Channel OB Clamp Register (address = 04h)

O[7:0]: OB clamp level = 2LSB x O[7:0] (default = 0101 0000)

Odd Channel OB Clamp Register (address = 05h)

O[7:0]: OB clamp level = 2LSB x O[7:0] (default = 0101 0000)

Test Mode Register (address = 06h)

T0: Test mode enable/disable (default = 0)

0 = Disable, 1 = Enable

T2: Test pattern select (default = 0)

0 = Gradation Pattern, 1 = Stripe Pattern

T[5:4]: Test pattern data interval (default = 00)

T5 = 0, T4 = 0 — Stripe pattern = 8 pixels, gradation pattern = 2 pixels
T5 = 0, T4 = 1 — Stripe pattern = 16 pixels, gradation pattern = 4 pixels
T5 = 1, T4 = 0 — Stripe pattern = 32 pixels, gradation pattern = 8 pixels
T5 = 1, T4 = 1 — Stripe pattern = 64 pixels, gradation pattern = 16 pixels

Register Read Out

R[2:0]: sets reading register address (A[2:0])

POWER SUPPLY, GROUNDING, AND DEVICE DECOUPLING RECOMMENDATIONS

The VSP5000 device incorporates high-precision, high-speed, ADC and analog circuitry, which are vulnerable to any extraneous noise from the voltage rails or elsewhere. For this reason, although the VSP5000 device has analog and digital supply terminals, it must be treated as an analog component and all supply terminals except for V_{DD} must be powered by the analog supply only. This ensures the most consistent results, since digital power lines often carry high levels of wide-band noise that would otherwise be coupled into the device and degrade the achievable performance.

Proper grounding, short lead length, and the use of ground planes are also important for high-frequency designs. Multilayer PC boards are recommended for the best performance, since they offer distinct advantages, for example, minimized ground impedance and separation of signal layers by ground layers. It is highly recommended that the analog and digital ground terminals of the VSP5000 device be joined together at the IC and be connected only to the analog ground of the system.

The driver stage of the digital outputs (B[11:0]) is supplied through a dedicated supply V_{DD} (terminal 18). V_{DD} must be separated from the other supply terminals completely or at least with a ferrite bead.

Because of the high operational speed, the ADC also generates high-frequency current transients and noises that are fed back into the supply and reference lines. This requires the supply and reference terminals to be sufficiently bypassed. In most cases, 0.1-μF ceramic chip capacitors are adequate to decouple the reference terminals. Supply terminals should be decoupled to the ground plane with a parallel combination of tantalum (1 μF to 22 μF) and ceramic (0.1 μF) capacitors. The effectiveness of the decoupling largely depends on the proximity to the individual terminal. V_{DD} must be decoupled to the proximity of DGND (terminal 17 and terminal 64).

PACKAGING INFORMATION

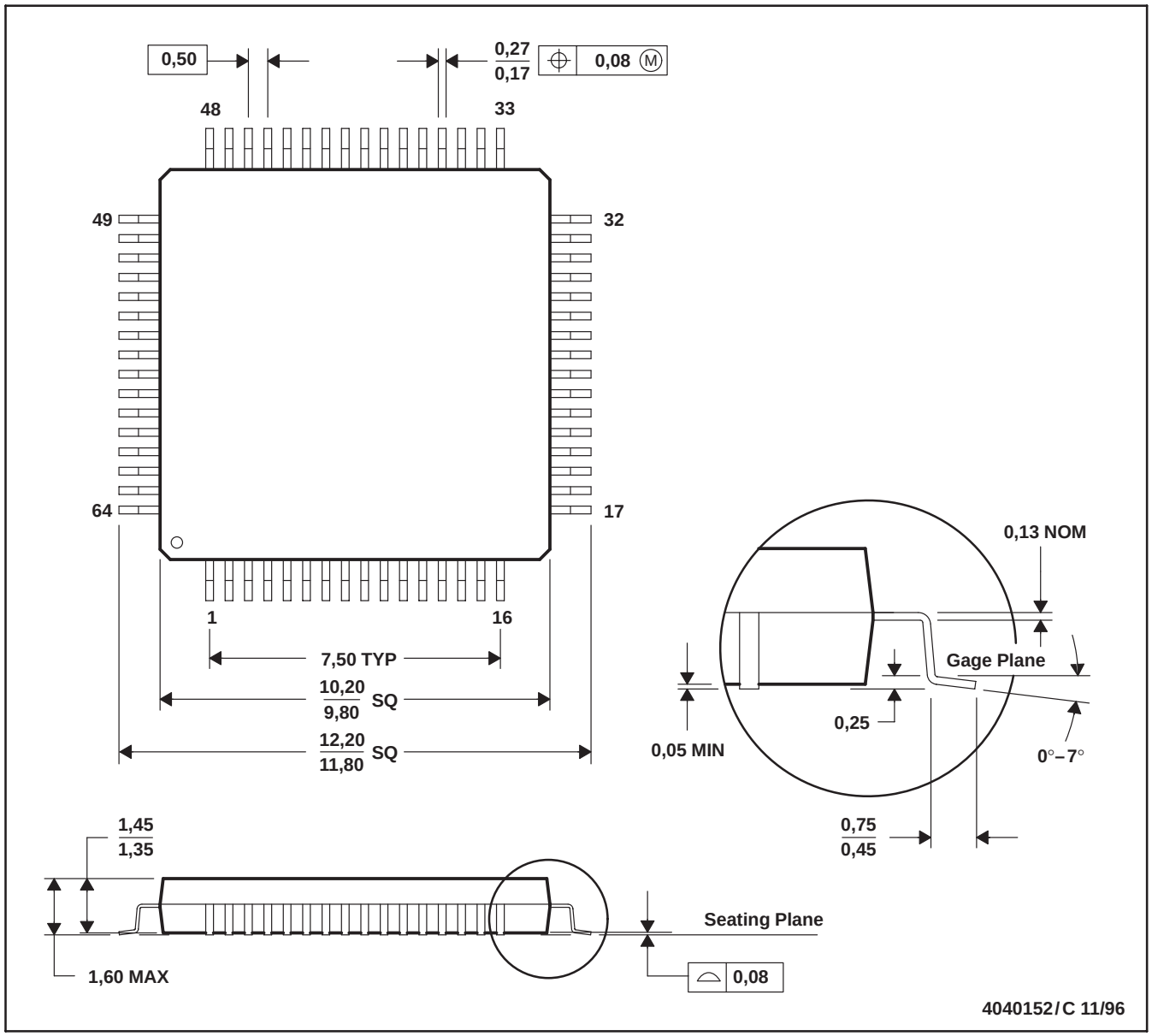
Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
VSP5000PM	NRND	LQFP	PM	64	160	Green (RoHS & no Sb/Br)	A42 SNBI	Level-1-260C-UNLIM
VSP5000PMG6	NRND	LQFP	PM	64	160	Green (RoHS & no Sb/Br)	A42 SNBI	Level-1-260C-UNLIM
VSP5000Y	NRND	SOIC	D	64		TBD	Call TI	Call TI

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

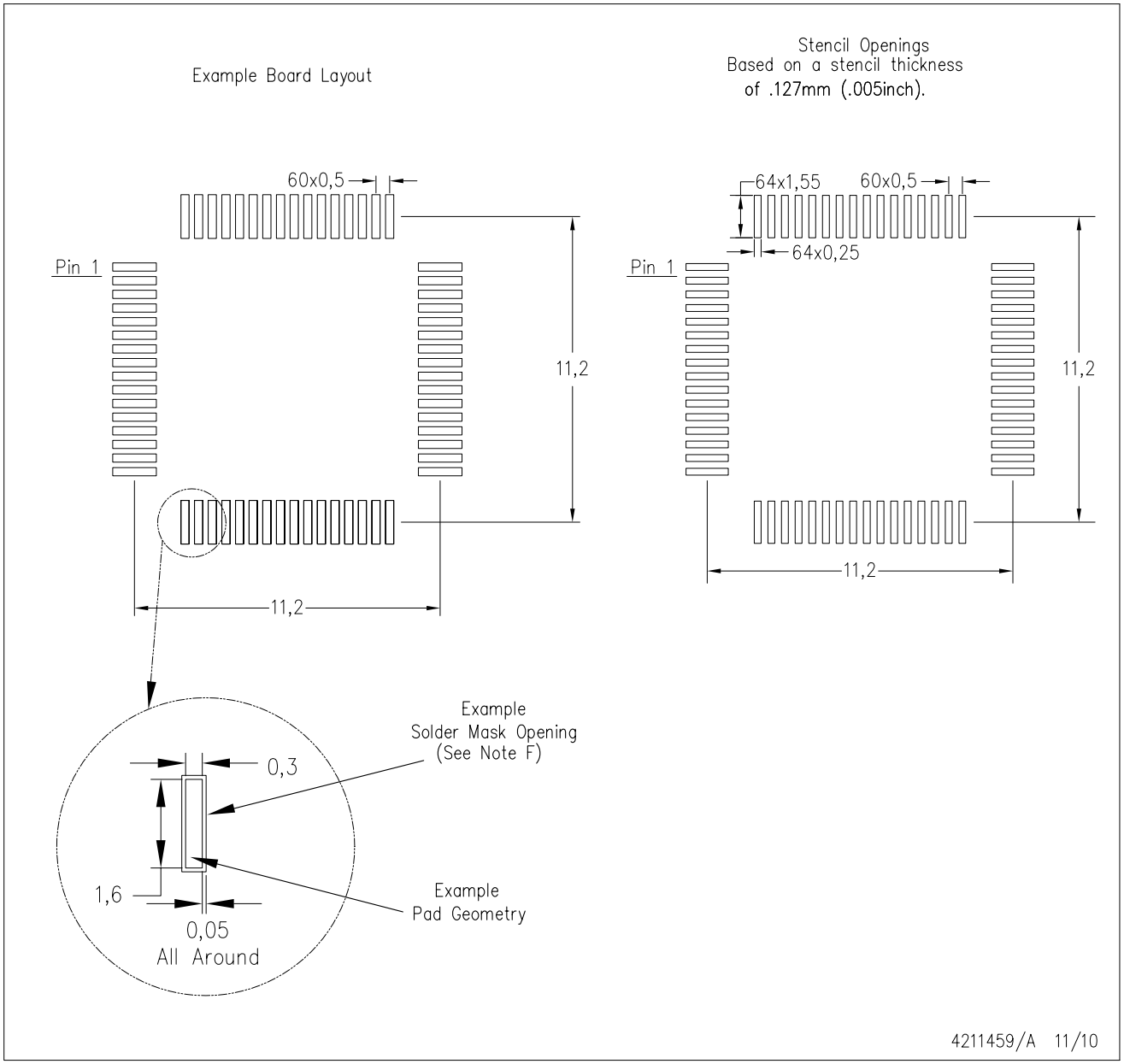
(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

PM (S-PQFP-G64) **PLASTIC QUAD FLATPACK**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-026
D. May also be thermally enhanced plastic with leads connected to the die pads.

PM (S–PQFP–G64) PLASTIC QUAD FLATPACK



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.
D. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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