



Burr-Brown Products
from Texas Instruments



VSP3200
VSP3210

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CCD SIGNAL PROCESSOR FOR SCANNER APPLICATIONS

FEATURES

- **INTEGRATED TRIPLE-CORRELATED DOUBLE SAMPLER**
- **OPERATION MODE SELECTABLE:**
1-Channel, 3-Channel CCD Mode, 8MSPs
- **PROGRAMMABLE GAIN AMPLIFIER:**
0dB to +13dB
- **SELECTABLE OUTPUT MODES:**
Normal/Demultiplexed
- **OFFSET CONTROL RANGE: ±500mV**
- **+3V, +5V Digital Output**
- **LOW POWER: 300mW (typ)**
- **LQFP-48 SURFACE-MOUNT PACKAGE**

DESCRIPTION

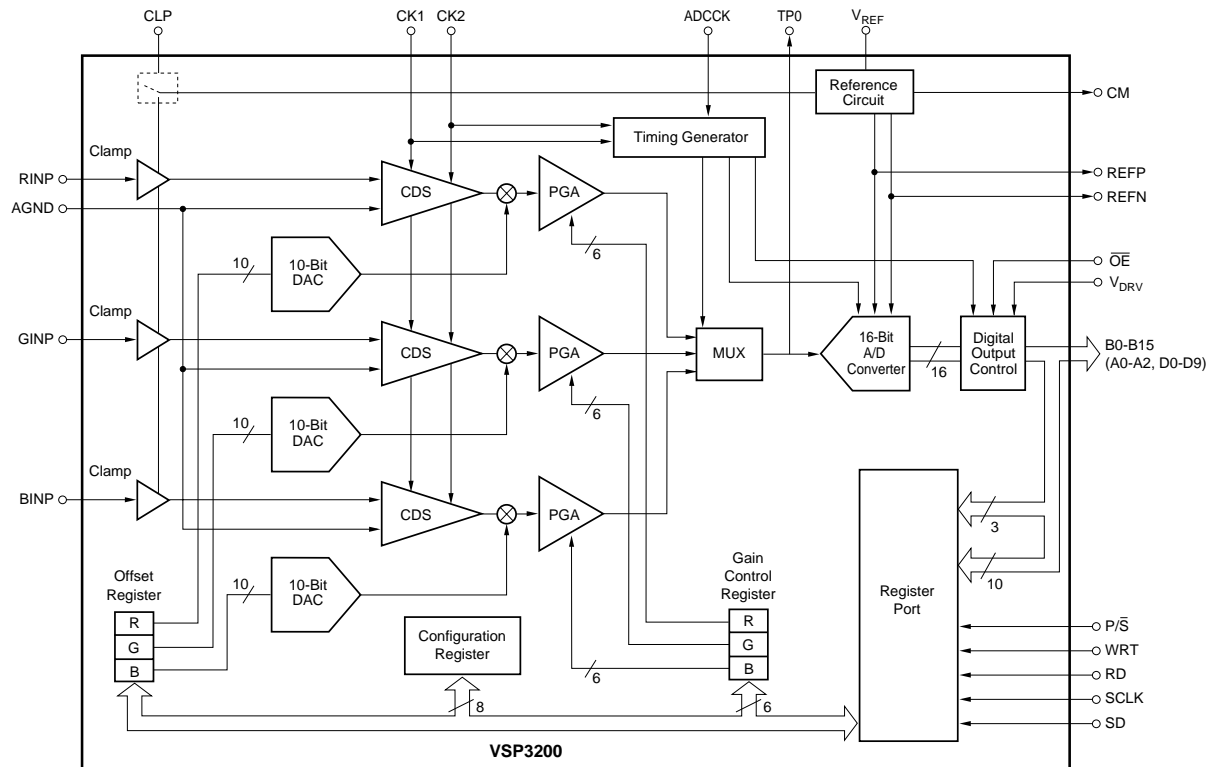
The VSP3200 and VSP3210 are complete CCD image processors that operate from single +5V supplies.

This complete image processor includes three Correlated Double Samplers (CDSs) and Programmable Gain Amplifiers (PGAs) to process CCD signals.

The VSP3200 is interface compatible with the VSP3210, which is a 16-bit, one-chip product.

The VSP3210 is pin-to-pin compatible with VSP3100, when in demultiplexed output mode.

The VSP3200 and VSP3210 can be operated from 0°C to +85°C, and are available in LQFP-48 packages.



SPECIFICATIONS

At $T_A = 25^\circ\text{C}$, $V_{CC} = +5.0\text{V}$, $V_{DRV} = +3.0\text{V}$, Conversion Rate (f_{ADCCK}) = 6MHz, $f_{CK1} = 2\text{MHz}$, $f_{CK2} = 2\text{MHz}$, PGA Gain = 1, normal output mode, no output load, unless otherwise specified.

| PARAMETER | CONDITIONS | VSP3200Y VSP3210Y | | | UNITS |
|--|---|--|---|--|--|
| | | MIN | TYP | MAX | |
| RESOLUTION | | | 16 | | Bits |
| CONVERSION CHARACTERISTICS 1-Channel CCD Mode, Max 3-Channel CCD Mode, Max | | | | 8 8 | MHz MHz |
| DIGITAL INPUTS Logic Family Convert Command High-Level Input Current ($V_{IN} = V_{CC}$) Low-Level Input Current ($V_{IN} = 0\text{V}$) Positive-Going Threshold Voltage Negative-Going Threshold Voltage Input Limit Input Capacitance | Start Conversion | | CMOS Rising Edge of ADCCK Clock | 20 20 2.20 $V_{CC} + 0.3$ | μA μA V V V pF |
| ANALOG INPUTS Full-Scale Input Range Input Capacitance Input Limits External Reference Voltage Range Reference Input Resistance | | 0.5 AGND – 0.3 0.25 | 10 800 | 3.5 $V_{CC} + 0.3$ 1.75 | Vp-p pF V V Ω |
| DYNAMIC CHARACTERISTICS Integral Non-Linearity (INL) Differential Non-Linearity (DNL) No Missing Codes Output Noise | $V_{IN} = 500\text{mV}$ ($V_{REF} = 1.0\text{V}$) PGA Gain = 0dB, Input Grounded | | ± 8 ± 1.5 Guaranteed 8.0 | | LSB LSB LSBs rms |
| PSRR | $V_{CC} = +5\text{V}$, $\pm 0.25\text{V}$ | | 0.04 | | % FSR |
| DC ACCURACY Zero Error Gain Error Offset Control Range | 10-Bit Control DAC Output Voltage Range | | 0.8 1.5 ± 500 | | % FS % FS mV |
| DIGITAL OUTPUTS Logic Family Logic Coding Digital Data Output Rate, Max V_{DRV} Supply Range Output Voltage, $V_{DRV} = +5\text{V}$ Low Level High Level Low Level High Level Output Voltage, $V_{DRV} = +3\text{V}$ Low Level High Level Output Enable Time 3-State Enable Time Output Capacitance Data Latency Data Output Delay | Normal Mode Demultiplexed Mode $I_{OL} = 50\mu\text{A}$ $I_{OH} = 50\mu\text{A}$ $I_{OL} = 1.6\text{mA}$ $I_{OH} = 0.5\text{mA}$ $I_{OL} = 50\mu\text{A}$ $I_{OH} = 50\mu\text{A}$ Output Enable = LOW Output Enable = HIGH $C_L = 15\text{pF}$ | 8 8 +2.7 +4.6 +2.4 +2.5 | CMOS Straight Binary | +5.3 +0.1 +0.4 +0.1 | MHz MHz V V V V V V ns ns pF Clock Cycles ns |
| POWER-SUPPLY REQUIREMENTS Supply Voltage: V_{CC} Supply Current: I_{CC} (No Load) Power Dissipation (No Load) | 3-Ch CCD Mode 1-Ch CCD Mode 3-Ch CCD Mode 1-Ch CCD Mode | 4.7 | 5 70 60 350 300 | 5.3 | V mA mA mW mW |
| TEMPERATURE RANGE Operation Temperature Thermal Resistance | LQFP-48 θ_{JA} | 0 | 100 | +85 | $^\circ\text{C}$ $^\circ\text{C/W}$ |

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

| | |
|--|------------------------------|
| Supply Voltage: V_{CC} , V_{DRV} | +6.5V |
| Supply Voltage Differences: Among V_{CC} | $\pm 0.1V$ |
| GND Voltage Differences: Among GNDA | $\pm 0.1V$ |
| Digital Input Voltage | -0.3V to ($V_{CC} + 0.3V$) |
| Analog Input Voltage | -0.3V to ($V_{CC} + 0.3V$) |
| Input Current (Any Pins Except Supplies) | $\pm 10mA$ |
| Ambient Temperature Under Bias | -40°C to +125°C |
| Storage Temperature | -55°C to +125°C |
| Junction Temperature | +150°C |
| Lead Temperature (soldering, 5s) | +260°C |
| Package Temperature (IR Reflow, peak, 10s) | +235°C |

NOTE: (1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability.



ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PACKAGE/ORDERING INFORMATION

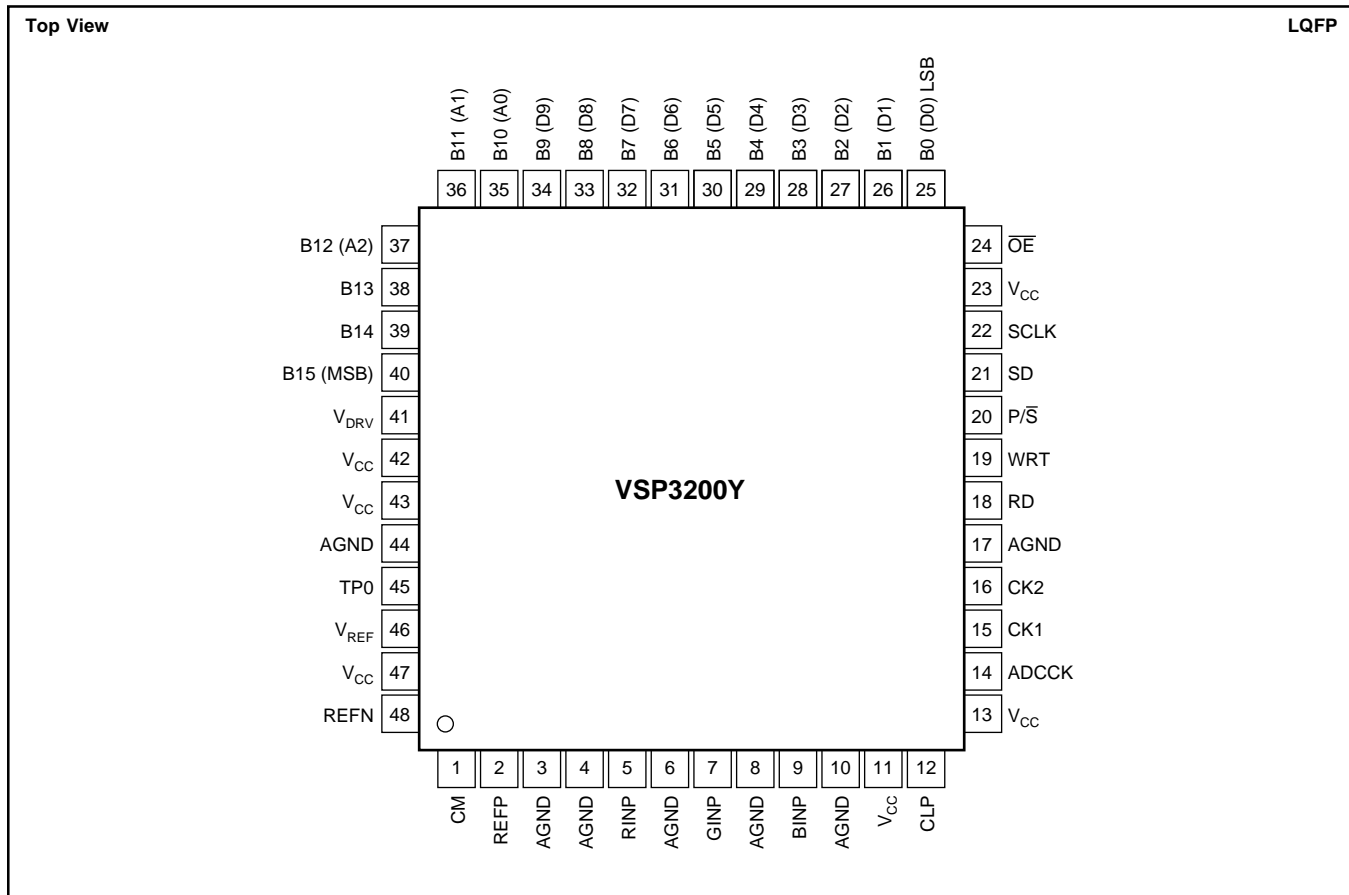
| PRODUCT | PACKAGE | PACKAGE DRAWING NUMBER | SPECIFIED TEMPERATURE RANGE | PACKAGE MARKING | ORDERING NUMBER ⁽¹⁾ | TRANSPORT MEDIA |
|---------------|--------------|------------------------|-----------------------------|-----------------|--------------------------------|---------------------------------|
| VSP3200Y " | LQFP-48 " | 340 " | 0°C to +85°C " | VSP3200Y " | VSP3200Y VSP3200Y/2K | 250-Piece Tray Tape and Reel |
| VSP3210Y " | LQFP-48 " | 340 " | 0°C to +85°C " | VSP3210Y " | VSP3210Y VSP3210Y/2K | 250-Piece Tray Tape and Reel |

NOTE: (1) Models with a slash (/) are available only in Tape and Reel in the quantities indicated (e.g., /2K indicates 2000 devices per reel). Ordering 2000 pieces of "VSP3200Y/2K" will get a single 2000-piece Tape and Reel.

DEMO BOARD ORDERING INFORMATION

| PRODUCT | PACKAGE |
|----------|--------------|
| VSP3200Y | DEM-VSP3200Y |

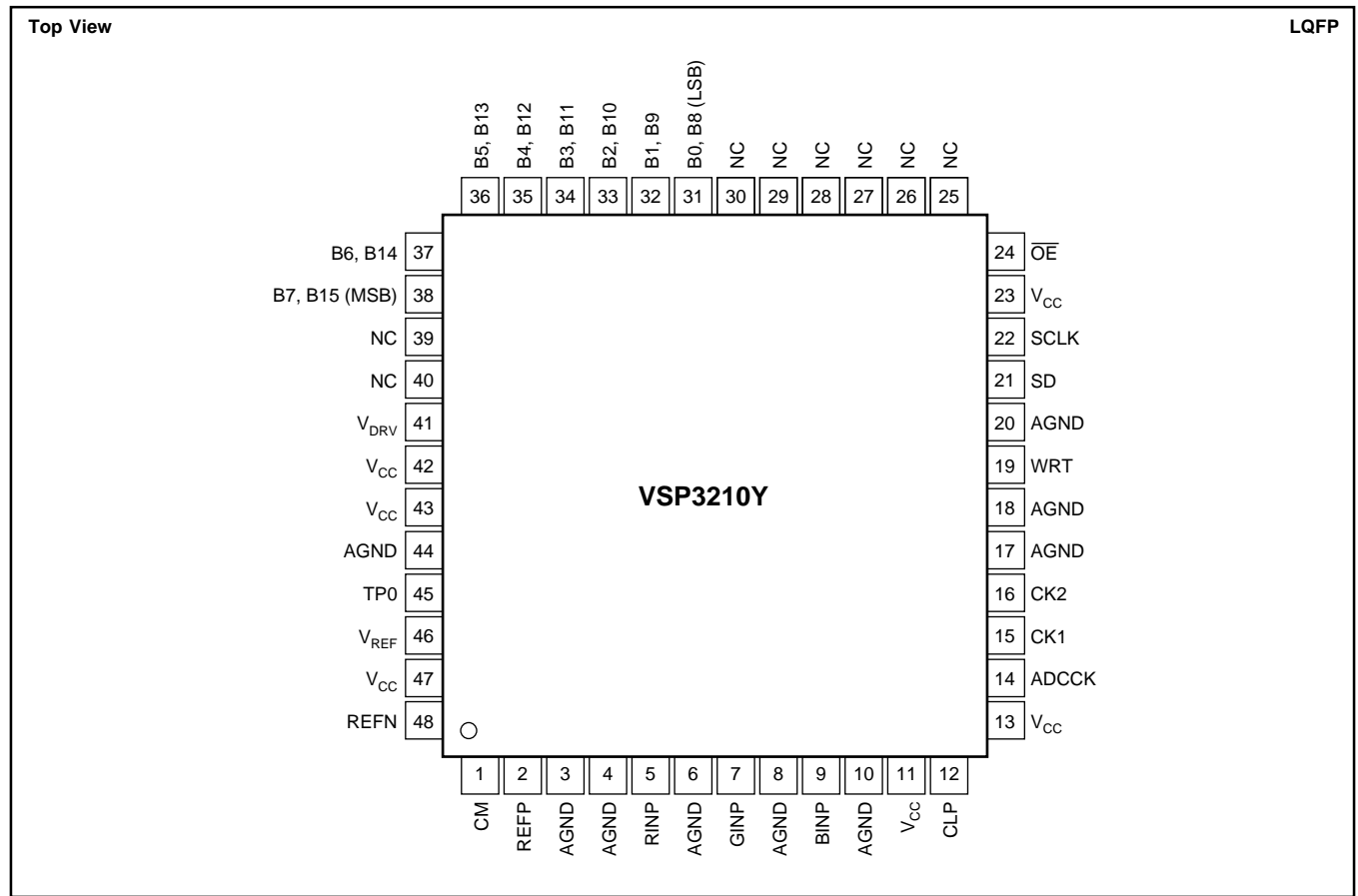
PIN CONFIGURATION



PIN DESCRIPTIONS (VSP3200Y)

| PIN | DESIGNATOR | TYPE | DESCRIPTION | PIN | DESIGNATOR | TYPE | DESCRIPTION |
|-----|-----------------|------|--|-----|------------------|------|---|
| 1 | CM | AO | Common-Mode Voltage | 29 | B4 (D4) | DIO | A/D Output (Bit 4) and Register Data (D4) |
| 2 | REFP | AO | Upper-Level Reference | 30 | B5 (D5) | DIO | A/D Output (Bit 5) and Register Data (D5) |
| 3 | AGND | P | Analog Ground | 31 | B6 (D6) | DIO | A/D Output (Bit 6) and Register Data (D6) |
| 4 | AGND | P | Analog Ground | 32 | B7 (D7) | DIO | A/D Output (Bit 7) and Register Data (D7) |
| 5 | RINP | AI | Red Channel Analog Input | 33 | B8 (D8) | DIO | A/D Output (Bit 8) and Register Data (D8) |
| 6 | AGND | P | Analog Ground | 34 | B0 LSB | DO | A/D Output (Bit 0) when Demultiplexed Output Mode |
| 7 | GINP | AI | Green Channel Analog Input | 35 | B1 | DO | A/D Output (Bit 1) when Demultiplexed Output Mode |
| 8 | AGND | P | Analog Ground | 36 | B11 (A1) | DIO | A/D Output (Bit 11) and Register Address (A1) |
| 9 | BINP | AI | Blue Channel Analog Input | 37 | B3 | DO | A/D Output (Bit 3) when Demultiplexed Output Mode |
| 10 | AGND | P | Analog Ground | 38 | B12 (A2) | DIO | A/D Output (Bit 12) and Register Address (A2) |
| 11 | V _{CC} | P | Analog Power Supply, +5V | 39 | B4 | DO | A/D Output (Bit 4) when Demultiplexed Output Mode |
| 12 | CLP | DI | Clamp Enable HIGH = Enable, LOW = Disable | 40 | B13 | DO | A/D Output (Bit 13) |
| 13 | V _{CC} | P | Analog Power Supply, +5V | 41 | B5 | DO | A/D Output (Bit 5) when Demultiplexed Output Mode |
| 14 | ADCCK | DI | Clock for A/D Converter Digital Data Output | 42 | B6 | DO | A/D Output (Bit 6) when Demultiplexed Output Mode |
| 15 | CK1 | DI | Sample Reference Clock | 43 | B15 MSB | DO | A/D Output (Bit 15) |
| 16 | CK2 | DI | Sample Data Clock | 44 | B7 MSB | DO | A/D Output (Bit 7) when Demultiplexed Output Mode |
| 17 | AGND | P | Analog Ground | 45 | V _{DRV} | P | Digital Output Driver Power Supply |
| 18 | RD | DI | Read Signal for Registers | 46 | V _{CC} | P | Analog Power Supply, +5V |
| 19 | WRT | DI | Write Signal for Registers | 47 | V _{CC} | P | Analog Power Supply, +5V |
| 20 | P/S | DI | Parallel/Serial Port Select HIGH = Parallel Port, LOW = Serial Port | 48 | AGND | P | Analog Ground |
| 21 | SD | DI | Serial Data Input | 45 | TP0 | AO | A/D Converter Input Monitor Pin (single-ended output) |
| 22 | SCLK | DI | Serial Data Shift Clock | 46 | V _{REF} | AIO | Reference Voltage Input/Output INT Ref: Bypass to GND with 0.1µF EXT Ref: Input Pin for Ref Voltage |
| 23 | V _{CC} | P | Analog Power Supply, +5V | 47 | V _{CC} | P | Analog Power Supply, +5V |
| 24 | OE | DI | Output Enable | 48 | REFN | AO | Lower-Level Reference |
| 25 | B0 (D0) LSB | DIO | A/D Output (Bit 0) and Register Data (D0) | | | | |
| 26 | B1 (D1) | DIO | A/D Output (Bit 1) and Register Data (D1) | | | | |
| 27 | B2 (D2) | DIO | A/D Output (Bit 2) and Register Data (D2) | | | | |
| 28 | B3 (D3) | DIO | A/D Output (Bit 3) and Register Data (D3) | | | | |

PIN CONFIGURATION

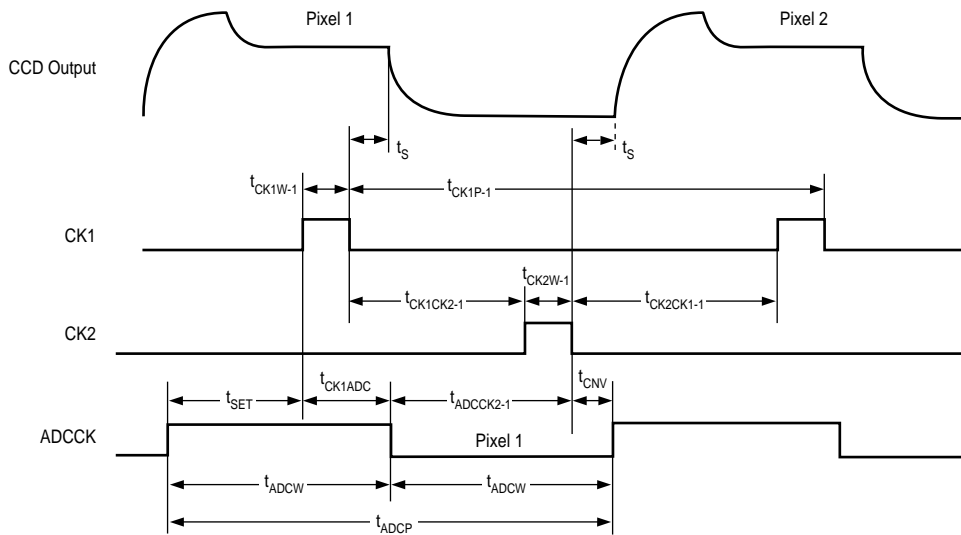


PIN DESCRIPTIONS (VSP3210Y)

| PIN | DESIGNATOR | TYPE | DESCRIPTION | PIN | DESIGNATOR | TYPE | DESCRIPTION |
|-----|-----------------|------|--|-----|------------------|------|---|
| 1 | CM | AO | Common-Mode Voltage | 30 | NC | - | Should Be Left OPEN |
| 2 | REFP | AO | Upper-Level Reference | 31 | B0 LSB | DO | A/D Output (Bit 0) LSB |
| 3 | AGND | P | Analog Ground | | B8 | DO | A/D Output (Bit 8) |
| 4 | AGND | P | Analog Ground | 32 | B1 | DO | A/D Output (Bit 1) |
| 5 | RINP | AI | Red Channel Analog Input | | B9 | DO | A/D Output (Bit 9) |
| 6 | AGND | P | Analog Ground | 33 | B2 | DO | A/D Output (Bit 2) |
| 7 | GINP | AI | Green Channel Analog Input | | B10 | DO | A/D Output (Bit 10) |
| 8 | AGND | P | Analog Ground | 34 | B3 | DO | A/D Output (Bit 3) |
| 9 | BINP | AI | Blue Channel Analog Input | | B11 | DO | A/D Output (Bit 11) |
| 10 | AGND | P | Analog Ground | 35 | B4 | DO | A/D Output (Bit 4) |
| 11 | V _{CC} | P | Analog Power Supply, +5V | | B12 | DO | A/D Output (Bit 12) |
| 12 | CLP | DI | Clamp Enable HIGH = Enable, LOW = Disable | 36 | B5 | DO | A/D Output (Bit 5) |
| 13 | V _{CC} | P | Analog Power Supply, +5V | | B13 | DO | A/D Output (Bit 13) |
| 14 | ADCK | DI | Clock for A/D Converter Digital Data Output | 37 | B6 | DO | A/D Output (Bit 6) |
| 15 | CK1 | DI | Sample Reference Clock | | B14 | DO | A/D Output (Bit 14) |
| 16 | CK2 | DI | Sample Data Clock | 38 | B7 | DO | A/D Output (Bit 7) |
| 17 | AGND | P | Analog Ground | | B15 MSB | DO | A/D Output (Bit 15) MSB |
| 18 | AGND | P | Analog Ground | 39 | NC | - | Should Be Left OPEN |
| 19 | WRT | DI | Write Signal for Registers | 40 | NC | - | Should Be Left OPEN |
| 20 | AGND | P | Analog Ground | 41 | V _{DRV} | P | Digital Output Driver Power Supply |
| 21 | SD | DI | Serial Data Input | 42 | V _{CC} | P | Analog Power Supply, +5V |
| 22 | SCLK | DI | Serial Data Shift Clock | 43 | V _{CC} | P | Analog Power Supply, +5V |
| 23 | V _{CC} | P | Analog Power Supply, +5V | 44 | AGND | P | Analog Ground |
| 24 | OE | DI | Output Enable | 45 | TP0 | AO | A/D Converter Input Monitor Pin (single-ended output) |
| 25 | NC | - | Should Be Left OPEN | 46 | V _{REF} | AIO | Reference Voltage Input/Output INT Ref: Bypass to GND with 0.1µF EXT Ref: Input Pin for Ref Voltage |
| 26 | NC | - | Should Be Left OPEN | 47 | V _{CC} | P | Analog Power Supply, +5V |
| 27 | NC | - | Should Be Left OPEN | 48 | REFN | AO | Lower-Level Reference |
| 28 | NC | - | Should Be Left OPEN | | | | |
| 29 | NC | - | Should Be Left OPEN | | | | |

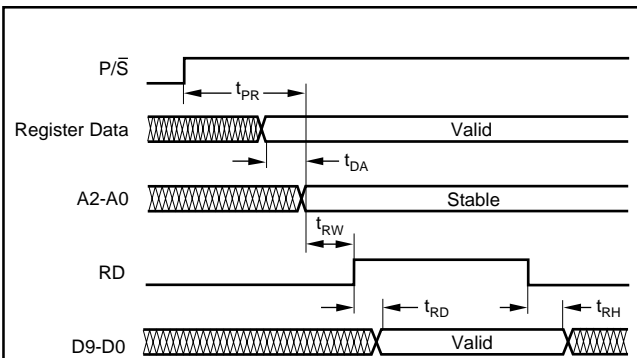
TIMING SPECIFICATIONS

VSP3200 AND VSP3210 1-CHANNEL CCD MODE TIMING



| SYMBOL | PARAMETER | MIN | TYP | MAX | UNITS |
|----------------|-------------------------------------|-----|-----------|-----|--------------|
| t_{CK1W-1} | CK1 Pulse Width | 20 | | | ns |
| t_{CK1P-1} | 1-Channel Mode Conversion Rate | 125 | 166 | | ns |
| t_{CK2W-1} | CK2 Pulse Width | 20 | | | ns |
| $t_{CK1CK2-1}$ | CK1 Falling to CK2 Rising | 15 | | | ns |
| $t_{CK2CK1-1}$ | CK2 Falling to CK1 Rising | 50 | | | ns |
| t_{CK1ADC} | CK1 Rising to ADCCK Falling | 10 | | | ns |
| $t_{ADCCK2-1}$ | ADCCK Falling to CK2 Falling | 15 | | | ns |
| t_{ADCW} | ADCCK Pulse Width | 62 | 83 | | ns |
| t_{ADCP} | ADCCK Period | 125 | 166 | | ns |
| t_s | Sampling Delay | 10 | | | ns |
| t_{SET} | ADCCK Rising to CK1 Rising | 40 | | | ns |
| t_{CNV} | Conversion Delay | 10 | | | ns |
| DL | Data Latency, Normal Operation Mode | | 8 (fixed) | | Clock Cycles |

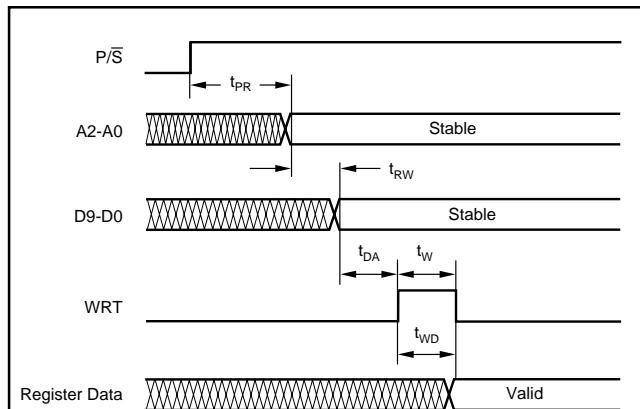
VSP3200 TIMING FOR PARALLEL PORT READING



| SYMBOL | PARAMETER | MIN | TYP | MAX | UNITS |
|----------|---------------------|-----|-----|-----|-------|
| t_{PR} | Parallel Ready Time | 20 | | | ns |
| t_{DA} | Data Setup Time | 30 | 50 | | ns |
| t_{RW} | Address Setup Time | 20 | 50 | | ns |
| t_{RD} | Read Out Delay | | | 20 | ns |
| t_{RH} | Data Hold Time | | | 1 | ns |

NOTES: (1) This feature is for the VSP3200 only. (2) Reading out register data through the serial port is prohibited.

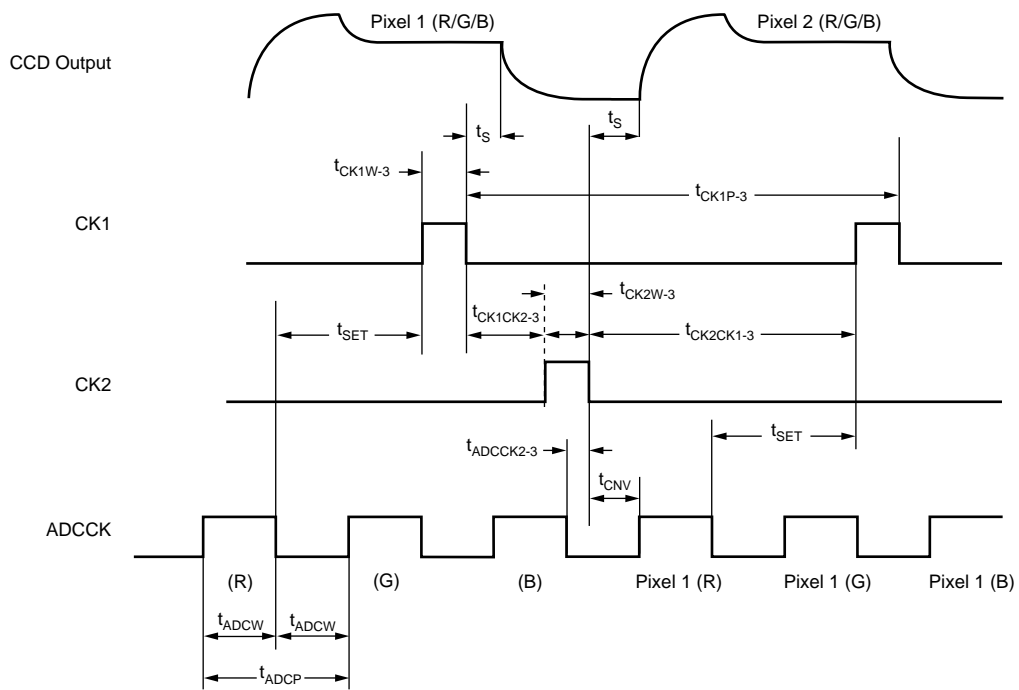
VSP3200 TIMING FOR PARALLEL PORT WRITING



| SYMBOL | PARAMETER | MIN | TYP | MAX | UNITS |
|----------|---------------------|-----|-----|-----|-------|
| t_{PR} | Parallel Ready Time | 20 | | | ns |
| t_W | WRT Pulse Width | 30 | 50 | | ns |
| t_{WD} | Data Valid Time | | | 30 | ns |
| t_{RW} | Address Setup Time | 20 | 50 | | ns |
| t_{DA} | Data Setup Time | 30 | 50 | | ns |

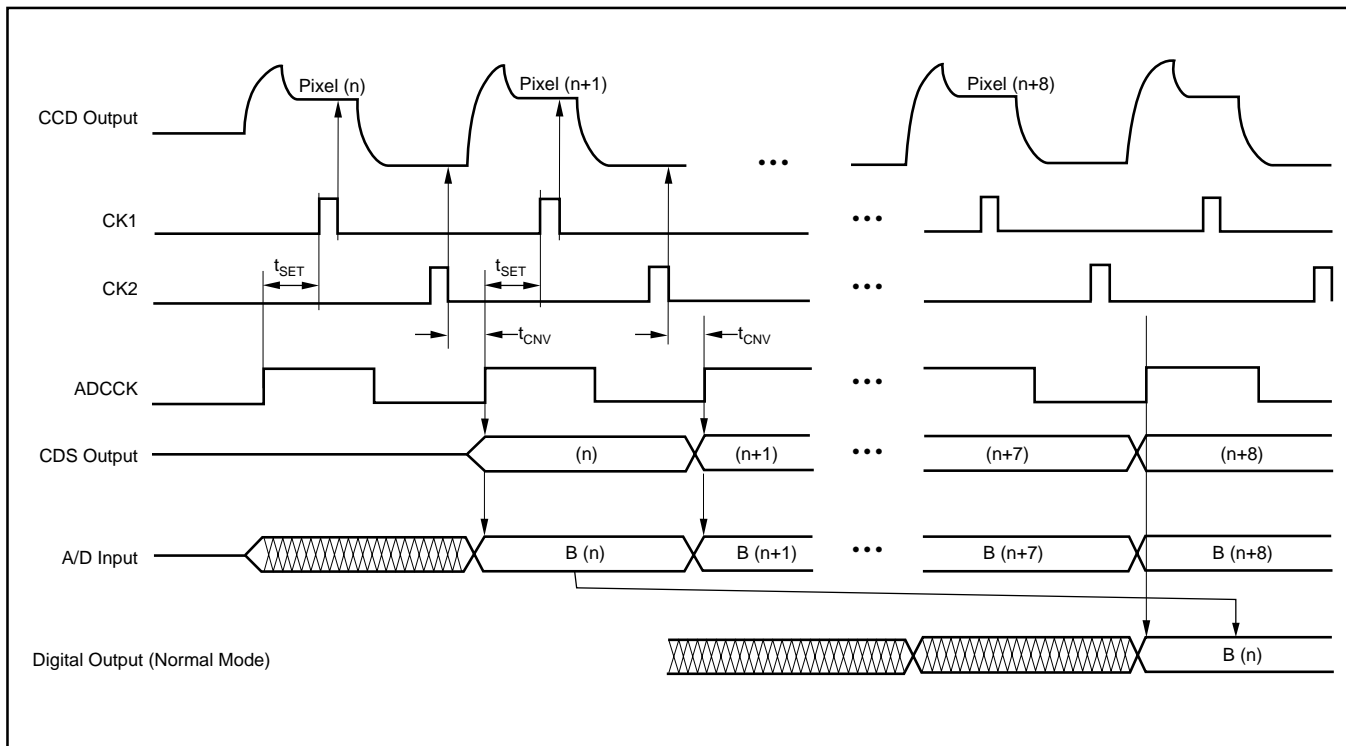
NOTE: (1) This feature is for the VSP3200 only.

VSP3200 AND VSP 3210 3-CHANNEL CCD MODE TIMING

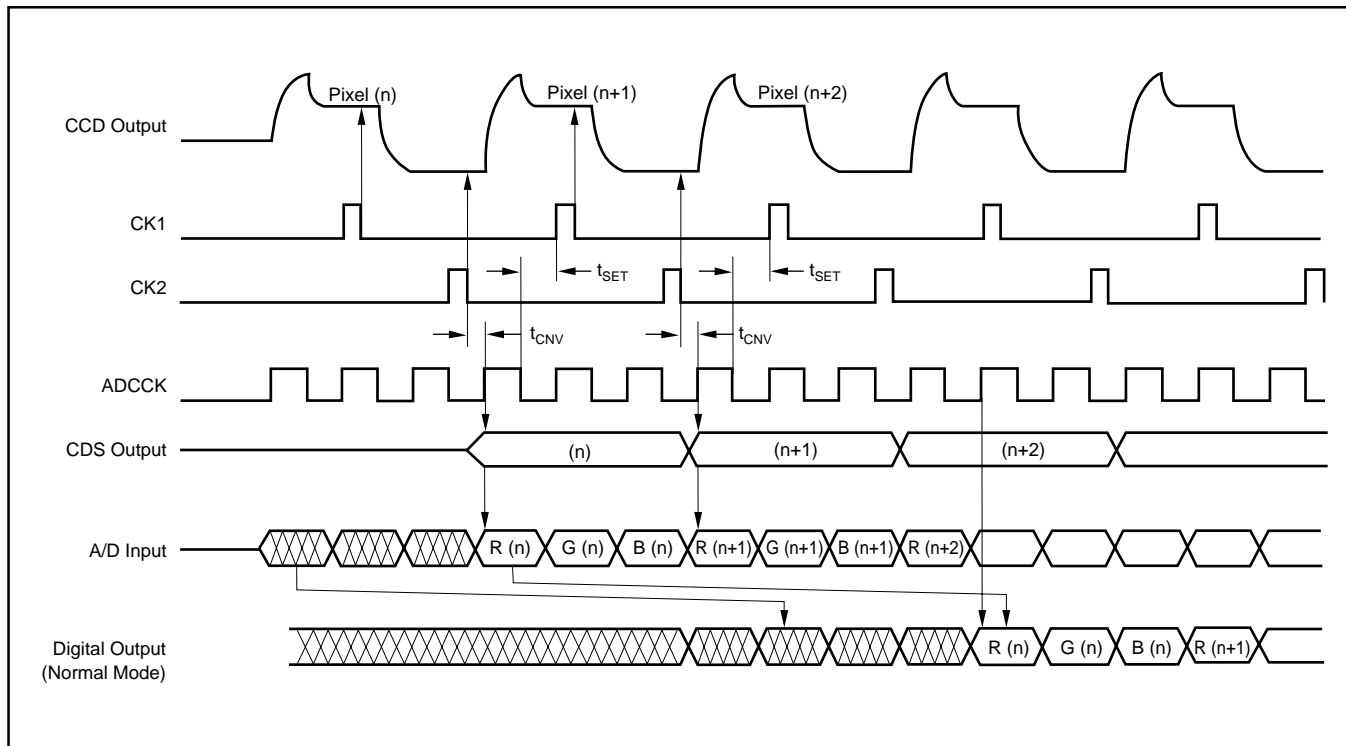


| SYMBOL | PARAMETER | MIN | TYP | MAX | UNITS |
|----------------|-------------------------------------|-----|-----------|-----|--------------|
| t_{CK1W-3} | CK1 Pulse Width | 20 | | | ns |
| t_{CK1P-3} | 3-Channel Mode Conversion Rate | 375 | 500 | | ns |
| t_{CK2W-3} | CK2 Pulse Width | 20 | | | ns |
| $t_{CK1CK2-3}$ | CK1 Falling to CK2 Rising | 15 | | | ns |
| $t_{CK2CK1-3}$ | CK2 Falling to CK1 Rising | 112 | | | ns |
| $t_{ADCCK2-3}$ | ADCCK Falling to CK2 Falling | 5 | | | ns |
| t_{ADCW} | ADCCK Pulse Width | 62 | 83 | | ns |
| t_{ADCP} | ADCCK Period | 125 | 166 | | ns |
| t_s | Sampling Delay | 10 | | | ns |
| t_{SET} | ADCCK Rising to CK1 Rising | 10 | | | ns |
| t_{CNV} | Conversion Delay | 40 | | | ns |
| DL | Data Latency, Normal Operation Mode | | 8 (fixed) | | Clock Cycles |

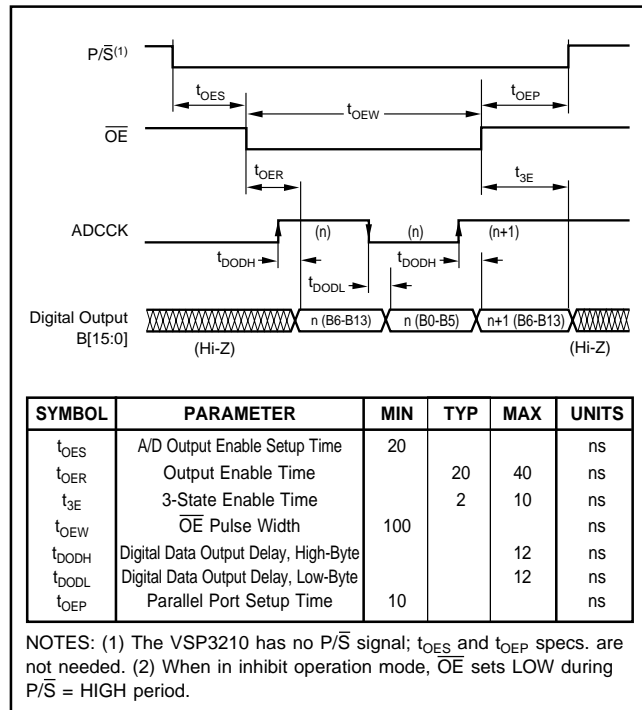
DIGITAL DATA OUTPUT SEQUENCE: 1-Ch CCD Mode, (B-Ch: D4 = 1 and D5 = 0)



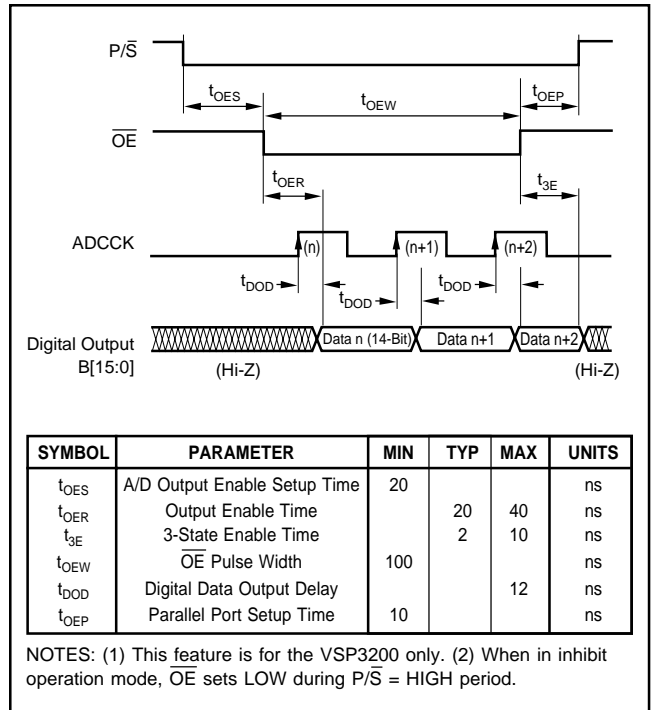
DIGITAL DATA OUTPUT SEQUENCE: 3-Ch CCD Mode, R > G > B Sequence



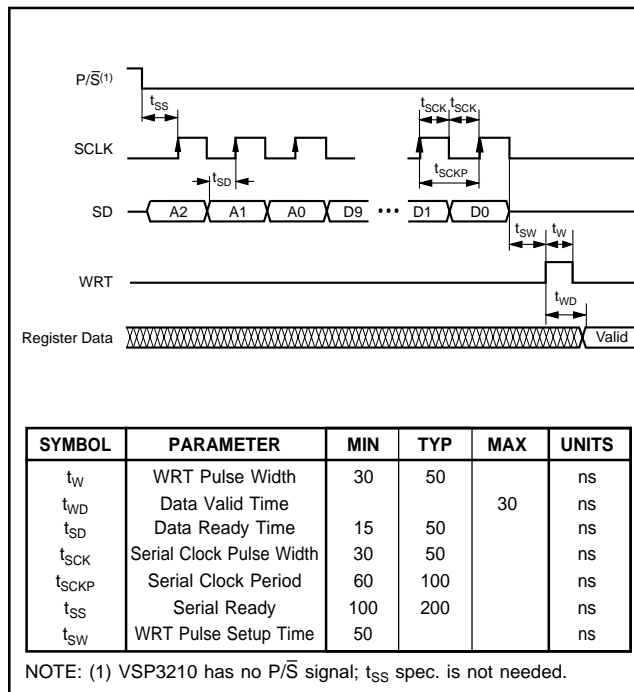
VSP3200 AND VSP3210 TIMING FOR DIGITAL DATA OUTPUT (DEMULTIPLEXED OUTPUT MODE)



VSP3200 TIMING FOR DIGITAL DATA OUTPUT (NORMAL OUTPUT MODE)



VSP3200 AND VSP3210 TIMING FOR SERIAL PORT WRITING



THEORY OF OPERATION

INTRODUCTION

The VSP3200 and VSP3210 are complete mixed-signal ICs that contain all of the key features associated with the processing of the CCD line sensor output signal in scanners, photo copiers, and similar applications. See the simplified block diagram on page 1 for details. The VSP3200 and VSP3210 include Correlated Double Samplers (CDSs), Programmable Gain Amplifiers (PGAs), Multiplexer (MUX), Analog-to-Digital (A/D) converter, input clamp, offset control, serial interface, timing control, and reference control generator.

The VSP3200 and VSP3210 can be operated in one of the following two modes:

- 1-Channel CCD mode
- 3-Channel CCD mode

1-CHANNEL CCD MODE

In this mode, the VSP3200 and VSP3210 process only one CCD signal (D3 of the Configuration Register sets to “1”). The CCD signal is AC-coupled to RINP, GINP, or BINP (depending on D4 and D5 of the Configuration Register). The CLP signal enables internal biasing circuitry to clamp this input to a proper voltage, so that internal CDS circuitry can work properly. The VSP3200 and VSP3210 inputs may be applied as DC-coupled inputs, which needs to be level-shifted to a proper DC level.

The CDS takes two samples of the incoming CCD signals: the CCD reset signal is taken on the falling edge of CK1, and the CCD information is taken on the falling edge of CK2. These two samples are then subtracted by the CDS and the result is stored as a CDS output.

In the 1-Channel CCD mode, only one of the three channels is enabled. Each channel consists of a 10-bit offset Digital-to-Analog Converter (DAC) with a range from -500mV to $+500\text{mV}$. A 3-to-1 analog MUX is inserted between the CDSs and a high-performance, 16-bit A/D converter. The outputs of the CDSs are then multiplexed to the A/D converter for digitization. The analog MUX is not cycling between channels in this mode. Instead, it is connected to a specific channel, depending on the contents of D4 and D5 in the Configuration Register.

The VSP3200 allows two types of output modes:

- Normal (D7 of Configuration Register sets to “0”).
- Demultiplexed (D7 of Configuration Register sets to “1”).

The VSP3210 allows one type of output mode:

- Demultiplexed (D7 of Configuration Register sets to “1”).

As specified in the “1-Channel CCD Mode” timing diagram, the rising edge of CK1 must be in the HIGH period of ADCCK, and at the same time, the falling edge of the CK2 must be in the LOW period of ADCCK. Otherwise, the VSP3200 and VSP3210 will not function properly.

3-CHANNEL CCD MODE

In the 3-Channel CCD mode, the VSP3200 and VSP3210 can simultaneously process triple output CCD signals. CCD signals are AC coupled to the RINP, GINP, and BINP inputs. The CLP signal enables internal biasing circuitry to clamp these inputs to a proper voltage so that internal CDS circuitry can work properly. The VSP3200 and VSP3210 inputs may be applied as DC-coupled inputs, which need to be level-shifted to a proper DC level.

The CDSs take two samples of the incoming CCD signals: the CCD reset signals are taken on the falling edge of CK1, and the CCD information is taken on the falling edge of CK2. These two samples are then subtracted by the CDSs and the results are stored as a CDS output.

In this mode, three CDSs are used to process three inputs simultaneously. Each channel consists of a 10-bit Offset DAC (range from -500mV to $+500\text{mV}$). A 3-to-1 analog MUX is inserted between the CDSs and a high-performance, 16-bit A/D converter. The outputs of the CDSs are then multiplexed to the A/D converter for digitization. The analog MUX is switched at the falling edge of CK2, and can be programmed to cycle between the Red, Green, and Blue channels. When D6 of the Configuration Register sets to “0”, the MUX sequence is Red > Green > Blue. When D6 of the Configuration Register sets to “1”, the MUX sequence is Blue > Green > Red.

MUX resets at the falling edge of CK1. In the case of a Red > Green > Blue sequence, it resets to “R”, and in the case of a Blue > Green > Red sequence, it resets to “B”.

The VSP3200 allows two types of output modes:

- Normal (D7 of Configuration Register sets to “0”).
- Demultiplexed (D7 of Configuration Register sets to “1”).

The VSP3210 allows one type of output mode:

- Demultiplexed (D7 of Configuration Register sets to “1”).

As specified in the “3-Channel CCD Mode” timing diagram, the falling edge of CK2 must be in the LOW period of ADCCK. If the falling edge of CK2 is in the HIGH period of ADCCK (in the timing diagram, ADCCK for sampling B-channel), the VSP3200 and VSP3210 will not function properly.

DIGITAL OUTPUT FORMAT

See Table I for the Digital Output Format. The VSP3200 and VSP3210 can be operated in one of the following two digital output modes:

- Normal output.
- Demultiplexed (B15-based Big Endian Format).

In Normal mode, the VSP3200 outputs the 16-bit data by B0 (pin 25) through B15 (pin 40) simultaneously.

In Demultiplexed mode, the VSP3200 outputs the high byte (upper 8 bits) by B8 (pin 33) through B15 (pin 40) at the rising edge of ADCCK HIGH, then outputs the low byte (lower 8 bits) by B8 (pin 33) through B15 (pin 40) at the falling edge of ADCCK.

The VSP3210 can be operated in Demultiplexed mode as the digital output (B13-based Big Endian Format), as shown in Table I. The VSP3210 outputs the high byte (upper 8 bits) by pin 31 through pin 38 at the rising edge of ADCCK HIGH, then outputs the low byte (lower 8 bits) by pin 31 through pin 38 at the falling edge of ADCCK (as shown in Table II). An 8-bit interface can be used between the VSP3200 and the Digital Signal Processor, allowing for a low-cost system solution.

DIGITAL OUTPUTS

The digital outputs of the VSP3200 and VSP3210 are designed to be compatible with both high-speed TTL and CMOS logic families. The driver stage of the digital outputs is supplied through a separate supply pin, V_{DRV} (pin 41), which is not connected to the analog supply pins (V_{CC}). By adjusting the voltage on V_{DRV} , the digital output levels will vary respectively. Thus, it is possible to operate the VSP3200 and VSP3210 on +5V analog supplies while interfacing the digital outputs to 3V logic. It is recommended to keep the capacitive loading on the data lines as low as possible (typically less than 15pF). Larger capacitive loads demanding higher charging current surges can feed back to the analog portion of the VSP3200 and VSP3210 and influence the performance. If necessary, external buffers or latches may be used, providing the added benefit of isolating the

VSP3200 and VSP3210 from any digital noise activities on the bus coupling back high-frequency noise. In addition, resistors in series with each data line may help minimize the surge current. Their use depends on the capacitive loading seen by the converter. As the output levels change from LOW to HIGH and HIGH to LOW, values in the range of 100Ω to 200Ω will limit the instantaneous current the output stage has to provide for recharging the parasitic capacitances.

PROGRAMMABLE GAIN AMPLIFIER (PGA)

The VSP3200 and VSP3210 have one PGA which is inserted between the CDSs and the 3:1 MUX. The PGA is controlled by a 6-bit of Gain Register; each channel (Red, Green, and Blue) has its own Gain Register.

The gain varies from 1 to 4.8 (0dB to 14dB), and the curve has log characteristics. Gain Register Code all “0” corresponds to minimum gain, and Code all “1” corresponds to maximum gain.

The transfer function of the PGA is:

$$\text{Gain} = 80 / (80 - GC)$$

where, GC is the integer representation of the 6-bit PGA gain register.

Figure 1 shows the PGA transfer function plots.

| PIN | 40 | 39 | 38 | 37 | 36 | 35 | 34 | 33 | 32 | 31 | 30 | 29 | 28 | 27 | 26 | 25 |
|-----------|-----|-----|-----|-----|-----|-----|----|----|-----|-----|-----|-----|-----|-----|-----|-----|
| High Byte | B15 | B14 | B13 | B13 | B11 | B10 | B9 | B8 | Low | Low | Low | Low | Low | Low | Low | Low |
| Low Byte | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 | Low | Low | Low | Low | Low | Low | Low | Low |

TABLE I. Output Format for VSP3200 (Demultiplexed Mode).

| PIN | 40 | 39 | 38 | 37 | 36 | 35 | 34 | 33 | 32 | 31 | 30 | 29 | 28 | 27 | 26 | 25 |
|-----------|----|----|-----|-----|-----|-----|-----|-----|----|----|----|----|----|----|----|----|
| High Byte | – | – | B15 | B14 | B13 | B12 | B11 | B10 | B9 | B8 | – | – | – | – | – | – |
| Low Byte | – | – | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 | – | – | – | – | – | – |

TABLE II. Output Format for VSP3210.

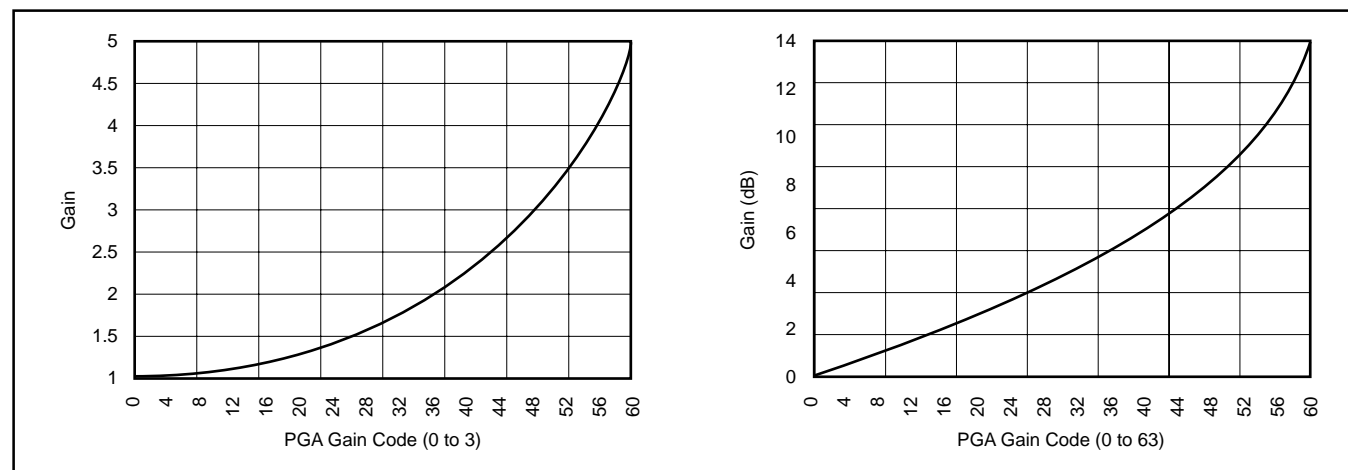


FIGURE 1. PGA Transfer Function Plots.

INPUT CLAMP

The input clamp should be used for 1-Channel and 3-Channel CCD mode, and enabled when both CLP and CK1 are set to HIGH.

Bit Clamp: the input clamp is always enabled.

Line Clamp: enables during the dummy pixel interval at every horizontal line, and disables during the effective pixel interval.

Generally, “Bit Clamp” is used for many scanner applications, however “Line Clamp” is used instead of “Bit Clamp” when the clamp noise is impressive.

CHOOSING THE AC INPUT COUPLING CAPACITORS

The purpose of the Input Coupling Capacitor is to isolate the DC offset of the CCD array from affecting the VSP3200 and VSP3210 input circuitry. The internal clamping circuitry is used to restore the necessary DC bias to make the VSP3200 and VSP3210 input circuitry functional. Internal clamp voltage, V_{CLAMP} , is set when both the CLP pin and CK1 are set HIGH. V_{CLAMP} changes depending on the value of V_{REF} . V_{CLAMP} is 2.5V if V_{REF} is set to 1V (D1 of the Configuration Register set to “0”), and V_{CLAMP} is 3V if V_{REF} is set to 1.5V (D1 of the Configuration Register set to “1”).

There are many factors that decide what size of Input Coupling Capacitor is needed. Those factors are CCD signal swing, voltage difference between the Input Coupling Capacitor, leakage current of the VSP3200 and VSP3210 input circuitry, and the time period of CK1.

Figure 2 shows the equivalent circuit of the VSP3200 and VSP3210 inputs.

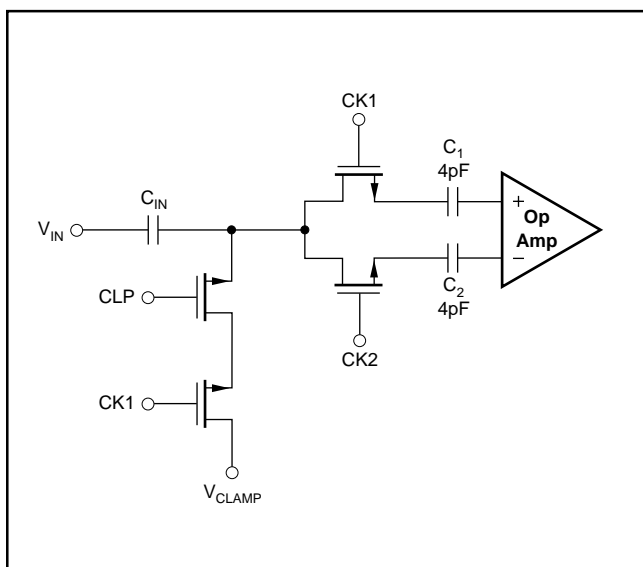


FIGURE 2. Equivalent Circuit of VSP3200 and VSP3210 Inputs.

In this equivalent circuit, Input Coupling Capacitor C_{IN} , and Sampling Capacitor C_1 , are constructed as a capacitor divider during CK1. For AC analysis, OP inputs are grounded. Therefore, the sampling voltage, V_S , during CK1 is:

$$V_S = (C_{IN}/(C_{IN} + C_1)) \cdot V_{IN}$$

From the above equation, we know that a larger C_{IN} makes V_S close to V_{IN} . In other words, the input signal (V_{IN}) will not be attenuated if C_{IN} is large.

However, there is a disadvantage of using a large C_{IN} : it will take longer for the CLP signal to charge up C_{IN} so that the input circuitry of the VSP3200 and VSP3210 can work properly.

CHOOSING C_{MAX} AND C_{MIN}

As mentioned before, a large C_{IN} is better if there is enough time for the CLP signal to charge up C_{IN} so that the input circuitry of the VSP3200 and VSP3210 can work properly. Typically, 0.01 μ F to 0.1 μ F of C_{IN} can be used for most cases.

In order to optimize C_{IN} , the following two equations can be used to calculate the maximum (C_{MAX}) and minimum (C_{MIN}) values of C_{IN} :

$$C_{MAX} = (t_{CK1} \cdot N)/[R_{SW} \cdot \ln(V_D/V_{ERROR})]$$

where t_{CK1} is the time when both CK1 and CLP go HIGH, and N is the number of black pixels; R_{SW} is the switch resistance of the VSP3200 and VSP3210 (typically, driver impedance + 4k Ω); V_D is the droop voltage of C_{IN} ; V_{ERROR} is the voltage difference between V_S and V_{CLAMP} .

$$C_{MIN} = (I/V_{ERROR}) \cdot t$$

where I is the leakage current of the VSP3200 and VSP3210 input circuitry (10nA is a typical number for this leakage current); t is the clamp pulse period.

SETTING FOR FULL-SCALE INPUT RANGE

The input range of the internal 16-bit A/D converter can be set in two ways:

- Internal reference: to set the internal reference mode, D2 of the configuration register must be set to “0” and the reference voltage set through D1. The full-scale input voltage setting is twice the reference voltage. When the reference voltage is set at 1V (D1 = “0”), the full-scale voltage is 2Vp-p. However, when the reference voltage is set at 1.5V (D1 = “1”), the full-scale voltage is 3Vp-p. In internal reference mode, V_{REF} should be connected to GND with a 0.1 μ F capacitor. Do not use V_{REF} voltages in

other system circuits, as it would affect the reference voltage of the A/D converter and prevent proper A/D conversion.

- External Reference: to set the external reference mode, D2 of the configuration register must be set to “1”. In external reference mode, V_{REF} operates as an analog voltage input pin. Inputting half the voltage necessary for the full-scale voltage range (e.g.: 1.7V applied for a necessary 3.4Vp-p input range), with a reference voltage range from 0.25V to 1.75V, will create the full-scale range. Thus, when V_{REF} is 0.5V, the full-scale range will be 0.5Vp-p, and when V_{REF} is 1.75V, the full-scale range will be 3.5Vp-p.

PROGRAMMING THE VSP3200 AND VSP3210

The VSP3200 and VSP3210 consist of three CCD channels and a 16-bit A/D. Each channel (Red, Green, and Blue) has its own 10-bit Offset and 6-bit Gain Adjustable Registers to be programmed by the user. There is also an 8-bit Configuration Register, on-chip, to program the different operation modes. Those registers are shown in Table III.

| ADDRESS A2 A1 A0 | REGISTER | POWER-ON DEFAULT VALUE |
|---------------------|--|---------------------------|
| 0 0 0 | Configuration Register (8-bit) | All “0s” |
| 0 0 1 | Red Channel Offset Register (10-bit) | All “0s” |
| 0 1 0 | Green Channel Offset Register (10-bit) | All “0s” |
| 0 1 1 | Blue Channel Offset Register (10-bit) | All “0s” |
| 1 0 0 | Red Channel Gain Register (6-bit) | All “0s” |
| 1 0 1 | Green Channel Gain Register (6-bit) | All “0s” |
| 1 1 0 | Blue Channel Gain Register (6-bit) | All “0s” |
| 1 1 1 | Reserved | |

TABLE III. On-Chip Registers.

These registers can be accessed by the following two programming modes:

- Parallel Programming Mode (VSP3200 only) using digital data output pins, with the data bus assigned as D0 to D9 (pins 25 to 34), and the address bus as A0 to A2 (pins 35 to 37). It can be used for both reading and writing operations. However, it cannot be used by the Demultiplexed mode (when D7 of the Configuration Register is set to “1”).
- Serial Programming Mode using a serial port, Serial Data (SD), the Serial Shift Clock (SCLK), and Write Signal (WRT) assigned.

It can be used only for writing operations; reading operations via the serial port are prohibited.

Table IV shows how to access these modes (VSP3200 only).

| \overline{OE} | P/\overline{S} | MODE |
|-----------------|------------------|---|
| 0 | 0 | Digital data output enabled, Serial mode enabled |
| 0 | 1 | Prohibit mode (can not set this mode) |
| 1 | 0 | Digital data output disabled, Serial mode enabled |
| 1 | 1 | Digital data output disabled, Parallel mode enabled |

TABLE IV. Access Mode for Serial and Parallel Port (VSP3200 Only).

CONFIGURATION REGISTER

The Configuration Register design is shown in Table V.

| BIT | LOGIC ‘0’ | LOGIC ‘1’ |
|-------------------|---------------------------------------|--|
| D0 | CCD mode | CIS mode |
| D1 | $V_{REF} = 1V$ | $V_{REF} = 1.5V$ |
| D2 | Internal Reference | External Reference |
| D3 | 3-channel Mode, D4 and D5 disabled | 1-channel Mode, D4 and D5 enabled |
| D4, D5 | (disabled when 3-channel) | D4 D5 0 0 1-channel mode, Red channel 0 1 1-channel mode, Green channel 1 0 1-channel mode, Blue channel |
| D6 | MUX Sequence Red > Green > Blue | MUX Sequence Blue > Green > Red |
| D7 ⁽¹⁾ | Normal output mode | Demultiplexed output mode |

NOTE: (1) D7 of the configuration register should always be set to “1” for the VSP3210. Power-on default value is “0”; initial write operation for “1” is also needed for the VSP3210, when in power-on.

TABLE V. Configuration Register Design.

Power-on default value is all “0s”, set to 3-Channel CCD mode with 1V internal reference, R > G > B MUX sequence, and normal output mode.

For reading/writing to the Configuration Register, the address will be A2 = “0”, A1 = “0”, and A0 = “0”.

For Example:

A 3-Channel CCD with internal reference $V_{REF} = 1V$ (2V full-scale input), R > G > B sequence and normal output mode will be D0 = “0”, D1 = “0”, D2 = “0”, D3 = “0”, D4 = “x (don’t care)”, D5 = “x (don’t care)”, D6 = “0”, and D7 = “0”.

For this example, bypass V_{REF} with an appropriate capacitor (e.g., 10 μ F to 0.1 μ F) when internal reference mode is used.

Another Example:

A 1-Channel CCD mode (Green channel) with an external 1.2V reference (2.4V full-scale input), Demultiplexed Output mode will be D0 = “0”, D1 = “x (don’t care)”, D2 = “1”, D3 = “1”, D4 = “0”, D5 = “1”, D6 = “x (don’t care)”, and D7 = “1”.

For this example, V_{REF} will be an input pin applied with 1.2V.

OFFSET REGISTER

Offset Registers control the analog offset input to channels prior to the PGA. There is a 10-bit Offset Register on each channel. The offset range varies from -500mV to $+500\text{mV}$. The Offset Register uses a straight binary code. All "0s" corresponds to -500mV , and all "1s" corresponds to $+500\text{mV}$ of the offset adjustment. The register code (200_{H}) corresponds to 0mV of the offset adjustment. The Power-on default value of the Offset Register is all "0s", so the offset adjustment should be set to -500mV .

PGA GAIN REGISTER

PGA Gain Registers control the gain to channels prior to the digitization by the A/D converter. There is a 6-bit PGA Gain Register on each channel. The gain range varies from 1 to 4.8 (from 0dB to 13dB). The PGA Gain Register is a straight binary code. All "0s" corresponds to an analog gain of 0dB , and all "1s" corresponds to an analog gain of 13dB . PGA Transfer function is log gain curve. Power-on default value is all "0s", so that it sets the gain of 0dB .

OFFSET AND GAIN CALIBRATION SEQUENCE

When the VSP3200 and VSP3210 are powered on, they will be initialized as 3-Channel CCDs, 1V internal reference mode (2V full-scale) with an analog gain of 1, and normal output mode. This mode is commonly used for CCD scanner applications. The calibration procedure is done at the very beginning of the scan.

To calibrate the VSP3200, use the following procedures:

- 1) Set the VSP3200 to the proper mode.
- 2) Set Offset to 0mV (control code: 00_{H}), and PGA gain to 1 (control code: 200_{H}).
- 3) Scan dark line.
- 4) Calculate the pixel offsets according to the A/D Converter output.
- 5) Readjust input Offset Registers.
- 6) Scan white line.
- 7) Calculate gain. It will be the A/D Converter full-scale divided by the A/D Converter output when the white line is scanned.
- 8) Set the Gain Register. If the A/D Converter output is not close to full-scale, go back to item 3. Otherwise, the calibration is done.

The calibration procedure is started at the very beginning of the scan. Once calibration is done, registers on the VSP3200 will keep this information (offset and gain for each channel) during the operation.

RECOMMENDATION FOR POWER SUPPLY, GROUNDING, AND DEVICE DECOUPLING

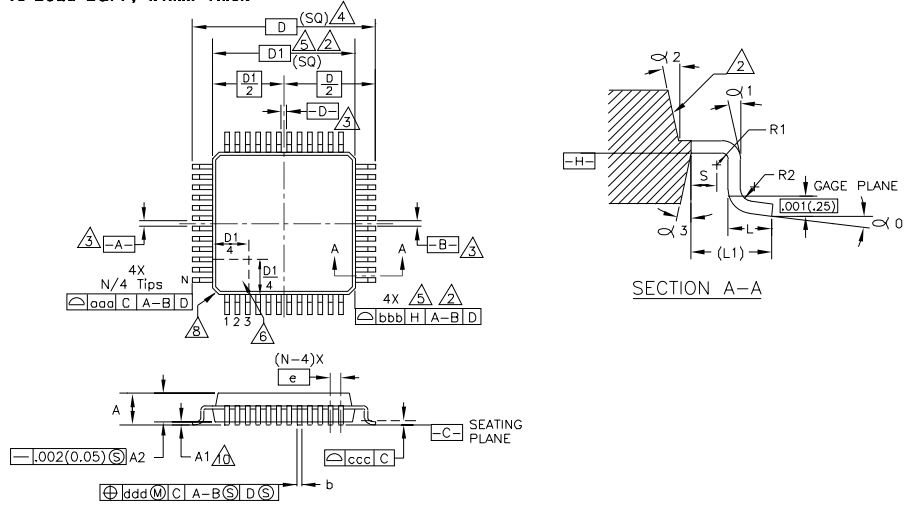
The VSP3200 and VSP3210 incorporate a very-high precision, high-speed A/D converter and analog circuitry vulnerable to any extraneous noise from the rails, etc. Therefore, it should be treated as an analog component and all supply pins, except V_{DRV} , should be powered by the only analog supply in the system. This will ensure the most consistent results, since digital power lines often carry high levels of wideband noise that otherwise would be coupled into the device and degrade the achievable performance.

Proper grounding, bypassing, short lead length, and the use of ground planes are particularly important for high-frequency designs. Multilayer PC boards are recommended for the best performance since they offer distinct advantages such as minimization of ground impedance, separation of signal layers by ground layers, etc.

It is recommended that all ground pins of the VSP3200 and VSP3210 be joined together at the IC and connected only to the analog ground of the system. The driver stage of the digital outputs ($B[15:0]$) is supplied through a dedicated supply pin, V_{DRV} , and should be completely separated from other supply pins with at least a ferrite bead. Keeping the capacitive loading on the output data lines as low as possible (typically less than 15pF) is also recommended. Larger capacitive loads demand higher charging current surges that can feed back into the analog portions of the VSP3200 and VSP3210, affecting device performance. If possible, external buffers or latches should be used, providing the added benefit of isolating the VSP3200 and VSP3210 from any digital noise activity on the data lines.

In addition, resistors in series with each data line may help minimize surge currents. Values in the range of 100Ω to 200Ω will limit the instantaneous current the output stage requires from recharging parasitic capacitances as output levels change from LOW to HIGH or HIGH to LOW. As the result of the high operation speed, the converter also generates high-frequency current transients and noises that are fed back into the supply and reference lines. This requires that the supply and reference pins be sufficiently bypassed. In most cases, $0.1\mu\text{F}$ ceramic chip capacitors are adequate in decoupling reference pins. Supply pins should be decoupled to the ground plane with a parallel combination of tantalum ($1\mu\text{F}$ to $22\mu\text{F}$) and ceramic ($0.1\mu\text{F}$) capacitors. Decoupling effectiveness largely depends upon the proximity to the individual pins.

Package Number 340 - 48-Lead LQFP, 1.4mm Thick



| DIM | INCHES | | MILLIMETERS | | NO | DIM | INCHES | | MILLIMETERS | | NO |
|-----|--------|-------|-------------|-------|-----|-----|--------|------|-------------|------|----|
| | MIN. | MAX. | MIN. | MAX. | | | MIN. | MAX. | MIN. | MAX. | |
| A | -- | .063 | -- | 1.60 | 10 | aaa | .008 | NOM. | 0.20 | NOM. | |
| A1 | .002 | .006 | 0.05 | 0.15 | 10 | bbb | .008 | NOM. | 0.20 | NOM. | |
| A2 | .053 | .057 | 1.35 | 1.45 | | ccc | .003 | NOM. | 0.08 | NOM. | |
| b | .007 | .011 | 0.17 | 0.27 | 7.9 | ddd | .003 | NOM. | 0.08 | NOM. | |
| C | .004 | .008 | 0.09 | 0.20 | 9 | α 0 | 0° | 7° | 0° | 7° | |
| D | .354 | BASIC | 9.00 | BASIC | 4 | α 1 | 0° | -- | 0° | -- | |
| D1 | .276 | BASIC | 7.00 | BASIC | 2.5 | α 2 | 11° | 13° | 11° | 13° | |
| e | .020 | BASIC | 0.50 | BASIC | | α 3 | 11° | 13° | 11° | 13° | |
| L1 | .018 | .030 | 0.45 | 0.75 | | | | | | | |
| L | .039 | REF | 1.00 | REF | | | | | | | |
| N | 48 | | 48 | | | | | | | | |
| R1 | .003 | -- | 0.08 | -- | | | | | | | |
| R2 | .003 | .008 | 0.08 | 0.20 | | | | | | | |
| S | .008 | -- | 0.20 | -- | | | | | | | |

NOTES:

- ALL DIMENSIONING AND TOLERANCING CONFORMS TO ANSI Y14.5M-1982.
- THE TOP PACKAGE BODY SIZE MAY BE SMALLER THAN THE BOTTOM PACKAGE BODY SIZE BY AS MUCH AS .006 in.(0.15mm).
- DATUMS [A-B] AND [D-] TO BE DETERMINED AT DATUM PLANE [-H-].
- TO BE DETERMINED AT SEATING PLANE [-C-].
- DIMENSION D1 DOES NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS .001 in.(0.25mm) PER SIDE. D1 IS THE MAXIMUM PLASTIC BODY SIZE DIMENSION INCLUDING MOLD MISMATCH.
- DETAILS OF PIN 1 IDENTIFIER ARE OPTIONAL BUT MUST BE LOCATED WITHIN THE ZONE INDICATED.
- DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION

SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE MAXIMUM b DIM. BY MORE THAN .003 in.(0.08mm). DAMBAR CAN NOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND AN ADJACENT LEAD IS .003 in.(0.07mm) FOR .016 in.(0.4mm) AND .020 in.(0.5mm) PITCH PACKAGES.

EXACT SHAPE OF EACH CORNER IS OPTIONAL.

9. DIMENSION b AND C APPLY TO THE FLAT SECTION OF LEAD BETWEEN .004 in.(0.10mm) AND .002 in.(0.25mm) FROM THE LEAD TIP.

A1 IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.

11. CONTROLLING DIMENSION IS MILLIMETER.

PACKAGE NUMBER: ZZ340 REV.: B
JEDEC NUMBER: MS-026-BBC

PACKAGING INFORMATION

| Orderable Device | Status ⁽¹⁾ | Package Type | Package Drawing | Pins | Package Qty | Eco Plan ⁽²⁾ | Lead/Ball Finish | MSL Peak Temp ⁽³⁾ |
|------------------|-----------------------|--------------|-----------------|------|-------------|-------------------------|------------------|------------------------------|
| VSP3200Y | NRND | LQFP | PT | 48 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| VSP3200YG4 | NRND | LQFP | PT | 48 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| VSP3210Y | ACTIVE | LQFP | PT | 48 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| VSP3210Y/2K | ACTIVE | LQFP | PT | 48 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| VSP3210Y/2KG4 | ACTIVE | LQFP | PT | 48 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| VSP3210YG4 | ACTIVE | LQFP | PT | 48 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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TAPE AND REEL INFORMATION



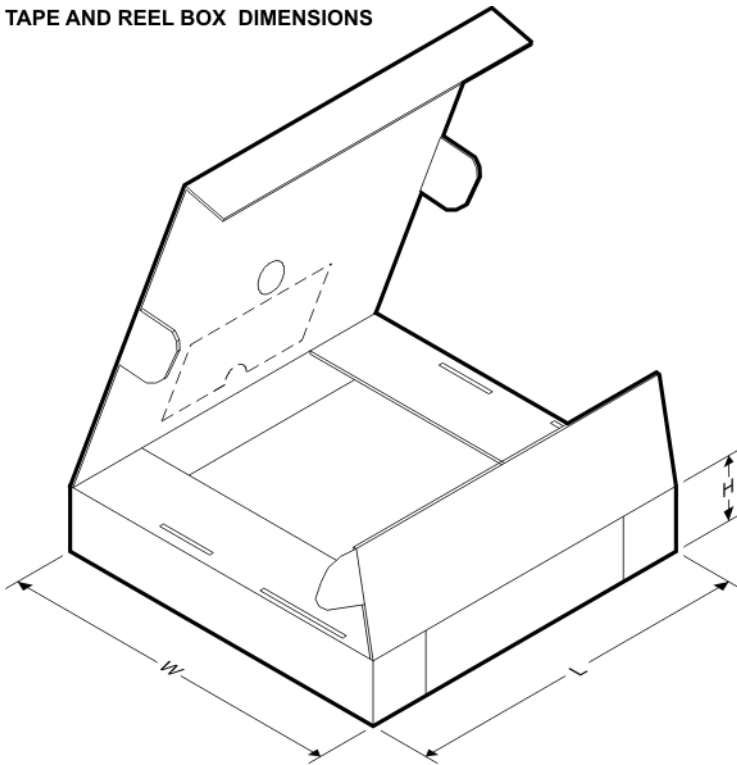
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|-------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| VSP3210Y/2K | LQFP | PT | 48 | 2000 | 330.0 | 17.4 | 9.5 | 9.5 | 2.0 | 12.0 | 16.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|-------------|--------------|-----------------|------|------|-------------|------------|-------------|
| VSP3210Y/2K | LQFP | PT | 48 | 2000 | 346.0 | 346.0 | 33.0 |

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