VSP1021
3-V, 10-BIT, 25-MSPS, LOW-POWER AREA CCD ANALOG FRONT END

features

- **10-Bit, 25-MSPS, Analog-to-Digital Converter (ADC)**
- **Single Power Supply Operation, 2.7 V to 3.3 V**
- **Low Power: 95 mW at 2.7 V, Power-Down Mode: 1 mW**
- **Full-Channel Differential-Nonlinearity Error: <±0.5 LSB Typical**
- **Full-Channel Integral-Nonlinearity Error: <±1.5 LSB Typical**
- **Dual Input Modes: CCD and Video**
- **Programmable-Gain Amplifier (PGA) With 0-dB to 36-dB Gain Range (0.047 dB/Step) for CCD Mode, 0-dB to 12-dB Gain Range (0.047 dB/Step) for Video Mode**

- **Serial Interface for Register Configuration**
- **Programmable Black-Level and Offset Calibration**
- **Analog Gain Implementation With Specified No Missing Code, Even At High Gains**
- **Additional Digital-to-Analog Converters (DACs) for External Analog Setting**
- **Internal Reference Voltages**
- **Programmable Internal-Timing Signal Delays**
- **48-Terminal TQFP Package**

applications

- **Digital Still Camera**
- **Digital Camcorder**
- **Digital Video Camera**

description

The VSP1021 device is a highly-integrated monolithic analog-signal processor/digitizer designed to interface the area charge-coupled-device (CCD) sensors in digital-camera and camcorder applications. The VSP1021 device performs all the analog processing functions necessary to maximize the dynamic range, corrects various errors associated with the CCD sensor, and then digitizes the results with an on-chip, high-speed ADC. The key components of the VSP1021 device include:

- Input clamp circuitry and a correlated double sampler (CDS)
- Programmable-gain amplifier (PGA) with 0-dB to 36-dB gain range for CCD mode and 0-dB to 12-dB range for video mode
- Two internal DACs for automatic or programmable optical-black-level and offset calibration
- 10-bit, 25-MSPS pipeline ADC for CCD mode and a 28-MSPS ADC for video mode
- Parallel data port for easy microprocessor interface and a serial port for configuring internal control registers
- Two additional DACs for external system control
- Internal reference voltages

The VSP1021 device is designed using advanced CMOS process and operates from a single 3-V power supply with a normal power consumption of just 95 mW, and 1 mW in power-down mode.

High throughput rate, single 3-V operation, very-low-power consumption, and fully-integrated analog-processing circuitry make the VSP1021 device an ideal CCD and video-signal-processing solution for electronic video-camcorder applications.

This device is available in a 48-terminal TQFP package and is specified over an operating temperature range of −20°C to 75°C.

AVAILABLE OPTIONS

T$_A$	PACKAGE TQFP (PFB)
−20°C to 75°C	VSP1021PFB

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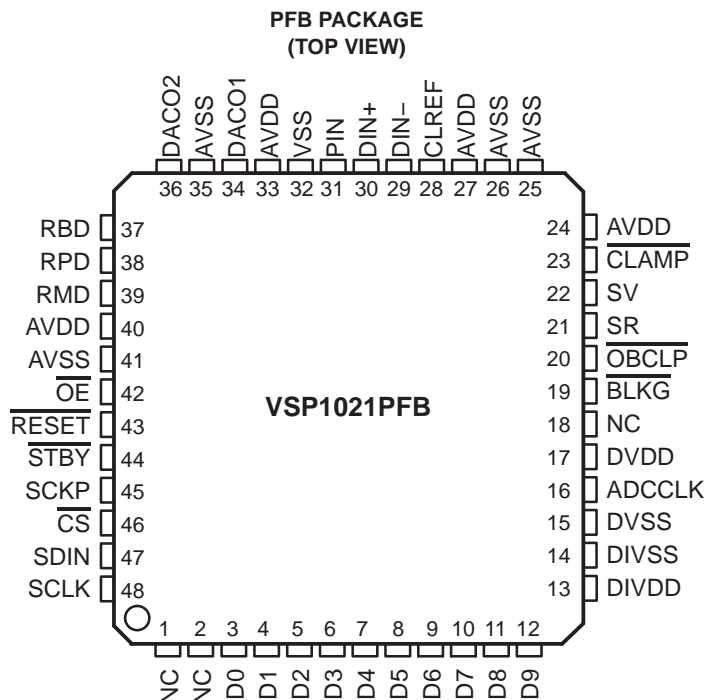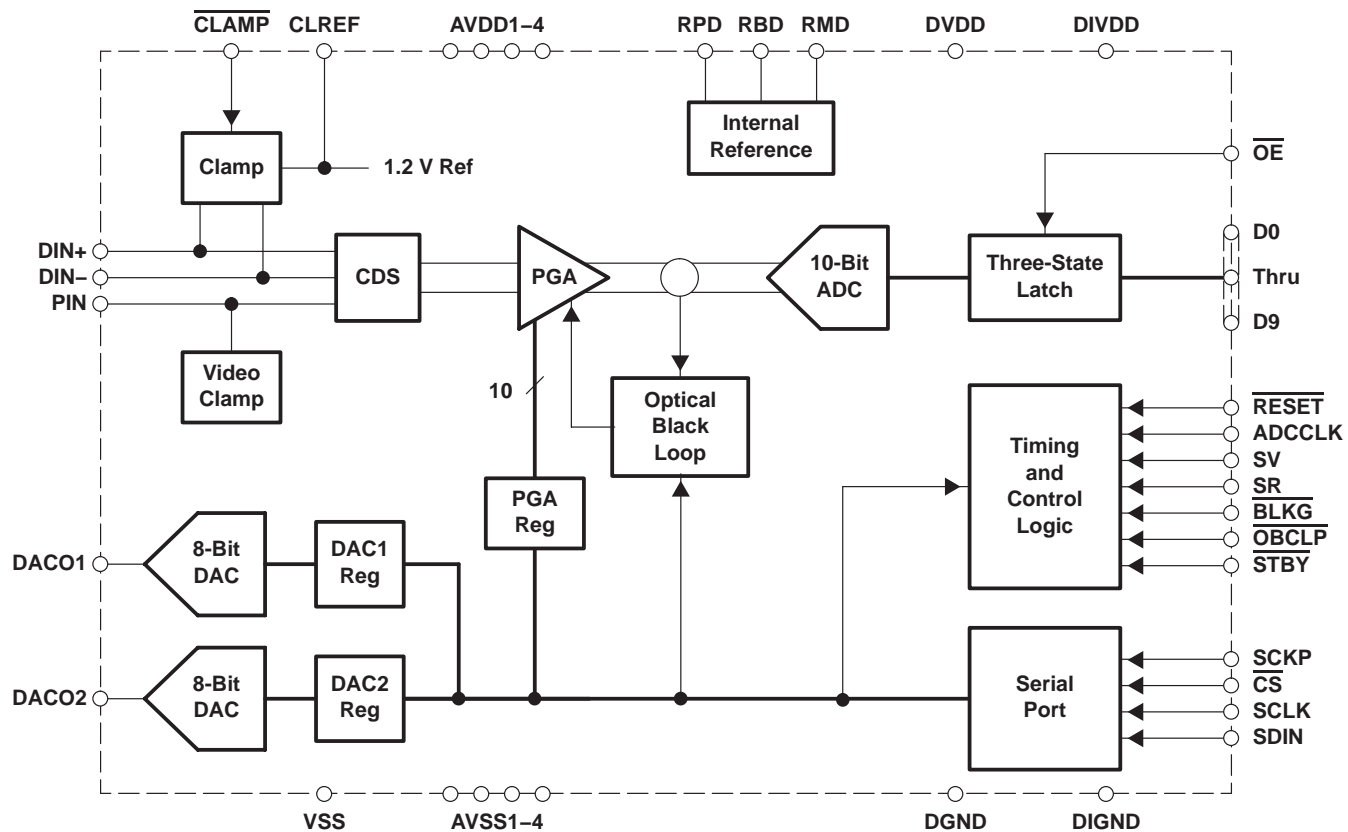**TEXAS INSTRUMENTS**

VSP1021
3-V, 10-BIT, 25-MSPS, LOW-POWER
AREA CCD ANALOG FRONT END

SLES016C– FEBRUARY 2002 – REVISED MARCH 2004

terminal assignments

PFB PACKAGE
(TOP VIEW)

Top pins (36–25): DACO2, AVSS, DACO1, AVDD, VSS, PIN, DIN+, DIN–, CLREF, AVDD, AVSS, AVSS

Left pins:
- 37 RBD
- 38 RPD
- 39 RMD
- 40 AVDD
- 41 AVSS
- 42 OE
- 43 RESET
- 44 STBY
- 45 SCKP
- 46 CS
- 47 SDIN
- 48 SCLK

Right pins:
- 24 AVDD
- 23 CLAMP
- 22 SV
- 21 SR
- 20 OBCLP
- 19 BLKG
- 18 NC
- 17 DVDD
- 16 ADCCLK
- 15 DVSS
- 14 DIVSS
- 13 DIVDD

Bottom pins (1–12): NC, NC, D0, D1, D2, D3, D4, D5, D6, D7, D8, D9

VSP1021PFB

functional block diagram

Terminal Functions

TERMINAL		TYPE	DESCRIPTION
NAME	NUMBER		
ADCCLK	16	I	ADC clock input
AVDD	24, 27, 33, 40		Analog-supply voltage, 3 V
AVSS	25, 26, 35, 41		Analog ground
$\overline{\text{BLKG}}$	19	I	Control input. The CDS operation is disabled when $\overline{\text{BLKG}}$ is pulled low.
$\overline{\text{CLAMP}}$	23	I	CCD signal clamp-control input
CLREF	28	O	Clamp reference-voltage output
$\overline{\text{CS}}$	46	I	Chip select. A logic low on this input enables the VSP1021 serial port.
DACO1	34	O	Digital-to-analog converter output 1
DACO2	36	O	Digital-to-analog converter output 2
DIN–	29	I	Negative input signal from CCD
DIN+	30	I	Positive input signal from CCD
DIVDD	13		Digital-interface-circuit supply voltage, 1.8 V to 3.6 V
DIVSS	14		Digital-interface-circuit ground
DVSS	15		Digital ground
DVDD	17		Digital-supply voltage, 3 V
D0–D9	3–12	O	10-bit, 3-state ADC output data or offset DACs test data
NC	1, 2, 18		Not connected
$\overline{\text{OBCLP}}$	20	I	Optical black-level and offset-calibration-control input, active low
$\overline{\text{OE}}$	42	I	Output data enable, active low
PIN	31	I	Video-input signal
RBD	37	O	Internal bandgap reference for external decoupling
$\overline{\text{RESET}}$	43	I	Hardware reset input, active low. This signal forces a reset of all internal registers.
RMD	39	O	Ref– output for external decoupling
RPD	38	O	Ref+ output for external decoupling
SCKP	45	I	This terminal selects the polarity of SCLK. 0 = SCLK stays high during idle period. The serial data is latched at the rising edge of SCLK. 1 = SCLK stays low during idle period. The serial data is latched at the falling edge of SCLK.
SCLK	48	I	Serial clock input. This clock synchronizes the serial-data transfer.
SDIN	47	I	Serial data input to configure the internal registers
SR	21	I	CCD reference-level sample-clock input
$\overline{\text{STBY}}$	44	I	Hardware power-down control input, active low
SV	22	I	CCD signal-level sample-clock input
VSS	32		Analog ground

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absolute maximum ratings over operating free-air temperature (unless otherwise noted)[†]

Supply voltage, AVDD, DVDD, DIVDD . . . . −0.3 V to 6.5 V
Analog input voltage range . . . . −0.3 V to AVDD+0.3 V
Digital input voltage range . . . . −0.3 V to DVDD+0.3 V
Operating virtual junction temperature range, T_J . . . . −40°C to 125°C
Operating free-air temperature range, T_A . . . . −20°C to 75°C
Storage temperature range, T_{stg} . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . 260°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and
functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not
implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

power supplies

PARAMETER	MIN	NOM	MAX	UNIT
Analog supply voltage, AVDD	2.7	3	3.3	V
Digital supply voltage, DVDD	2.7	3	3.3	V
Digital-interface supply voltage, DIVDD	1.8		3.6	V

digital inputs

PARAMETER	TEST CONDITIONS	MIN	NOM	MAX	UNIT
High-level input voltage, V_{IH}		0.8 DVDD			V
Low-level input voltage, V_{IL}				0.2 DVDD	V
Input ADCCLK frequency				25 (CCD)	MHz
				28 (Video)	
ADCCLK pulse duration, clock high, $t_{w(MCLKH)}$	DVDD = 3 V	20 (CCD)			ns
		17.9 (Video)			
ADCCLK pulse duration, clock low, $t_{w(MCLKL)}$		20 (CCD)			ns
		17.9 (Video)			
Input SCLK frequency				40	MHz
SCLK pulse duration, clock high, $t_{w(SCLKH)}$		12.5			ns
SCLK pulse duration, clock low, $t_{w(SCLKL)}$		12.5			ns

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electrical characteristics over recommended operating free-air temperature range, T_A = 25°C, AVDD = DVDD = 3 V, ADCCLK = 25 MHz (unless otherwise noted)

total device

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Device power consumption	AVDD = DVDD = 3 V		105		mW
Device power consumption	AVDD = DVDD = 2.7 V		95		mW
Power consumption in power-down mode			1		mW
Full-scale input span			1		V_{p-p}
Full-channel nonlinearity			0.5	1	LSB
No missing code			Assured		

analog-to-digital converter (ADC)

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
	ADC resolution			10 (CCD)		Bits
				8 (Video)		
INL	Integral nonlinearity	AVDD=DVDD= 2.7 V to 3.3 V		±1.2		LSB
DNL	Differential nonlinearity			±0.5	±0.99	
	Conversion rate			25 (CCD)		MHz
				28 (Video)		
	ADC output latency			5		CLK cycles
SNR	Input-referred signal-to-noise ratio	0-dB gain		65		dB
		36-dB gain		78		

correlated double sampler(CDS) and programmable-gain amplifier (PGA)

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
	CDS and PGA sample rate			25 (CCD)		MHz
				28 (Video)		
	CDS full-scale input span	Single-ended input			1	V
	Input capacitance of CDS			4		pF
	Minimum PGA gain			0		dB
Maximum PGA gain	CCD			36		dB
	Video			12		
	PGA gain resolution			0.047		dB
	PGA programming-code resolution	10-bit monotonic gain control		10		Bits

user digital-to-analog converter (DAC)

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
	DAC resolution			8		Bits
INL	Integral nonlinearity			±1		LSB
DNL	Differential nonlinearity			±0.5		LSB
	Output voltage range		0		AVDD	V
	Output settling time	10-pF external load, settle to 1 mV		4		µs

electrical characteristics over recommended operating free-air temperature range, T_A = 25°C, AVDD = DVDD = 3 V, ADCCLK = 25 MHz (unless otherwise noted) (continued)

reference voltages

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Internal bandgap-voltage reference		1.43	1.50	1.58	V
Temperature coefficient			100		ppm/°C
Voltage-reference noise			0.5		LSB
ADC Ref+	Externally decoupled		2		V
ADC Ref–	Externally decoupled		1		V

digital specifications

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Logic Inputs						
I_{IH}	High-level input current	DVDD = 3 V	–10		10	μA
I_{IL}	Low-level input current		–10		10	
C_i	Input capacitance			5		pF
Logic Outputs						
V_{OH}	High-level output voltage	I_{OH} = 50 μA, DIVDD = 3 V		DIVDD–0.4		V
V_{OL}	Low-level output voltage	I_{OL} = 50 μA, DIVDD = 3 V		0.4		V
I_{OZ}	High-impedance-state output current			±10		μA
C_O	Output capacitance			5		pF

key timing requirements

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{SRW}	SR pulse width	Measured at 50% of pulse height, recommend to use 1/4 of ADCCLK cycle	10			ns
t_{SVW}	SV pulse width	Measured at 50% of pulse height, recommend to use 1/4 of ADCCLK cycle	10			ns
t_{SRD}	Delay between the SR rising edge (SR active low) and the actual sampling instant	Measured at 50% of pulse height		5		ns
t_{SVD}	Delay between the SV falling edge (SV active low) and the actual instant of sampling the video signal	Measured at 50% of pulse height		8		ns
t_{ADC_SV}	Delay between the SV falling edge (SV active low) and the ADCCLK rising edge	Measured at 50% of pulse height		10		ns
t_{OD}	ADCCLK-to-output data delay	Measured at 50% of pulse height		6		ns
	Maximum internal delay for SR, SV, and ADCCLK timing signals	With 16 programmable delay steps		7.5		ns
	SR, SV, and ADCCLK delay resolution			0.5		ns
t_{CSF}	CS falling edge to SCLK rising edge when SCKP = 1, or CS falling edge to SCLK falling edge when SCKP = 0	Measured at 50% of pulse height	0			ns
t_{CSR}	SCLK falling edge to CS rising edge when SCKP = 1, or SCLK falling edge to CS falling edge when SCKP = 0	Measured at 50% of pulse height	5			ns

NOTE: t_{SRD}, t_{SVD}, and t_{ADC_SV} minimum requirements are measured while the registers for internal delay are programmed to 0.

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TYPICAL CHARACTERISTICS
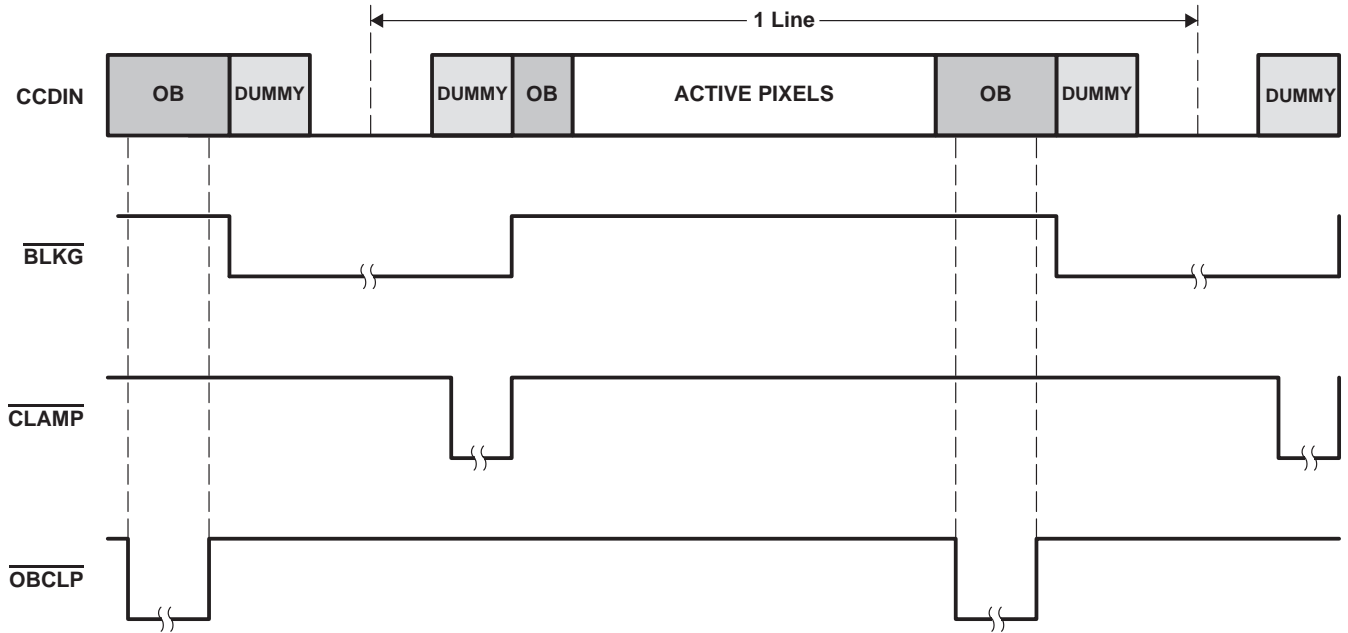
Figure 1. CCD Horizontal Synchronization Timing Diagram
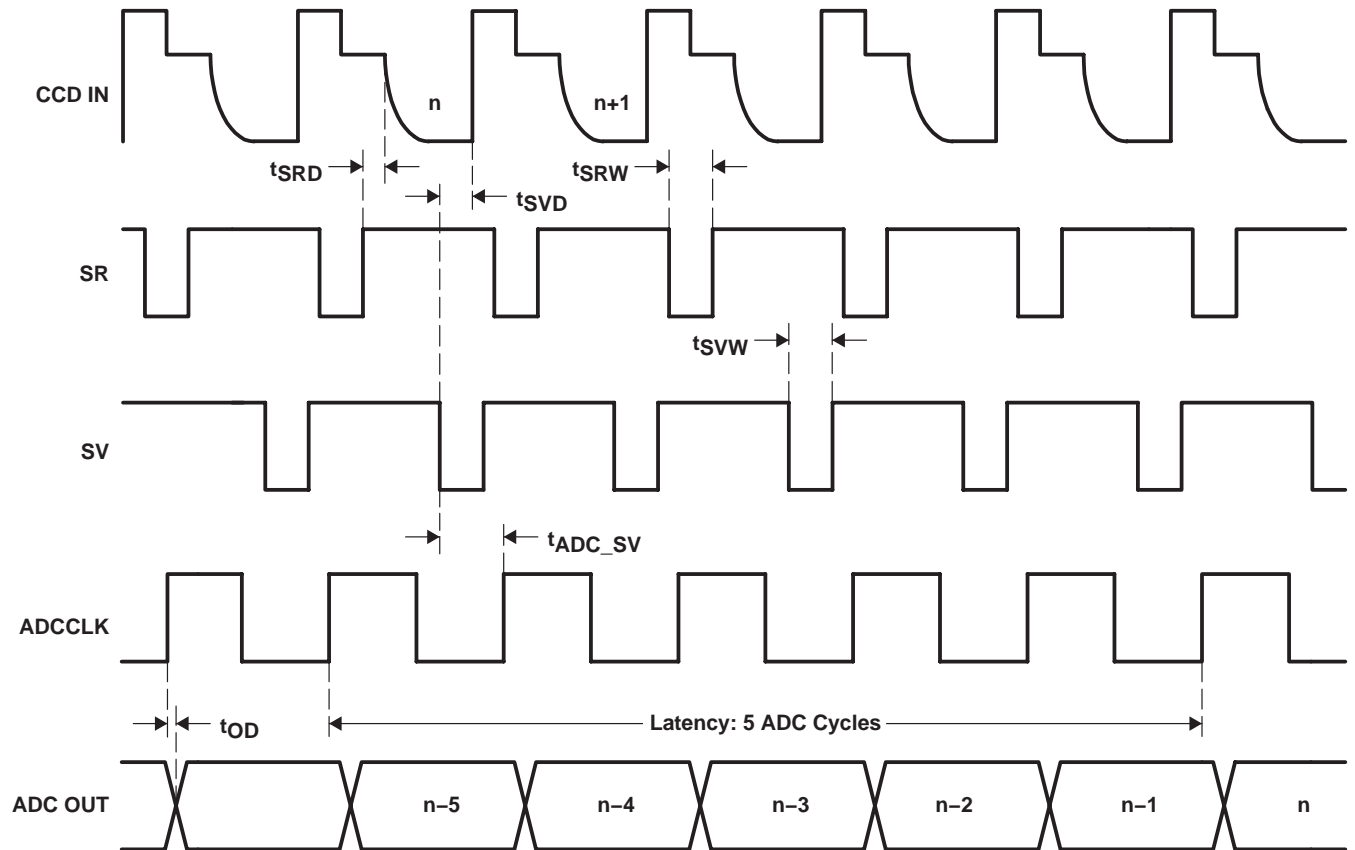
Figure 2. CCD Pixel Synchronization Timing Diagram

TYPICAL CHARACTERISTICS

SCKP Terminal Is Pulled Low

SCKP Terminal Is Pulled High
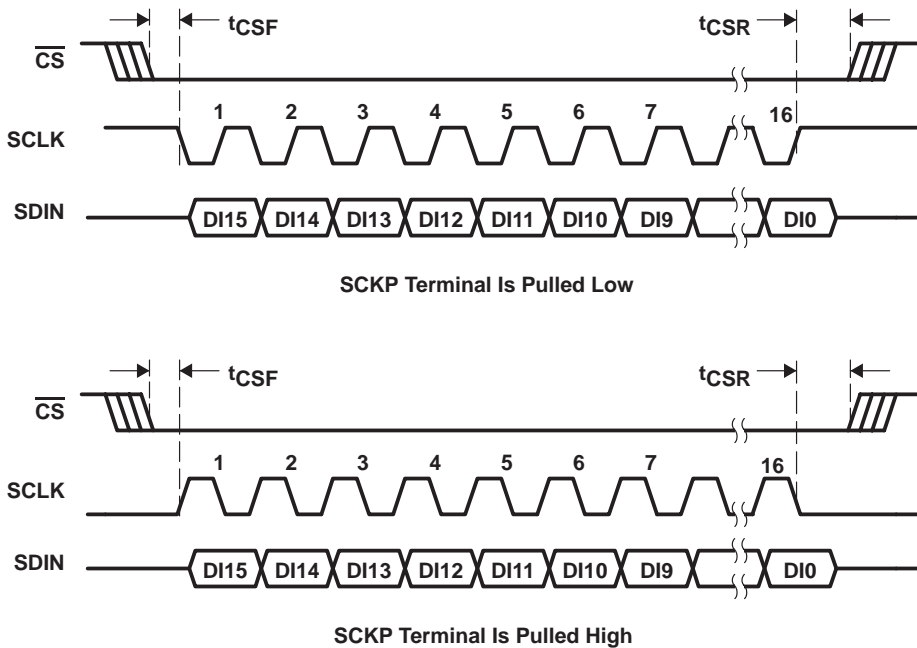
Figure 3. Serial Interface Timing Diagram

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APPLICATION INFORMATION
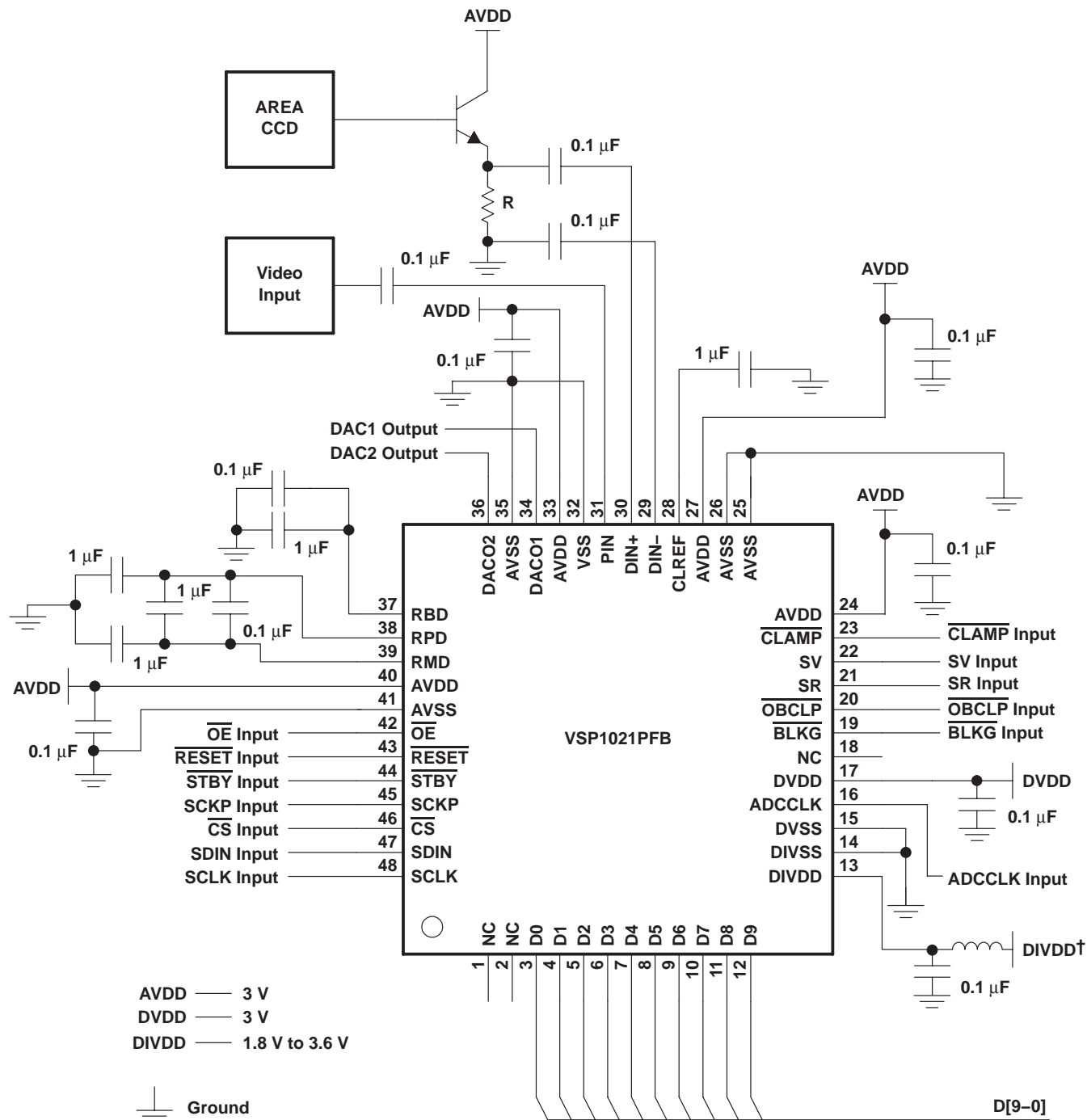
† DIVDD is recommended to have a ferrite bead to filter the power transients.
NOTE: All analog outputs should be buffered if the load is resistive or if the load is capacitive with more than 2 pF loading.
       The decoupling capacitors for the power supplies must be placed as close as possible to these terminals.

Figure 4. Typical Application Connection

REGISTER DEFINITION

serial input data format

DI15	DI14	DI13	DI12	DI11	DI10	DI9	DI8	DI7	DI6	DI5	DI4	DI3	DI2	DI1	DI0
X	X	A3	A2	A1	A0	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

A3	A2	A1	A0		D9–D0
0	0	0	0	Control register 1	10-bit data to be written into the selected register
0	0	0	1	PGA gain register	
0	0	1	0	User DAC1 register	
0	0	1	1	User DAC2 register	
0	1	0	0	SR/SV delay	
0	1	0	1	Optical-black Vb setup register	
0	1	1	0	Control register 2	

control register 1 format (00H)

D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
STBY	PDD2	PDD1	DACD	X	X	X	PSVR	X	RTSY

control register 1 description

BIT	NAME	DESCRIPTION
D9	STBY	Device global power-down control: 1 = Standby 0 = Active (default)
D8	PDD2	Power down the user DAC2: 0 = Active (default) 1 = Standby
D7	PDD1	Power down the user DAC1: 0 = Active (default) 1 = Standby
D6	DACD	Sustain the user DACs in global standby 0 = User DACs are in standby during global standby (default) 1 = User DACs are not in standby during global standby
D5	X	Reserved
D4	X	Reserved
D3	X	Reserved
D2	PSVR	This bit sets the polarity of the SV/SR. 0 = SV and SR are active low (default) 1 = SV and SR are active high
D1	X	Reserved
D0	RTSY	Writing 1 to this bit resets the entire system to the default settings (active high).

Default = 00 0000 0000

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REGISTER DEFINITION

PGA register format (01H)

D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0

Default PGA gain = 00 0000 0000 (0 dB)

NOTE: The gain-code range for CCD mode is 0–767, which covers the 0-dB to 36-dB range in 0.047-dB steps. Users must employ this code range. The gain stays at 36 dB when the code range is 768 to 1023. For the video mode, the gain code range is 256–512, which covers the 0-dB to 12-dB range in 0.047-dB steps. Users must employ a 256–512 code range for the video mode. In video mode, the gain code 0–255 must not be used. In video mode, the gain range is from 12 dB to 24 dB for the gain code range of 513 to 767; however, the offset might be too large for this gain range.

user DAC1 and DAC2 registers format (02H and 03H)

D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
X	X	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0

Default user DAC register value = 00 0000 0000

NOTE: The DAC1 and DAC2 codes range from 0 to 255, which covers the 0-to-AVDD output voltages at DACO1 and DACO2 output terminals with linear correspondence.

SV/SR delay register format (04H)

D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
X	X	SRL3	SRL2	SRL1	SRL0	SVL3	SVL2	SVL1	SVL0

SV/SR delay register description

BIT	NAME	DESCRIPTION
D9–D8	X	Reserved
D7–D4	SRL3–SRL0	These four bits set the internal SR delay. Set D7–D4 to 0 in video mode. **SRL3 SRL2 SRL1 SRL0 Typical internal delay** 0 0 0 0 0 ns (default) 0 0 0 1 0.5 ns ⋮ 1 1 1 1 7.5 ns
D3–D0	SVL3–SVL0	These four bits set the internal SV delay. Set D3–D0 to 0 in video mode. **SVL3 SVL2 SVL1 SVL0 Typical internal delay** 0 0 0 0 0 ns (default) 0 0 0 1 0.5 ns ⋮ 1 1 1 1 7.5 ns

Default SV/SR delay register value = 00 0000 0000

REGISTER DEFINITION

optical black Vb setup register format (05H)

D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
X	X	X	X	X	NOB	VB3	VB2	VB1	VB0

optical black Vb setup register description

BIT	NAME	DESCRIPTION
D9–D5	X	Reserved
D4	NOB	This bit controls the OB output. 0 = OB output is not affected by the Vb setting and it is always 0. 1 = OB output corresponds to the Vb setting (VB3–VB0).
D3–D0	VB3–VB0	**VB3** **VB2** **VB1** **VB0** **OB output (when NOB = 1)** 0 0 0 0 20 (default) 0 0 0 1 21 ⋮ ⋮ 1 1 1 1 35

Default optical black Vb setup register value = 00 0000 0000
NOTE: If NOB (D4) is set to 0, VB3–VB0 (D3–D0) has no effect. The output OB is 0.
         If NOB is set to 1, the output OB is defined by VB3–VB0, and ranges from 20 LSB to 35 LSB.

control register 2 format (06H)

D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
ADL3	ADL2	ADL1	ADL0	X	X	X	GNDV	MOD	X

control register 2 description

BIT	NAME	DESCRIPTION
D9–D6	ADL3–ADL0	These four bits set the internal ADCCLK delay. **ADL3** **ADL2** **ADL1** **ADL0** **Typical internal delay** 0 0 0 0 0 ns (default) 0 0 0 1 0.5 ns ⋮ ⋮ 1 1 1 1 7.5 ns
D5–D3	X	Reserved
D2	GNDV	This bit defines whether to short the video terminal (PIN) to ground (VSS) internally. 0 = No short (default) 1 = Short the video terminal to ground (VSS)
D1	MOD	This bit defines the mode of the input. 0 = CCD mode (default) 1 = Video mode
D0	X	Reserved. Always program this bit to 0.

Default register value = 00 0000 0000

PRINCIPLES OF OPERATION

CDS/PGA signal processor

In a CCD imaging system, the output from the CCD sensor is differentially fed to the correlated double sampler (CDS) of the VSP1021 device. The CCD signal is sampled and held during the reset reference interval and the video signal interval. By subtracting the two resulting voltage levels, the CDS removes low-frequency noise from the output of the CCD sensor and obtains the voltage difference between the CCD reference level and the video level of each pixel. Two sample/hold control pulses (SR and SV) are required to perform the CDS function.

The CCD output is capacitively coupled to the VSP1021 device. The $\overline{\text{CLAMP}}$ input clamps the ac-coupling capacitor to establish the proper dc bias during the dummy pixel interval. The bias at the input to the VSP1021 device is set to 1.2 V. Normally, $\overline{\text{CLAMP}}$ is applied at the sensor's line rate. A capacitor with a value ten times larger than that of the input ac-coupling capacitor should be connected between terminal 28 (CLREF) and AVSS.

The signal is sent to the PGA after completing the CDS function. The PGA gain can be adjusted from 0 to 36 dB by programming the internal gain register via the serial port. The PGA is digitally controlled with 10-bit resolution on a linear dB scale, resulting in a 0.047-dB gain step. The gain can be expressed by the following equation:

$$\text{Gain} = \text{PGA code} \times 0.047 \text{ dB}$$

where the PGA code has a range of 0 to 767.

For example, if the PGA code = 128, then the PGA Gain = 6 dB (a gain of 2).

In CCD mode, users must use the 0–767 range for the PGA-gain code. The gain stays at 36 dB when the code is from 768 to 1023.

video-mode operation

The VSP1021 device also provides an analog video processing channel that consists of an input clamp, a PGA, and an ADC. Setting bit D1 (MOD) to 1 in control register 2 enables the video channel. The video signal must be connected to terminal 31 (PIN) via a 0.1-μF capacitor as shown in Figure 4.

The video input has its own clamp circuit operated automatically. Around 60 LSB is added to balance the offset of the output with zero input.

The PGA gain in the video mode can be adjusted from 0 to 12 dB by programming the internal gain register via the serial port. The PGA is digitally controlled with 10-bit resolution on a linear dB scale, resulting in a 0.047-dB gain step. The gain can be expressed by the following equation,

$$\text{Gain} = (\text{PGA code} - 256) \times 0.047 \text{ dB}$$

where the PGA code has a range of 256 to 512.

For the video mode, users must utilize the 256 to 512 range for the PGA gain code. The gain code 0–255 must not be used, and the gain range is from 12 dB to 24 dB for the gain code range of 513 to 767; however, the offset might be too large for this gain range.

In the video mode, the internal SR and SV delays need to be set to 0.

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PRINCIPLES OF OPERATION

internal timing

As previously explained, the SR and SV signals are required to operate the CDS. Users need to synchronize the SR and SV clocks with the CCD signal waveform. The ADCCLK signal fine tunes the databus output in relation to the CDS timing to achieve optimal performance (see Figure 2).

The $\overline{\text{CLAMP}}$ signal activates the clamping circuit for the input signal. The $\overline{\text{OBCLP}}$ signal activates the optical-black calibration, and the active portion (the low pulse) of this signal must be within the optical-black period of the CCD (see Figure 1).

ADC

The ADC employs a pipelined architecture to achieve high throughput and low-power consumption. Fully-differential implementation and digital-error correction ensure 10-bit resolution.

The latency of the ADC data output is the default five ADCCLK cycles as shown in Figure 2. Pulling terminal 42 ($\overline{\text{OE}}$) high puts the ADC output in high impedance.

automatic optical black calibration

In the VSP1021 device, the optical black and the system channel offset corrections are performed by an automatic analog-feedback loop. During the optical-black-calibration interval ($\overline{\text{OBCLP}}$ = low) of each line, the optical-black pixels plus the channel offset are sampled and compared with the desired black level specified in the optical-black Vb setup register. The difference is then integrated and added to incoming pixel data at the PGA input. This analog feedback loop will calibrate the PGA output to the desired black pixel level, which can be programmed to either zero or from 20 LSBs to 35 LSBs in 1-LSB/step resolution via the serial port. The OB calibration settles within approximately 1000 OB pixels in order to avoid line noise.

input blanking function

During the blanking period of CCD operation, large input transients may occur at the VSP1021 input, making the ADC output unpredictable. Activating the $\overline{\text{BLKG}}$ pulse during this period will ensure a digital code of zero at the ADC output.

user DACs

The VSP1021 device includes two user DACs that can be utilized for external analog settings. The output voltage of each DAC can be independently set and has a range of 0 V to the supply voltage, with an 8-bit resolution. When the user DACs are not used in a camera system, they can be put in the standby mode by programming control bits in control register 1. The following table defines the status of the user DACs.

SOFTWARE/HARDWARE GLOBAL STANDBY	PDD1/PDD2	DACD	STATUS OF DAC1/DAC2
Active	0	x	Active
Active	1	x	Standby
Standby	0	0	Standby
Standby	0	1	Active
Standby	1	x	Standby

NOTE:
The hardware global standby is set by pulling down terminal 44 ($\overline{\text{STBY}}$) of the VSP1021 device. The software global standby is controlled by setting bit D9 (STBY) in control register 1 to 1.

![Texas Instruments logo]

PRINCIPLES OF OPERATION

three-wire serial interface

A simple three-wire (SCLK, SDIN, and $\overline{\text{CS}}$) serial interface is provided to allow writing to the internal registers of the VSP1021 device. Serial clock SCLK can be run at a maximum speed of 40 MHz. Serial data SDIN is 16 bits long. After 2 leading null bits, there are 4 address bits for which the internal register is to be updated; the following 10 bits are the data to be written to the register. Terminal 46 ($\overline{\text{CS}}$) must be held low to enable the serial port. The data transfer is initiated by the incoming SCLK after $\overline{\text{CS}}$ falls. Figure 3 shows the detailed timing for the serial interface.

The SCLK polarity is selected by pulling terminal 45 (SCKP) either high or low.

device reset

The device is not under the default configuration after power on. The registers are set to the default value by a reset. When terminal 43 ($\overline{\text{RESET}}$) is pulled low, all internal registers are set to their default values. In addition, the VSP1021 device has a software-reset function that resets the device when writing a control bit to control register 1.

See the *register definition* section for the register default values.

power-down mode (standby)

The VSP1021 device implements both hardware and software power-down modes. Pulling terminal 44 ($\overline{\text{STBY}}$) low puts the device in the low-power standby mode. The total power drops to about 1 mW. Setting a power-down control bit in the control register can also activate the power-down mode. Users can still program all internal registers during the power-down mode.

power supply

The VSP1021 device has several power-supply terminals. Each major internal analog block has a dedicated AVDD supply terminal. All internal digital circuitry is powered by DVDD. Both AVDD and DVDD are 3 V nominal.

Terminals 13 (DIVDD) and 14 (DIVSS) supply power to the output digital driver (D9–D0). DIVDD is independent of DVDD and can be operated from 1.8 V to 3.6 V. This allows the outputs to interface with digital ASICs requiring different supply voltages.

grounding and decoupling

General practices should apply to the printed-circuit-board (PCB) design to limit high-frequency transients and noise that feed back into the supply and reference lines. This requires sufficient bypass of the supply and reference terminals. In the case of power-supply decoupling, 0.1-μF ceramic chip capacitors are adequate to keep the impedance low over a wide frequency range. Recommended external decoupling for the three voltage-reference terminals is shown in Figure 4. Since the effectiveness of the decoupling capacitors depends largely on the proximity to the individual supply terminal, they must be placed as close as possible to these terminals. An inductor is recommended for the DIVDD power supply (see Figure 4). Common ground level is also recommended.

voltage references

An internal precision voltage reference of 1.5 V nominal is provided. This reference voltage generates the ADC Ref– voltage of 1 V and Ref+ of 2 V. It also generates the internal clamp voltage. All internally-generated voltages are fixed values and cannot be adjusted. Terminals 37 (RBD), 38 (RPD), and 39 (RMD) must not be used to drive any loads.

TEXAS INSTRUMENTS

PACKAGING INFORMATION

Orderable Device	Status [1]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [2]	Lead/Ball Finish	MSL Peak Temp [3]
VSP1021PFB	NRND	TQFP	PFB	48	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
VSP1021PFBG4	NRND	TQFP	PFB	48	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR

[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

[3] MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

PFB (S-PQFP-G48)   **PLASTIC QUAD FLATPACK**
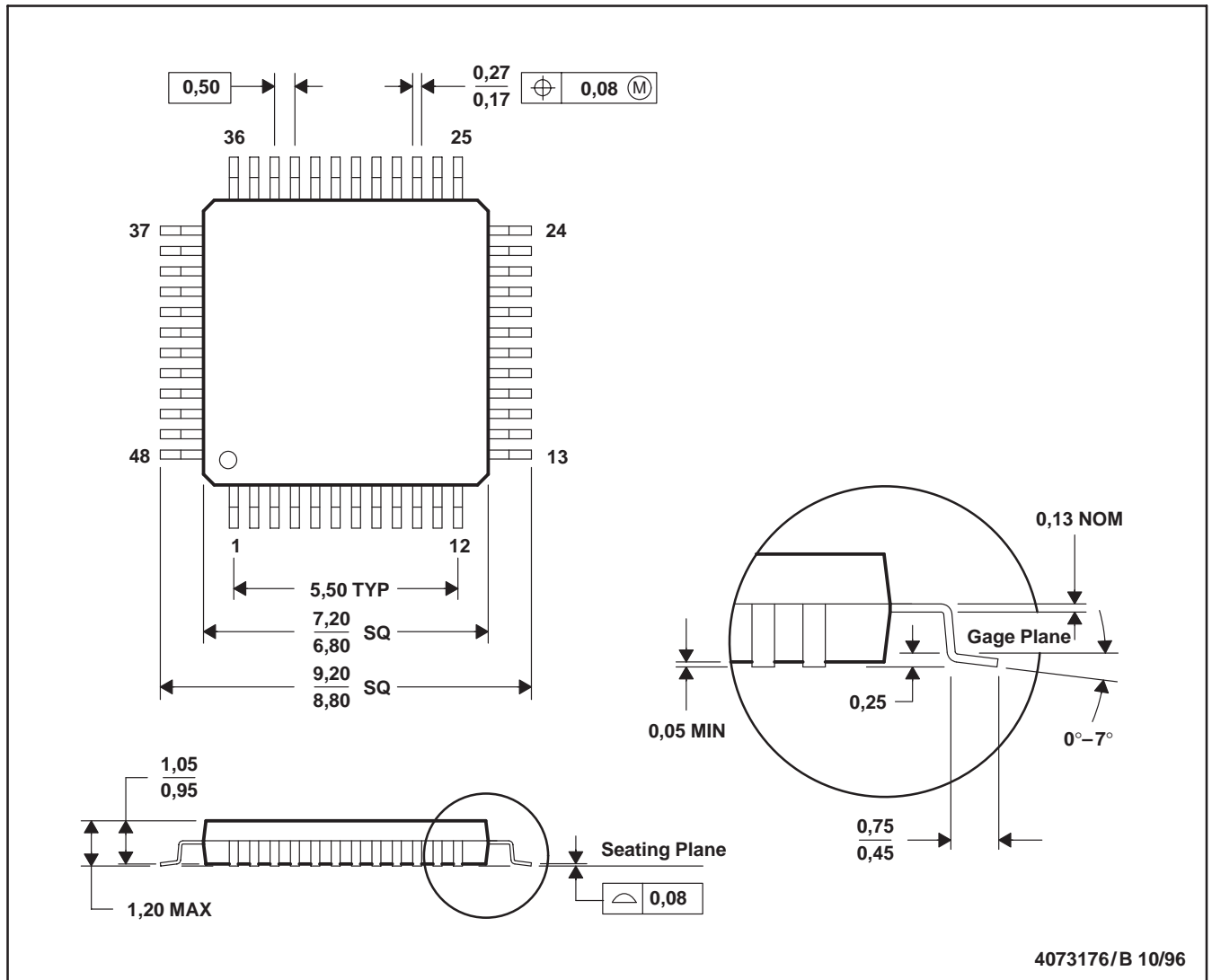
4073176 / B 10/96

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-026

TEXAS INSTRUMENTS

POST OFFICE BOX 655303 ● DALLAS, TEXAS 75265

PFB (S−PQFP−G48)

Example Board Layout
(Note C)

Example Stencil Design
(Note D)

0,5

0,25

0,5

1,35

8,5

8,5

8,5

8,5

Non Solder Mask Defined Pad

Example
Pad Geometry
(Note C)

0,3

1,4

0,05
All Around

Example
Solder Mask Opening
(Note E)

4209366/A 03/08

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC−7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC−7525.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

IMPORTANT NOTICE