Low-Power, High-Speed Buffer for CCD Sensor

Check for Samples: VSP1000

FEATURES

- **High Speed:**
  - **210 MHz, 3-dB Bandwidth**
- **Fast Settling Time**
- **Adjustable Active Load Current**
- **Adjustable Drive Strength**
- **Low Power: 20 mW**
- **Ultra-Small Package:**
  - **1-mm × 1-mm Ultra-Thin 0.35-mm QFN**

DESCRIPTION

The VSP1000 is a high-speed, low-noise, low-power, fast-settling, unity-gain buffer. It is specially designed for use between charge-coupled device (CCD) sensors and analog front-ends (AFEs). The device has an adjustable active load current that can load the CCD sensor output appropriately. The VSP1000 also features an adjustable output drive strength that can be set in accordance with the bandwidth requirements. At a 2-mA drive current, the device provides a bandwidth of 210 MHz, which allows for very low power operation with good performance. An ultra-small package of 1 mm × 1 mm and 0.35-mm height helps in saving printed circuit board (PCB) space and achieving a very low profile.

The VSP1000 is ideal for driving Texas Instruments AFEs for CCD sensors and, in general, any analog-to-digital converter (ADC) inputs. The adjustable load current allows for easy interfacing with a variety of CCD sensors from various manufacturers.

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PACKAGE/ORDERING INFORMATION(1)

PRODUCT	PACKAGE-LEAD	PACKAGE DESIGNATOR	SPECIFIED TEMPERATURE RANGE	PACKAGE MARKING	ORDERING NUMBER	TRANSPORT MEDIA, QUANTITY
VSP1000	QFN-6	DSF	0°C to +85°C	VSP1000DSF	VSP1000DSFT	Tape and Reel, 250
					VSP1000DSFR	Tape and Reel, 5000

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or visit the device product folder at www.ti.com.

ABSOLUTE MAXIMUM RATINGS(1)

Over free-air temperature range, unless otherwise noted.

		VSP1000	UNIT
Supply voltage	VCC	20.0	V
Input voltage		–0.3 to VCC + 0.3	V
Input current	Any pin except supplies	±10	mA
Ambient temperature under bias		–25 to +85	°C
Storage temperature		–55 to +125	°C
Junction temperature		+150	°C
Package temperature (IR reflow, peak)		+250	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

All specifications at T_A = +25°C, V_{CC} = 13 V, R_{IDRV} = 90 kΩ, and C_{LOAD} = 22 pF, unless otherwise noted.

PARAMETER		TEST CONDITIONS	VSP1000			UNIT
			MIN	TYP	MAX	
POWER SUPPLY						
V_{CC}	Supply voltage		10	13	16	V
I_{CC}	Supply current			2		mA
DYNAMIC PERFORMANCE						
	Gain	1-MHz, 200-mV_{PP} input		0.999		ns
	Rise time	V_{IN} = 7.5 V to 8.5 V		5		ns
	Fall time	V_{IN} = 8.5 V to 7.5 V		6		ns
	I/O delay time	V_{IN} = 7.5 V to 8.5 V		1.28		ns
	–3-dB bandwidth	100-mV_{PP} input		210		MHz
V_{IN}	Input voltage range	V_{CC} = 13 V	1.5		10.5	V
T_A	Operating free-air temperature		0		+85	°C

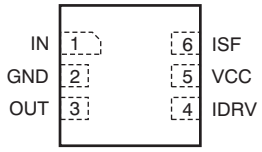
THERMAL INFORMATION

THERMAL METRIC(1)		VSP1000 DSF 6 PINS	UNITS
θ_{JA}	Junction-to-ambient thermal resistance	333.2	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance	56.9	
θ_{JB}	Junction-to-board thermal resistance	239	
ψ_{JT}	Junction-to-top characterization parameter	13.9	
ψ_{JB}	Junction-to-board characterization parameter	236	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance	202	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

PIN CONFIGURATION

DSF PACKAGE
1-mm × 1-mm × 0.35-mm QFN-6
(TOP VIEW)



PIN ASSIGNMENTS

PIN NAME	PIN NUMBER	TYPE	DESCRIPTION
IN	1	Analog input	Input terminal; connect this pin to the sensor output
VEE	2	Ground	Negative supply terminal; must be connected to ground
OUT	3	Analog output	Output terminal; connect this pin to the AFE input
IDRV	4	Analog input	Drive current adjustment; refer to the application diagram for further details
VCC	5	Power	Positive supply terminal; must be decoupled to the VEE terminal with a 0.1-µF capacitor
ISF	6	Analog input	Sink current adjustment; refer to the application diagram for further details

FUNCTIONAL BLOCK DIAGRAM

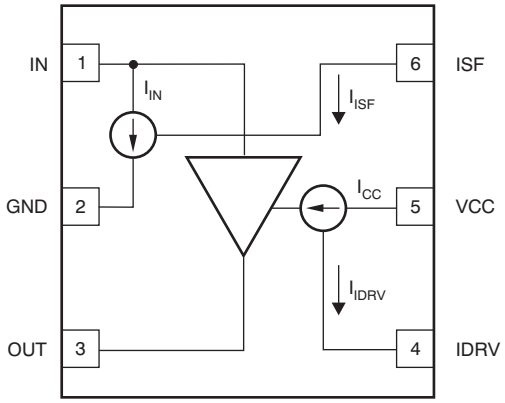


Figure 1. Block Diagram

TYPICAL CHARACTERISTICS

At T_A = +25°C, V_{CC} = 13 V, R_{IDRV} = 90 kΩ, R_{ISF} = 300 kΩ, and C_{LOAD} = 22 pF, unless otherwise noted.

BANDWIDTH vs IDRV

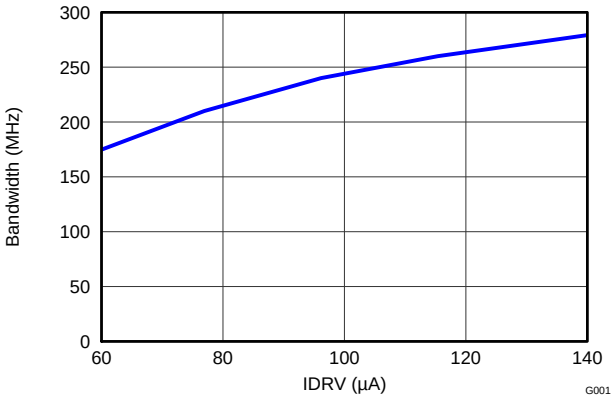


Figure 2.

INPUT MARGIN FROM V_{CC} vs IDRV

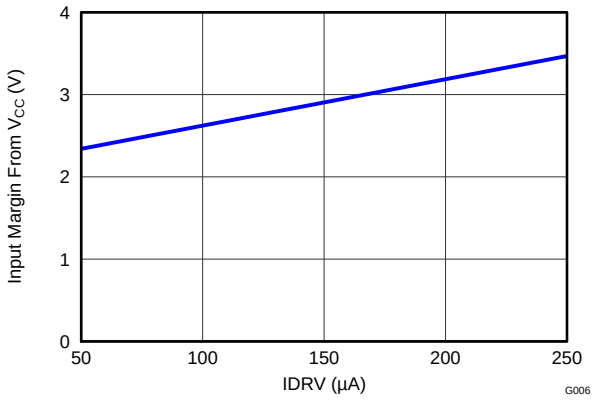


Figure 3.

IDRV vs R_{IDRV}

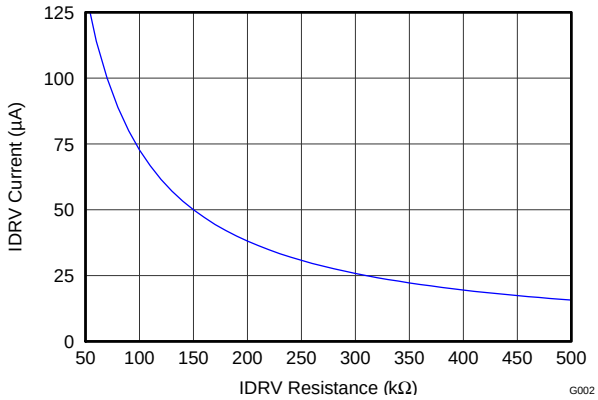


Figure 4.

INPUT LOAD CURRENT vs R_{ISF}

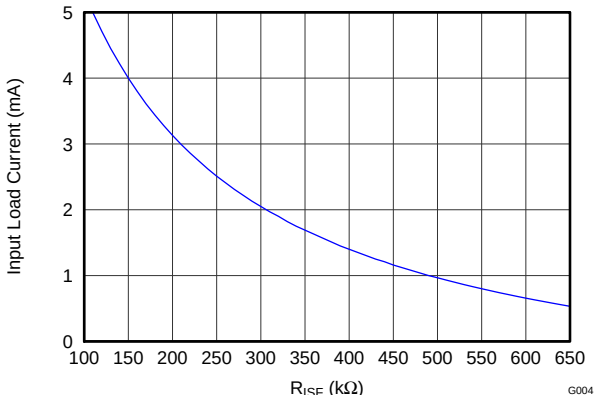


Figure 5.

IDRV vs TEMPERATURE

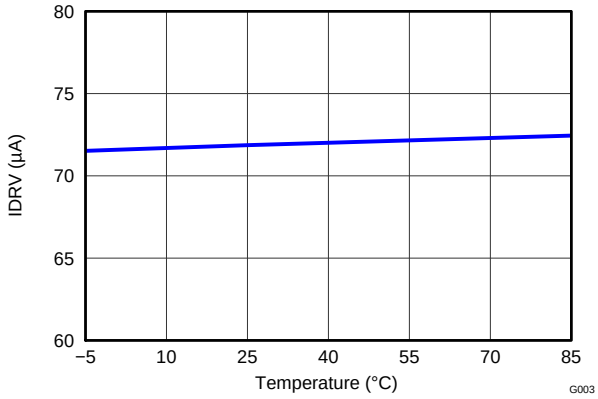


Figure 6.

INPUT LOAD CURRENT vs TEMPERATURE

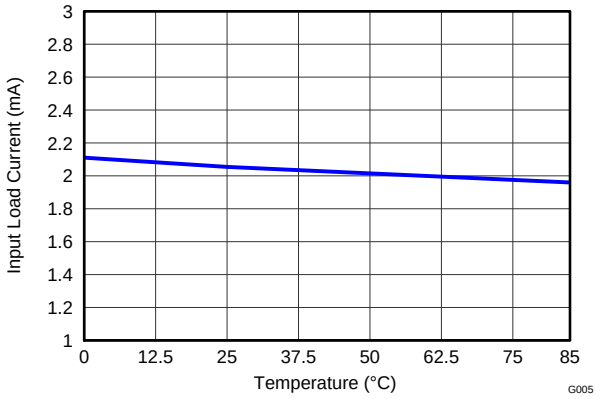


Figure 7.

TYPICAL CHARACTERISTICS (continued)

At T_A = +25°C, V_{CC} = 13 V, R_{IDRV} = 90 kΩ, R_{ISF} = 300 kΩ, and C_{LOAD} = 22 pF, unless otherwise noted.

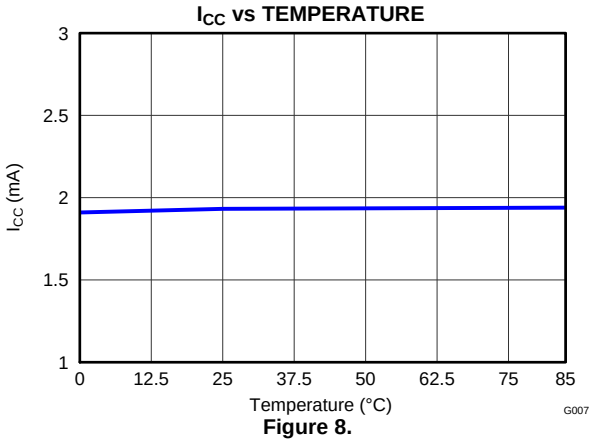


Figure 8.

OVERVIEW

TYPICAL APPLICATION CIRCUIT

Figure 9 shows a typical application circuit for the VSP1000.

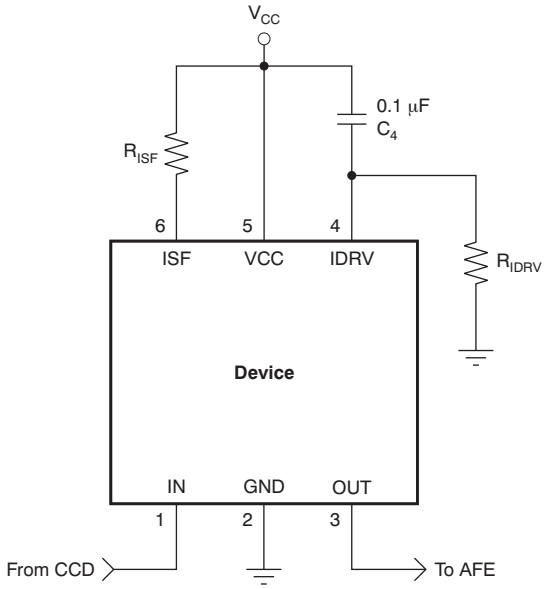


Figure 9. Typical Application Circuit

DESIGN EQUATIONS

The CCD outputs must be loaded with current for proper operation. The VSP1000 provides the ability to draw adjustable current through the IN pin. The value of the input load current can be set by choosing an appropriate value of R_{ISF} connected to the ISF pin, as per Equation 1.

$$I_{IN} = \frac{\left(\frac{(V_{CC} \times 100\ k\Omega)}{(R_{ISF} + 100\ k\Omega)}\right) - 1.2}{1\ k\Omega} \quad (1)$$

The bandwidth of the VSP1000 can be adjusted using the IDRV pin. The resistor connected at IDRV determines the drive strength of the output buffer as well as the total quiescent current of the VSP1000. Equation 2 and Equation 3 describe the relationship between R_{IDRV} and the drive strength. C_{IDRV} is used to increase the power-supply rejection ratio of the device. A value of 0.1 µF for C_{IDRV} is recommended.

$$I_{DRV} = \frac{(V_{CC} - 5)}{(R_{IDRV} + 10\ k\Omega)} \quad (2)$$

$$I_{CC} = 26 \times I_{DRV} \quad (3)$$

EXAMPLE CONFIGURATIONS

Table 1 details several example configurations for the VSP1000. All examples are with V_{CC} = 13 V.

Table 1. Example Configurations

CONFIGURATION	I_{CC} (mA)	R_{ISF} (kΩ)	R_{IDRV} (kΩ)
Bandwidth = 170 MHz , I_{IN} = 2 mA	1.5	300	133
Bandwidth = 170 MHz , I_{IN} = 4 mA	1.5	150	133
Bandwidth = 210 MHz , I_{IN} = 2 mA	2	300	91
Bandwidth = 210 MHz , I_{IN} = 4 mA	2	150	91
Bandwidth = 260 MHz , I_{IN} = 2 mA	3	300	62
Bandwidth = 260 MHz , I_{IN} = 4 mA	3	150	62

LAYOUT GUIDELINES

The decoupling capacitors C_{IDRV}, R_{IDRV}, and R_{ISF} should be placed as close as possible to the VSP1000.

REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (September 2011) to Revision A	Page
• Updated Figure 4	5
• Updated Figure 5	5

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
VSP1000DSFR	ACTIVE	SON	DSF	6	5000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 85	VK	Samples
VSP1000DSFT	ACTIVE	SON	DSF	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 85	VK	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

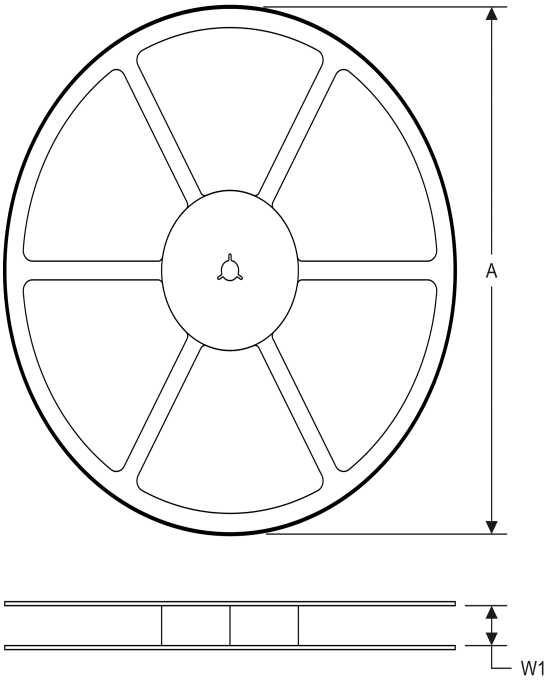
(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

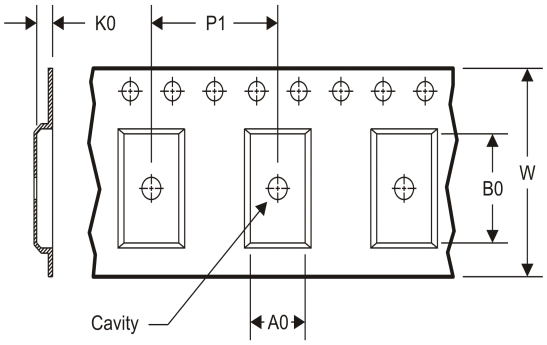
(4) Only one of markings shown within the brackets will appear on the physical device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



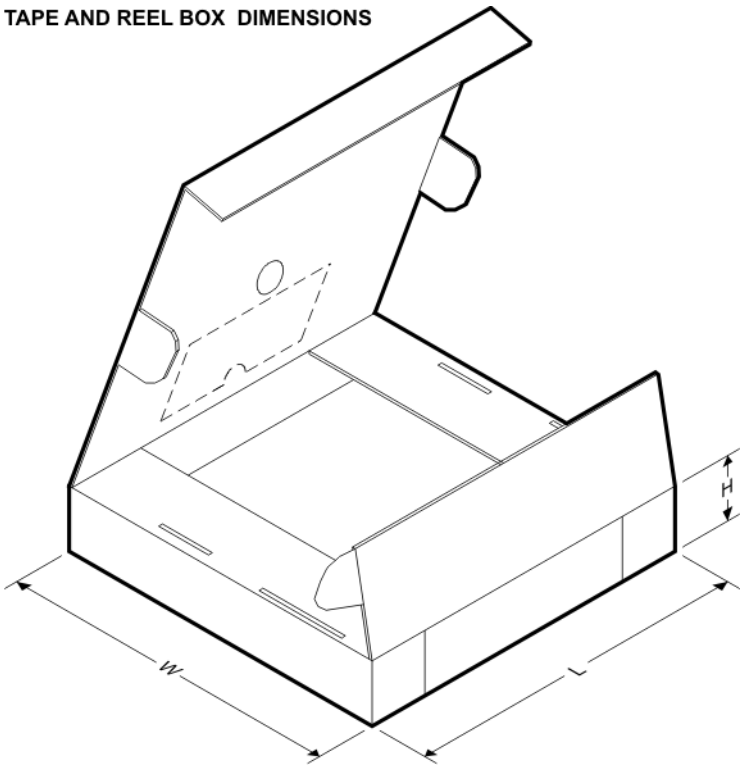
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
VSP1000DSFR	SON	DSF	6	5000	180.0	9.5	1.16	1.16	0.63	4.0	8.0	Q2
VSP1000DSFT	SON	DSF	6	250	180.0	9.5	1.16	1.16	0.63	4.0	8.0	Q2

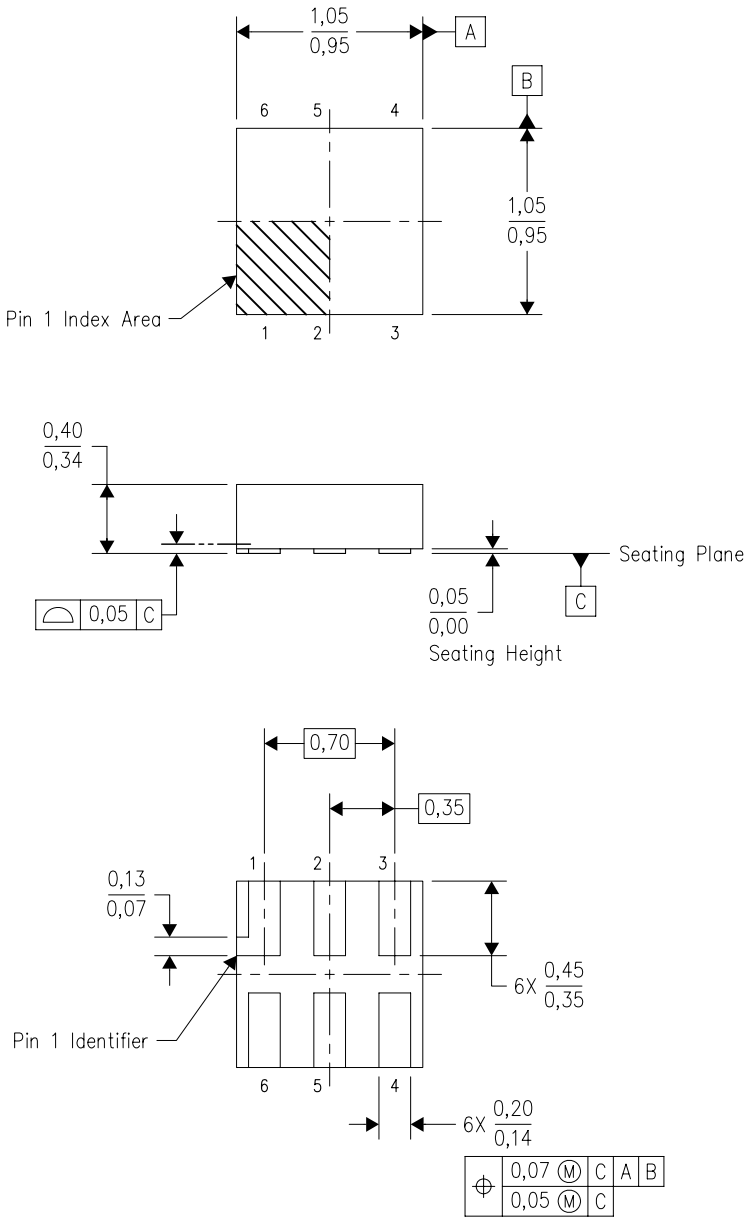
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
VSP1000DSFR	SON	DSF	6	5000	180.0	180.0	30.0
VSP1000DSFT	SON	DSF	6	250	180.0	180.0	30.0

DSF (S–PX2SON–N6) PLASTIC SMALL OUTLINE NO–LEAD



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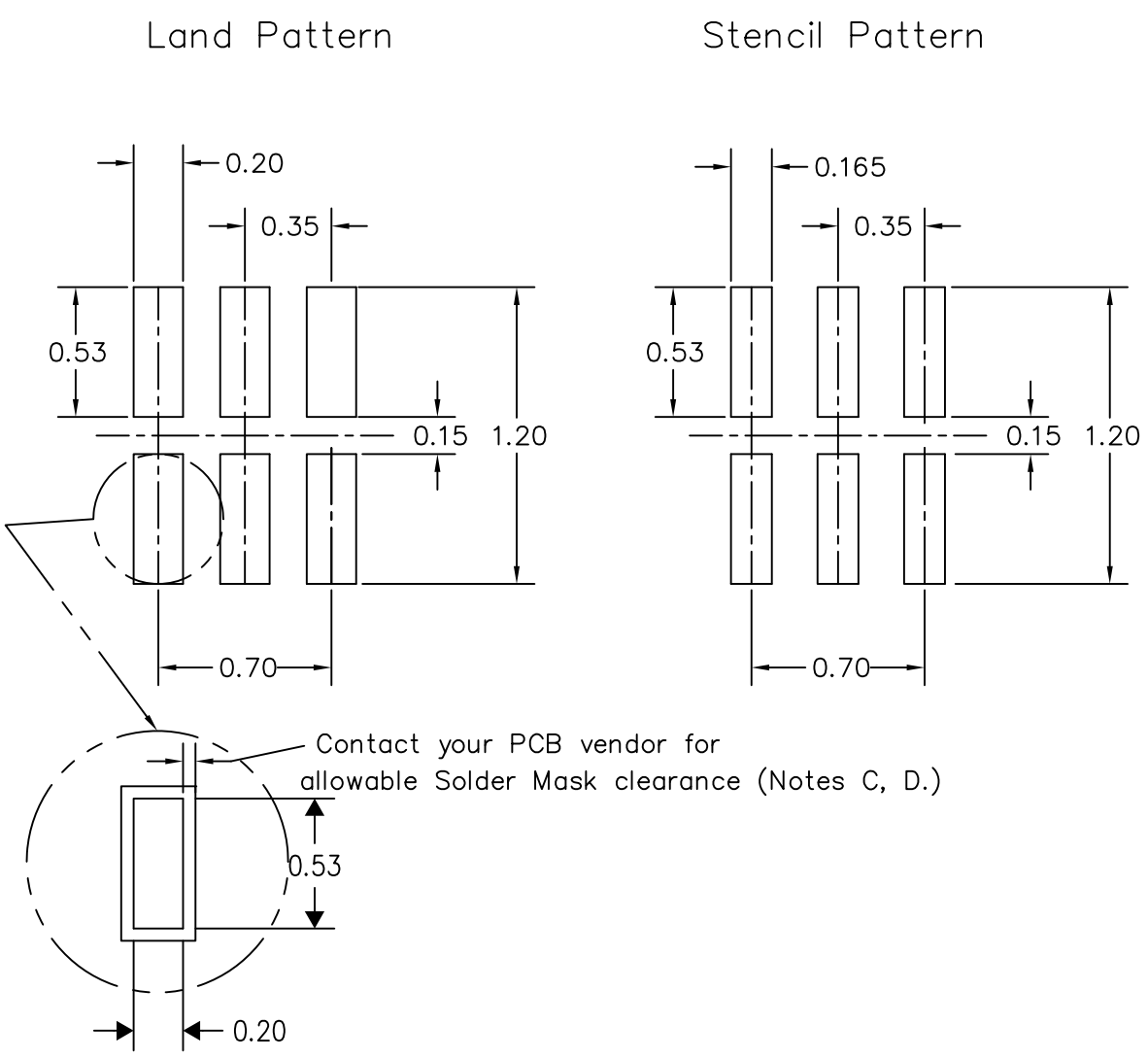
NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. SON (Small Outline No–Lead) package configuration.
D. This package complies to JEDEC MO–287 variation X2AAF.

DSF (S–PX2SON–N6) PLASTIC SMALL OUTLINE NO–LEAD



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NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads. If 2 mil solder mask is outside PCB vendor capability, it is advised to omit solder mask.
E. Maximum stencil thickness 0,1016 mm (4 mils). All linear dimensions are in millimeters.
F. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
G. Suggest stencils cut with lasers such as Fiber Laser that produce the greatest positional accuracy.
H. Component placement force should be minimized to prevent excessive paste block deformation.

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