Preliminary Data Sheet Supplement

Subject:	Additional Information for the VPC 32xxD
Data Sheet Concerned:	VPC 323xD 6251-472-1PD, Edition July 26, 2001
Supplement:	No. 7/ 6251-472-1PDS
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VPC 3230D-C5 **06.08.01**

The VPC 3230D-C5 is hardware- and software-compatible to VPC 3230D-B3. Problems 15 and 21 have been corrected in this version.

It provides the following new functions:

1. Additional horizontal and vertical sync outputs HSYA, VSYA to support analog RGB insertion (e. g. PIP or OSD/ Text)

2. Improved external memory controlling to suppress joint lines and joint field distortions

The new control bits as well as the modified pinning are described in the Preliminary data sheet.

Problem list for VPC 3230D-C5

No.	Problem	Description	Comment	OK
22.	no PAL+ helper output	In PAL+ mode, the demodulated helper signal is not available at the luma output pins	firmware change workaround: –	
23.	data output hold time out of spec	In case of 16 MHz output mode, max. load on pins and min. $V_{SUPY/C/PA/LLC}$, the data output hold time is approx. 1 ns less than specified	hardware redesign workaround: –	

Data Sheet Errata VPC 32xxD-C5 (for Preliminary Data Sheet: Edition July 26, 2001; 6251-472-1PD).

The following description replaces the corresponding specification on page 72 of the Preliminary Data Sheet (6251-472-1PD) (applies to B3 and following versions)

Symbol	Parameter	Pin Name	Min.	Typ.	Max.	Unit	Test Conditions
t_{OH}	Output Hold Time		14	–	–	ns	LLC2=32.0 MHz, OMODE=1, DBCLK=0/1

VPC 3230D-B3 **06.10.00**

The VPC 3230D-B3 is hardware- and software-compatible to VPC 3230D-B2. Problems 13 and 17 to 20 have been corrected in this version.

It provides the following new functions:

1. New status bit ‘SWITCH’ of Automatic Standard Recognition (ASR) indicating a change of the chroma standard

2. New vertical synchronization ‘AV/VS_LOCK’ of the PIP for two VPCD applications to provide a stable PIP display in case of no input signal for VPC_{main}

Problem list for VPC 3230D-B3

No.	Problem	Description	Comment	OK
15.	LLC1/LLC2 output timing	Clock skew between LLC1 and LLC2 out of spec This may cause disturbances like horizontal jitter of the picture and/or an unstable chroma demultiplex, in feature-boxes using both (LLC1 and LLC2) clocks.	hardware redesign C4 workaround for feature boxes using LLC1 and LLC2: adjust overall capacitive load on LLC1 to min. 33 pF and on LLC2 to min. 22 pF.	C5
21.	wrong interlace in NTSC	In case of NTSC input and AV_LOCK or VS_LOCK = 1, the interlace of the main picture is wrong (2VPCD application only).	hardware redesign C4 workaround: set DIS_INTL = 1 in NTSC	C5

Application Note VPC 32xxD-B3 (for Advance Information: Edition Jan. 19, 1999; 6251-472-1AI).

To ensure optimum EMI performance of the VPC 32xxD clock and data outputs, no external resistors and/or inductors should be connected to these pins (applies to B1 and following versions)!

Data Sheet Errata VPC 32xxD-B3 (for Advance Information: Edition Jan. 19, 1999; 6251-472-1AI).

The following description must be added in Table 3-2 on page 40 of the Advance Information (6251-472-1AI) (applies to B3).

FP Sub-address	Function	Default	Name
h'148	Enable automatic standard recognition bit[0] 0/1 PAL B,G,H,I (50 Hz) 4.433618 bit[1] 0/1 NTSC M (60 Hz) 3.579545 bit[2] 0/1 SECAM (50 Hz) 4.286 bit[3] 0/1 NTSC44 (60 Hz) 4.433618 bit[4] 0/1 PAL M (60 Hz) 3.575611 bit[5] 0/1 PAL N (50 Hz) 3.582056 bit[6] 0/1 PAL 60 (60 Hz) 4.433618 bit[10:7] reserved set to 0 bit[11] 1 reset status information bit 'switch' in register 'asr_status' (cleared automatically) 0: disable recognition; 1: enable recognition **Note:** For correct operation, do not change FP reg. 20h and 21h while ASR is enabled!	0	ASR_ENABLE
h'14e	Status of automatic standard recognition bit[0] 1 error of the vertical standard (neither 50 nor 60 Hz) bit[1] 1 detected standard is disabled bit[2] 1 search active bit[3] 1 search terminated, but failed bit[4] 1 no color found bit[5] 1 standard has been switched (since last reset of this flag with bit[11] of ASR_ENABLE) bit[4:0] 00000 all ok 00001 search not started, because vwin error detected (no input or SECAM L) 00010 search not started, because detected vert. standard not enabled 0x1x0 search started and still active 01x00 search failed (found standard not correct) 01x10 search failed, (detected color standard not enabled) 10000 no color found (monochrome input or switch betw. CVBS/SVHS necessary)	0	ASR_STATUS VWINERR DISABLED BUSY FAILED NOCOLOR SWITCH

The following description must be added in Table 3-2 on page 35 of the Advance Information (6251-472-1AI) (applies to B3).

I²C Sub-address	Number of bits	Mode	Function	Default	Name
			PIP Control		
h'84	16	w/r	VPC MODE: bit[0] 0/1 dis-/enable field memory control for PIP bit[1] 0/1 double/single VPC application bit[2] 0/1 select VPC_{pip}/VPC_{main} mode bit[3] 0/1 4:3/16:9 screen bit[4] 0/1 13.5/16 MHz output pixel rate bit[5] 0/1 vertical PIP window size is based on a 625/525 line video bit[7:6] field memory type 00 TI TMS4C2972/3 01 PHILIPS SAA 4955TJ 10 reserved 11 other (OKI MSM5412222, ...) *bit[11:8] are evaluated only if bit[7:6] = 11* bit[8] 0/1 delay the video output compared to WE for 0/1 LLC1 clock, if DBLCLK = 0 0/1 LLC2 clock, if DBLCLK = 1 bit[9] 0/1 pos/neg polarity for WE and RE signals bit[10] 0/1 pos/neg polarity for IE and OE signals bit[11] 0/1 pos/neg polarity for RSTWR signal bit[12] reserved (set to 0) bit[13] 0/1 vertical PIP position synchronized by input video/vertical sync in case of no video input, FLW = 0 and LLC PLL disabled. For VPC_{main} combined with a feature-box without read/write mask only! bit[14] 0/1 vertical PIP position synchronized by input video/free running sync raster FLW bit[15] reserved (set to 0) This register is updated when the PIPOPER register is written.	0	VPCMODE ENA_PIP SINGVPC MAINVPC F16TO9 F16MHZ W525 FIFOTYPE VIDEODEL WEREINV IEOEINV RSTWRINV AV_LOCK VS_LOCK

The following description must be added in Table 3-2 on page 42 of the Advance Information (6251-472-1AI) (applies to B1 and following versions).

FP Sub-address	Function	Default	Name
h'17a	ACC PAL+ Helper gain adjust, gain is referenced to PAL burst bit[11:0] 0...4094 (1591 corresponds to 100% helper gain) 4095 disabled (testmode only) a value of 4095 allows manual adjust of Helper amplitude via ACCH	1591	HLPGAIN

VPC 3230D-B2 **15.12.99**

The VPC 3230D-B2 is hardware- and software-compatible to VPC 3230D-B1. Problems 4, 8, and 16 have been corrected in this version.

Problem list for VPC 3230D-B2

No.	Problem	Description	Comment	OK
13.	PIP picture corrupted	In case of WRMAIN active, a change of the video input signal may corrupt the PIP picture (single VPC application only).	hardware redesign B3 workaround: set AVSTRT < 81 for 16 MHz mode or AVSTRT < 65 for 13.5 MHz mode	B3
15.	LLC1/LLC2 output timing	Clock skew between LLC1 and LLC2 out of spec	hardware redesign B3	
17.	FF control signals suppressed	In case of main picture = NTSC or VGA, PIP picture = PAL or SECAM, W525 = 0 and MODSEL = 3, the FFOE, FFRE, FFIE, and FFWE signals are suppressed in field 1 for dedicated settings of VSTR, e. g. VSTR = 134.	hardware redesign B3	B3
18.	TINT value overwritten	The ASR sets the TINT value (FP reg. dc'h) to 0 automatically if the color standard changes from NTSC to PAL or SECAM.	firmware change B3 workaround: rewrite TINT value	B3
19.	clamp lock in visible at the top edge of the picture	Copy-protected YC_rC_b input signals disturb the internal clamp control. Therefore, the clamp lock in remains visible at the top edge of the picture.	hardware redesign B3	B3
20.	horizontal clamp stripes on component and/or CVBS signals	There have been reports of sporadic problems with VPC 32xxD at power-up. These problems manifest themselves in the form of clamping stripes.	hardware redesign B3 workaround: replace the 10 µF capacitors attached to the pins 66 (VRT) and 78 (VREF) with 47 µF	B3

VPC 3230D-B1 **29.07.99**

The VPC 3230D-B1 is hardware- and software-compatible to VPC 3230D-A0. Problems 1, 2, 3, 5, 6, 7, 9, 11, and 12 have been corrected in this version.

Problem list for VPC 3230D-B1

No.	Problem	Description	Comment	OK
4.	CVBS/component signals	CVBS and component signals are not matched by 1 clock.	firmware change B2 workaround: set CIP_MATCH to 8!	B2
8.	vertical standard force	Vertical standard force (VFRC) is OK, but flywheel interlace (DFLW) doesn't work in case of interlace-free input signals.	firmware change B2	B2
13.	PIP picture corrupted	In case of WRMAIN active, a change of the video input signal may corrupt the PIP picture (single VPC application only).	hardware redesign B2 workaround: set WRSTOP = 1 before changing the input signal	
15.	LLC1/LLC2 output timing	Clock skew between LLC1 and LLC2 out of spec	hardware redesign B2	
16.	hor. shift of main picture	The horizontal shift of the main picture via NEWLIN doesn't work if the external memory/feature box is controlled by IE/WE. Memory write operation controlled by HS or AVO is OK!	hardware redesign B2	B2

VPC 3230D-A0 **07.05.99**

Problem list for VPC 3230D-A0

No.	Problem	Description	Comment	OK
1.	SVHS C input	internal shortcut on analog chroma signal	hardware redesign B1 workaround: connect SVHS chroma to VIN1 pin and set CIS = 0	B1
2.	I^2C register	The I^2C registers 9F, 83, and 23h don't work at V_{SUPD} > 3.2 V, while other registers don't work at V_{SUPD} > 3.4 V.	hardware redesign B1 workaround: to adjust these registers, set V_{SUPD} < 3.2 V	B1
3.	MacroVision detection	MacroVision detection doesn't work.	firmware change B1	B1
4.	CVBS/component signals	CVBS and component signals are not matched by 7 clocks.	firmware change B1 workaround: set CIP_MATCH to 2!	
5.	ASR	ASR working for CVBS only	firmware change B1	B1
6.	free-run mode	V-sync delayed by 1H in vertical free-run mode	hardware redesign B1	B1
7.	vertical stripes	white vertical stripes caused by internal FIFO timing problem for V_{SUPD} < 3.2 V	hardware redesign B1 workaround: adjust V_{SUPD} > 3.2V	B1
8.	vertical standard force	Vertical standard force (VFRC) doesn't work.	firmware change B1	
9.	PIP vertical start position	The vertical start position VSTR of all predefined PIP modes > 1 is shifted by −1 line.	hardware redesign B1 workaround: increase VSTR by +1	B1
10.	PIP frame overwritten	In case of WRPIC active, a change of the video input signal may corrupt the PIP frame.	hardware redesign B1 workaround: set WRSTOP = 1 before changing the input signal	
11.	PIP Mode 14: PIP overwritten	In single VPC operation, an update of the main picture always overwrites the PIP pictures.	hardware redesign B1 workaround: set NSPX = NSPY = 0	B1
12.	AGC	AGC doesn't work.	firmware change B1	B1
13.	PIP picture corrupted	In case of WRMAIN active, a change of the video input signal may corrupt the PIP picture (single VPC application only).	hardware redesign B1 workaround: set WRSTOP = 1 before changing the input signal	

Data Sheet Errata VPC 32xxD-A0 (for Advance Information: Edition Jan. 19, 1999; 6251-472-1AI)

The following description must be changed on page 51/52 of the Advance Information (6251-472-1AI).

Pin No. PQFP 80-pin	Pin Name	Type	Connection (if not used)	Short Description
9	V_{SUPCAP}	OUT	X	Digital Decoupling Circuitry Supply Voltage
12	GND_{CAP}	OUT	X	Digital Decoupling Circuitry GND
25	GND_{PA}	OUT	X	Pad Decoupling Circuitry GND
26	V_{SUPPA}	OUT	X	Pad Decoupling Circuitry Supply Voltage

The following description must be changed on page 55 of the Advance Information (6251-472-1AI).

Pin 58 – Front-End/Back-End Data FPDAT (Fig. 4-5)
This pin interfaces to the DDP 3300A back-end processor. The information for the deflection drives and for the white drive control, i. e. the beam current limiter, is transmitted by this pin. In applications without DDPA/B, this pin is connected with 10 kΩ to V_{SUPSY}.

The following description must be changed in Table 3-2 on page 43 of the Advance Information (6251-472-1AI).

FP Sub-address	Function	Default	Name
h'36	measured burst amplitude	read only	BAMPL

The following description must be added in Table 3-2 on page 42 of the Advance Information (6251-472-1AI).

FP Sub-address	Function	Default	Name
h'27	component input to main video input delay matching bit[5:0] reserved, set to zero bit[11:6] delay adjust cip/main 0...18 clocks, 9 = matched The setting is updated when 'sdt' register is updated.	9	CIP_ MATCH

The following description must be added in Table 3-2 on page 40 of the Advance Information (6251-472-1AI).

FP Sub-address	Function	Default	Name
h'148	Enable automatic standard recognition bit[0] 0/1 PAL B,G,H,I (50 Hz) 4.433618 bit[1] 0/1 NTSC M (60 Hz) 3.579545 bit[2] 0/1 SECAM (50 Hz) 4.286 bit[3] 0/1 NTSC44 (60 Hz) 4.433618 bit[4] 0/1 PAL M (60 Hz) 3.575611 bit[5] 0/1 PAL N (50 Hz) 3.582056 bit[6] 0/1 PAL 60 (60 Hz) 4.433618 bit[11:7] reserved set to 0 0: disable recognition; 1: enable recognition **Note:** For correct operation, do not change FP reg. 20h and 21h, while ASR is enabled!	0	ASR_ ENABLE

The following description must be added in Table 3-2 on page 42 of the Advance Information (6251-472-1AI).

FP Sub-address	Function	Default	Name
h'2f	VGA mode select, pull-in range is limited to 2% bit[1:0] 0 31.5 kHz 1 35.2 kHz 2 37.9 kHz 3 reserved is set to 0 by FP if VGA = 0 bit[10] 0/1 disable/enable VGA mode bit[11] status bit, write 0, this bit is set to 1 to indicate operation complete.	 0 0	VGA_C VGAMODE VGA

The following description must be added in Table 3-2 on page 43 of the Advance Information (6251-472-1AI).

FP Sub-address	Function	Default	Name
h'170	status of macrovision detection bit[0] AGC pulse detected bit[1] pseudo sync detected	read only	MCV_ STATUS

The following description must be added in Table 3-2 on page 45 of the Advance Information (6251-472-1AI).

FP Sub-address	Function	Default	Name
h'52	brightness register	16	SCBRI
	bit[7:0] luma brightness –128...127 ITU-R output format: 16 CVBS output format: –4	16	BR
	bit[9:8] horizontal lowpass filter for Y/C 0 bypass 1 filter 1 2 filter 2 3 filter 3	0	LPF2
	bit[10] horizontal lowpass filter for high-resolution chroma 0/1 bypass/filter enabled	0	CBW2
	bit[11] reserved, set to 0 This register is updated when the scaler mode register is written.		