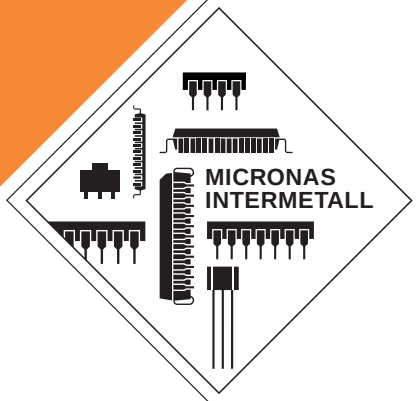


VCU 2133
Video Codec

6251-253-5E

MICRONAS
INTERMETALL

Video Codec

High-speed coder/decoder IC for analog-to-digital and digital-to-analog conversion of the video signal in digital TV receivers based on the DIGIT 2000 concept. The VCU 2133 is a VLSI circuit in CI technology, housed in a 40-pin Dil plastic package. One single silicon chip combines the following functions and circuit details (Fig. 1):

- two input video amplifiers
- one A/D converter for the composite video signal
- the noise inverter
- one D/A converter for the luminance signal
- two D/A converters for the color difference signals
- one RGB matrix for converting the color difference signals and the luminance signal into RGB signals
- three RGB output amplifiers
- programmable auxiliary circuits for blanking, brightness adjustment and picture tube alignment
- additional clamped RGB inputs for text and other analog RGB signals
- programmable beam current limiting

1. Functional Description

The VCU 2133 Video Codec is intended for converting the analog composite video signal from the video demodulator into a digital signal. The latter is further processed digitally in the VPU 2203 Video Processor and in the DPU 2553 Deflection Processor. After processing in the VPU 2203 (color demodulation, PAL compensation, etc.), the VPU's digital output signals (luminance and color difference) are reconverted into analog signals in the VCU 2133. From these analog signals are derived the RGB signals by means of the RGB matrix, and, after amplification in the integrated RGB amplifiers, the RGB signals drive the RGB output amplifiers of the color TV set.

For TV receivers using the NTSC standard the VPU 2203 may be replaced by the CVPU 2233 Comb Filter Video Processor which is pin-compatible with the VPU 2203, but offers better video performance. In the case of SECAM, the SPU 2220 SECAM Chroma Processor must be connected in parallel to the VPU 2203 for chroma processing, while the luma processing remains in the VPU 2203.

In a more sophisticated CTV receiver according to the DIGIT 2000 concept, after the VPU Video Processor may be placed the DTI 2223 Digital Transient Improvement Processor which serves for sharpening color transients on the screen. The output signals of the DTI are fed to the VCU's luma and chroma inputs. To achieve the desired transient improvement, the R-Y and B-Y D/A converters of the VCU must be stopped for a certain time which is done by the hold pulse supplied by the DTI and fed to the Reset pin 23 of the VCU. The pulse detector following this pin seperates the (capacitively-coupled) hold pulse from the reset signal.

In addition, the VCU 2133 carries out the functions:

- brightness adjustment
- automatic CRT spot-cutoff control (black level)
- white balance control and beam current limiting

Further, the VCU 2133 offers direct inputs for text or other analog RGB signals including adjustment of brightness and contrast for these signals.

The RGB matrix and RGB amplifier circuits integrated in the VCU 2133 are analog. The CRT spot-cutoff control is carried out via the RGB amplifiers' bias, and the white balance control is accomplished by varying the gain of these amplifiers. The VCU 2133 is clocked by a 17.7 or 14.3 MHz clock signal supplied by the MCU 2632 Clock Generator IC.

1.1. The A/D Converter with Input Amplifiers and Bit Enlargement

The video signal is input to the VCU 2133 via pins 35 and 37 which are intended for normal TV video signal (pin 35) and for VCR or SCART video signal (pin 37) respectively. The video amplifier whose action is required, is activated by the CCU 2030, CCU 2050 or CCU 2070 via the IM bus by software. The amplification of both video amplifiers is doubled during the undelayed horizontal blanking pulse (at pin 36) in order to obtain a higher digital resolution of the color synchronization signal (burst). At D 2-MAC reception, the doubled gain is switched off by means of bit p = 1 (Fig. 8).

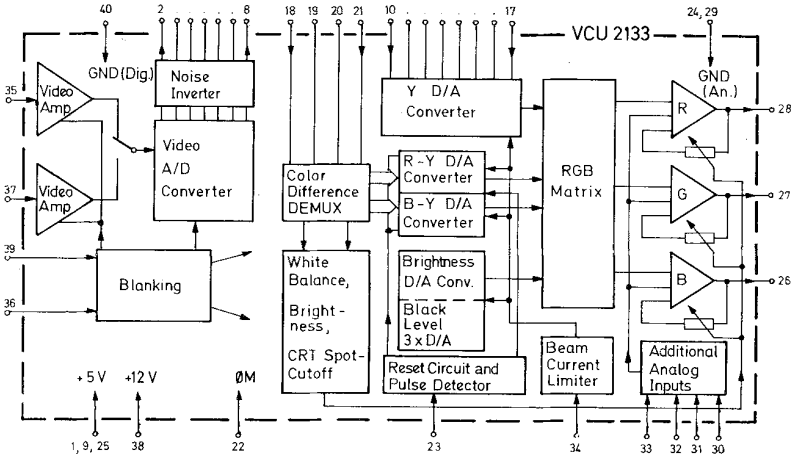


Fig. 1: Block diagram of the VCU 2133 Video Codec

The A/D converter is of the flash type, a circuit of 2^n comparators connected in parallel. This means that the number of comparators must be doubled if one additional bit is needed. Thus it is important to have as few bits as possible. For a slowly varying video signal, 8 bits are required. In order to achieve an 8-bit picture resolution using a 7-bit converter, a trick is used: during every other line the reference voltage of the A/D converter is changed by an amount corresponding to one half of the least significant bit. In this procedure, a grey value located between two 7-bit steps is converted to the next lower value during one line and to the next higher value during the next line. The two grey values on the screen are averaged by the viewer's eye, thus producing the impression of grey values with 8-bit resolution. Synchronously to the changing reference voltage of the A/D converter, to the output signal of the Y D/A converter is added a half-bit step every second line.

The bit enlargement just described must be switched off in the case of using the D2-MAC standard (q = 1 and r = 1 in Fig. 8). In the case of using the comb filter CVPU instead of the VPU, the half-bit adding in the Y D/A converter must be switched off (r = 1 in Fig. 8).

The A/D converter's sampling frequency is 17.7 MHz for PAL and 14.3 MHz for NTSC, the clock being supplied by the MCU 2632 Clock Generator IC which is common to all circuits for the digital TV system. The converter's resolution is 1/2 LSB of 8 bits. Its output signal is Gray-coded to eliminate spikes and glitches resulting from different comparator speeds or from the coder itself. The output is fed to the VPU 2203 and to the DPU 2553 in parallel form.

1.2. The Noise Inverter

The digitized composite video signal passes the noise inverter circuit before it is put out to the VPU 2203 and to the DPU 2553. The noise inverter serves for suppressing bright spots on the screen which can be generated by noise pulses, p. ex. produced by ignition sparks of cars etc. The function of the noise inverter can be seen in Fig. 2. The maximum white level corresponds with step 126 of the A/D converter's output signal (that means a voltage of 7 V at pin 35). If, due to an unwanted pulse on the composite video signal, the voltage reaches 7.5 V (what means step 127 in digital) or more, the signal level is reduced by such an amount, that a medium grey is obtained on the screen (about 40 IRE). The noise inverter circuit can be switched off by software (address 16 in the VPU 2203, see there).

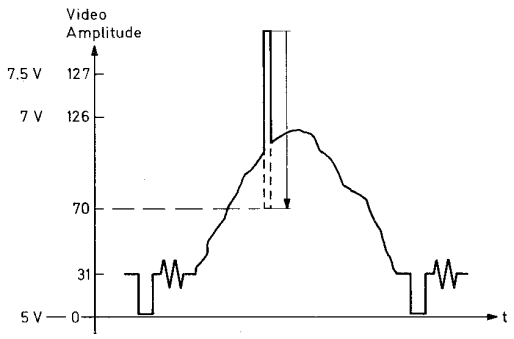


Fig. 2: Principle of the noise inverter

1.3. The Luminance D/A Converter (Y)

After having been processed in the VPU 2203 (color demodulation, PAL compensation, etc.), the different parts of the digitized video signal are fed back to the VCU 2133 for further processing to drive the RGB output amplifiers. The luminance signal (Y) is routed from the VPU's contrast multiplier to the Y D/A converter in the VCU 2133 in the form of a parallel 8-bit signal with a resolution of 1/2 LSB of 9 bits. This bit range provides a sufficient signal range for contrast as well as positive and negative overshoot caused by the peaking filter (see Fig. 3 and Data Sheet VPU 2203).

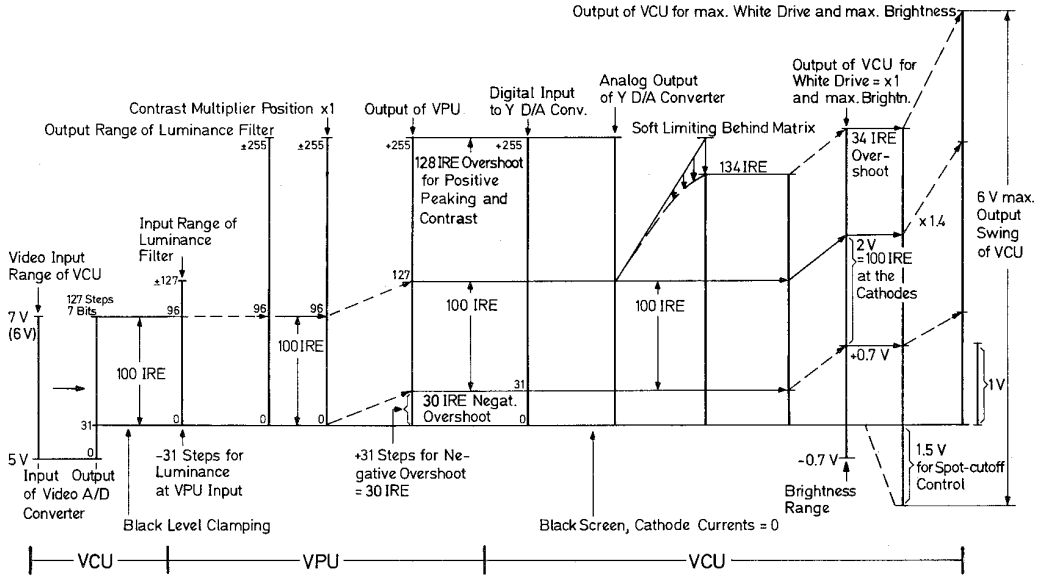


Fig. 3: Luminance level diagram (for European standard: 100 IRE ≡ 100 % BA)

The luminance D/A converter is designed as an R-2R ladder network. It is clocked with the 17.7 or the 14.3 MHz clock signal applied to pin 22. The cutoff frequency of the luminance signal is determined by the clock frequency.

1.4. The D/A Converters for the Color Difference Signals R-Y and B-Y

In order to save output pins at the VPU 2203 and input pins at the VCU 2133 as well as connection lines, the two digital color difference signals R-Y and B-Y are transferred in time multiplex operation. This is possible because these signals' bandwidth is only 1 MHz and the clock is a 17.7 or 14.3 MHz signal.

The two 8-bit D/A converters R-Y and B-Y are also built as R-2R ladder networks. They are clocked with ¼ clock frequency, but the clock for the multiplex data transfer is 17.7 or 14.3 MHz. Four times 4 bits are transferred sequentially, giving a total of 16 bits. A sync signal coordinates the multiplex operations in both the VCU 2133 and the VPU 2203. Thus, only four lines are needed for 16 bits. Fig. 4 shows the timing diagram of the data transfer described.

In a CTV receiver with digital transient improvement (DTI 2223), the R-Y and B-Y D/A converters are stopped by the hold pulse supplied by the DTI, and their output signal is kept constant for the duration of the hold pulse. Thereafter, the output signal jumps to the new value, as described in the DTI's data sheet.

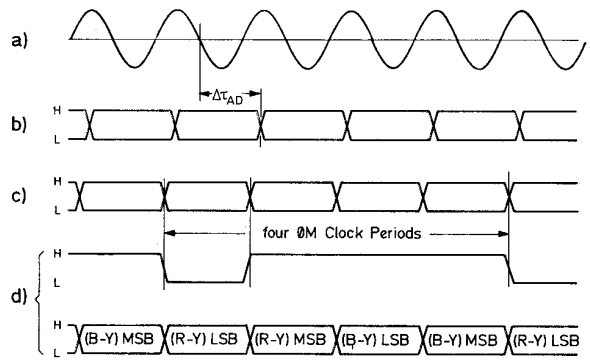


Fig. 4:
Timing diagram of the multiplex data transfer of the chroma channel between VPU 2203, VCU 2133 and SPU 2220

a) main clock signal ØM

b) valid data out of the VCU 2133's video A/D converter. $\Delta\tau_{AD}$ is the delay time of this converter, about 40 ns.

c) valid data out of the VPU 2203.

d) MUX data transfer of the chroma signals from VPU 2203 to VCU 2133, upper line: sync pulse from pin 27 VPU to pin 21 VCU during sync time in vertical blanking time, see Fig. 8; lower line: valid data from pins 27 to 30 (VPU) to pins 18 to 21 (VCU)

1.5. The RGB Matrix and the RGB Output Amplifiers

In the RGB matrix, the signals Y, R-Y and B-Y are dematrixed, the reduction coefficients of 0.88 and 0.49 being taken into account. In addition, the matrix is supplied with a signal produced by an 8-bit D/A converter for setting the brightness of the picture. The brightness adjustment range corresponds to ½ of the luminance signal range (see Fig. 3). It can be covered in 255 steps. The brightness is set by commands fed from the CCU 2030, CCU 2050 or CCU 2070 Central Control Unit to the VPU 2203 via the IM bus.

There are available four different matrices: standard PAL, matrix 2, 3 and 4, the latter for foreign markets. The required matrix must be mask-programmed during production. The matrices are shown in Table 1, based on the formulas:

$$R = r_1 \cdot (R\text{-}Y) + r_2 \cdot (B\text{-}Y) + Y$$

$$G = g_1 \cdot (R\text{-}Y) + g_2 \cdot (B\text{-}Y) + Y$$

$$B = b_1 \cdot (R\text{-}Y) + b_2 \cdot (B\text{-}Y) + Y$$

Table 1:
Values for the RGB matrices available with the VCU 2133

Coefficient	Stand.PAL	Matrix 2	Matrix 3	Matrix 4
r_1	0.56	0.93	0.72	0.87
r_2	0	−0.12	−0.19	−0.15
g_1	−0.285	−0.24	−0.22	−0.203
g_2	−0.185	−0.17	−0.10	−0.053
b_1	0	0	0	0
b_2	1	1	1	1
VCU 2133:	Brand A	Brand B	Brand C	Brand D

The three RGB output amplifiers are impedance converters having a low output impedance, an output voltage swing of 6 V (p-p), thereof 3 V for the video part and 3 V for brightness and dark signal. The output current is 4 mA. Fig. 5 shows the recommended video output stage configuration.

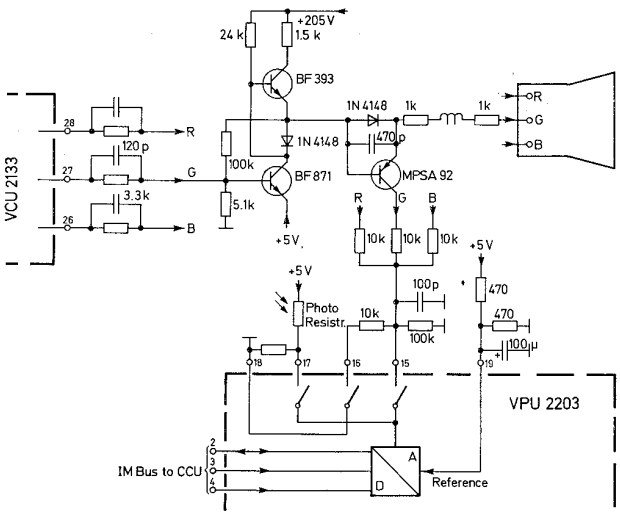


Fig. 5: Video output stage connected to the VCU 2133

For the purpose of white-balance control, the amplification factor of each output amplifier can be varied stepwise in 127 steps (7 bits) by a factor of 1 to 2. Further, the CRT spot-cutoff control is accomplished via these amplifiers' bias by adding the output signal of an 8-bit D/A converter to the intelligence signal. The amplitude of the output signal corresponds to one half of the luminance range. The eight bits make it possible to adjust the dark voltage in 0.5 % steps. By means of this circuit, the factory-set values for the dark currents can be maintained and aging of the picture tube compensated.

1.6. The Beam Current and Peak Beam Current Limiter

The principle of this circuitry may be explained by means of Fig. 6. Both facilities are carried out via pin 34 of the VCU 2133. For beam current limiting and peak beam current limiting, contrast and brightness are reduced by reducing the reference voltages for the D/A converters Y, R-Y and B-Y. At a voltage of more than +4 V at pin 34, contrast and brightness are not affected. In the range of +4 V to +3 V, the contrast is continuously reduced. At +3 V, the original contrast is reduced to a programmable level, which is set by the bits of address 16 of the VPU as shown in Table 2. A further decrease of the voltage merely reduces brightness, the contrast remains unchanged. At 2 V, the brightness is reduced to zero. At voltages lower than 2 V, the output goes to ultra black. This is provided for security purposes.

The beam current limiting is sensed at the ground end of the EHT circuit, where the average value of the beam current produces a certain voltage drop across a resistor inserted between EHT circuit and ground. The peak beam current limiting can be provided additionally to avoid "blooming" of white spots or letters on the screen. For this, a fast peak current limitation is needed which is sensed by three sensing transistors inserted between the RGB amplifiers and the cathodes of the picture tube. One of these three transistors is shown in Fig. 6. The sum of the picture tube's three cathode currents produces a voltage drop across resistor R1. If this voltage exceeds that generated by the divider R2, R3 plus the base emitter voltage of T2, this transistor will be turned on and the voltage at pin 34 of the VCU 2133 sharply reduced. Time constants for both beam current limiting and peak beam current limiting can be set by the capacitors C1 and C2.

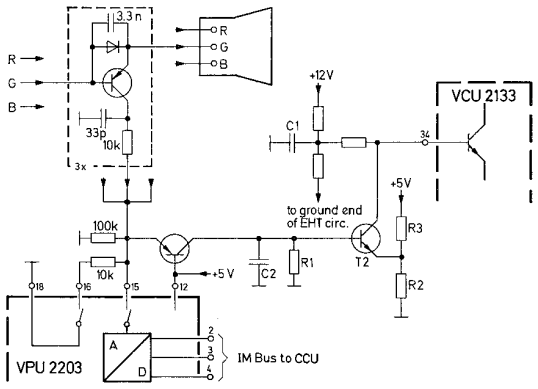


Fig. 6: Beam current and peak beam current limiter

Table 2: Code of the contrast reduction bits (addr. 16)

I	m	Contrast Reduction	
		%	dB
0	0	10	−20
0	1	30	−10
1	0	50	− 6
1	1	70	− 3

1.7. The Blanking Circuit

The blanking circuit coordinates blanking during vertical and horizontal flyback. During the latter, the VCU 2133's output amplifiers are switched to "ultra black". Such switching is different during vertical flyback, however, because at this time the measurements for picture tube alignment are carried out. During vertical flyback, only the cathode to be measured is switched to "black" during measuring time, the other two are at ultra black so that only the dark current of one cathode is measured at the same time. For measuring the leakage current, all three cathodes are switched to ultra black.

The sequence described is controlled by three code bits contained in a train of 72 bits which is transferred from the VPU 2203 to the VCU 2133 during each vertical blanking interval. This transfer starts with the vertical blanking pulse. During the transfer all three cathodes of the picture tube are biased to ultra black. In the same manner, the white-balance control is done.

The blanking circuit is controlled by two pulse combinations supplied by the DPU 2553 Deflection Processor ("sandcastle pulses"). Pin 39 of the VCU 2133 receives the combined vertical blanking and delayed horizontal blanking

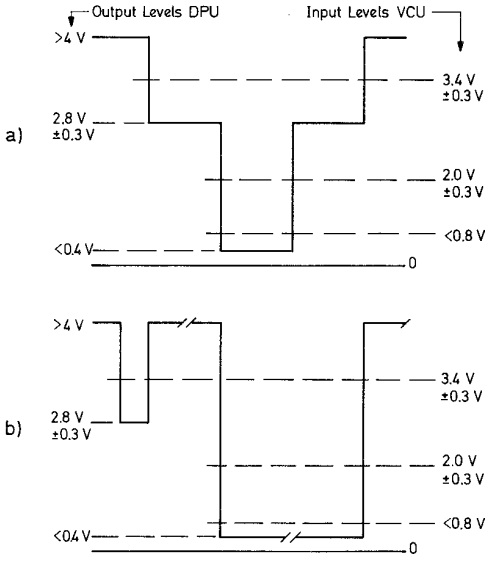


Fig. 7: Pulses which control the VCU's blanking circuit
a) combined undelayed horizontal blanking and color key pulse (pin 36)
b) combined delayed horizontal blanking and vertical blanking pulse (pin 39)

pulse from pin 22 of the DPU (Fig. 7 b), and pin 36 of the VCU gets the combined undelayed horizontal blanking and color key pulse from pin 19 of the DPU (Fig. 7 a). The two outputs of the DPU are tristate-controlled, supplying the output levels max. 0.4 V (low), min. 4.0 V (high), or high-impedance, whereby the signal level in the high-impedance mode is determined by the VCU's input configuration, a voltage divider of 3.6 kΩ and 5 kΩ between the +5 V supply and ground, to 2.8 V. The VCU's input amplifier has two thresholds of 2.0 V and 3.4 V for detecting the three levels of the combined pulses. In this way, two times two pulses are transferred via only two lines.

1.8. The Circuitry for Picture Tube Alignment

During vertical flyback, a number of measurements are taken and data is exchanged between the VCU 2133, the VPU 2203 and the CCU 2030 or CCU 2050. These measurements deal with picture tube alignment, as white level and dark current adjustment, and with the photo current supplied by a photo resistor (Fig. 5) which serves for adapting the contrast of the picture to the light in the room where the TV set is operated. The circuitry for transferring the picture tube alignment data, the sensed beam currents and the photo current is clocked in compliance with the VPU 2203 by the vertical blanking pulse and the color key pulse. To carry out the measurements, a quadruple cycle is provided (see Table 3). The timing of the data transfer during the vertical flyback is shown in Fig. 9, and Fig. 8 shows the data sequence during that data transfer.

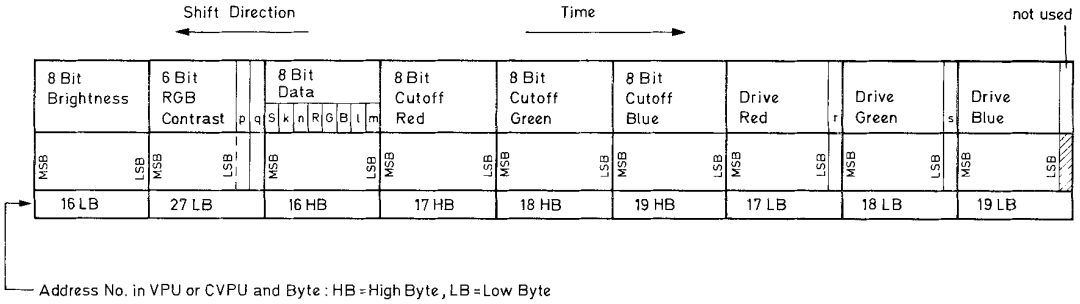


Fig. 8:
Data sequence during the transfer of test results from the VPU 2203 to the VCU 2133. Nine Bytes are transferred, in each case the LSB first. These 9 Bytes, 8 bits each, coincide with the 72 pulses of 4.4 MHz that are transferred during vertical flyback from pin 27 of the VPU 2203 to pin 21 of the VCU 2133 (see Fig. 9).
l and m: beam current limiter range
k: noise inverter on/off
n: video input switching bit
S: SECAM chroma sync bit; S = 1 means that the chroma demultiplexer is synchronized every line. The switch-over time from C0 to demux counter begins with the end of the undelayed horizontal blanking pulse and remains valid for a time of 12 ∅ M clock periods.
R, G, B: code bits
p = 1: no doubled gain in the input amplifier during horizontal blanking (see section 1.1.)
q = 1: no changing of the A/D converter's reference voltage during every other line (see section 1.1.)
r = 1: when operating with the DMA D2-MAC decoder or the CVPU comb filter video processor, the adding of a step of ½ LSB to the output signal of the Y D/A converter is switched off (see section 1.1.).
s = 1: the blanking pulse in the analog video output signal at pins 26 to 28 is switched off, as is required in stand-alone applications.

Table 3: Test cycles during four consecutive vertical blanking periods

Half Picture No.	Test carried out	Code Bit VPU→ VCU R	G	B	Code Bit VPU→ CCU	
1	Cathode leakage currents and photo current	1	1	1	0	0
2	Dark current Red, and white level Red	0	1	1	0	1
3	Dark current Green, and white level Green	1	0	1	1	0
4	Dark current Blue, and white level Blue	1	1	0	1	1

Code bit 1 means that the corresponding output amplifier of the VCU 2133 delivers the signal "ultra black" to the output amplifier connected to it.

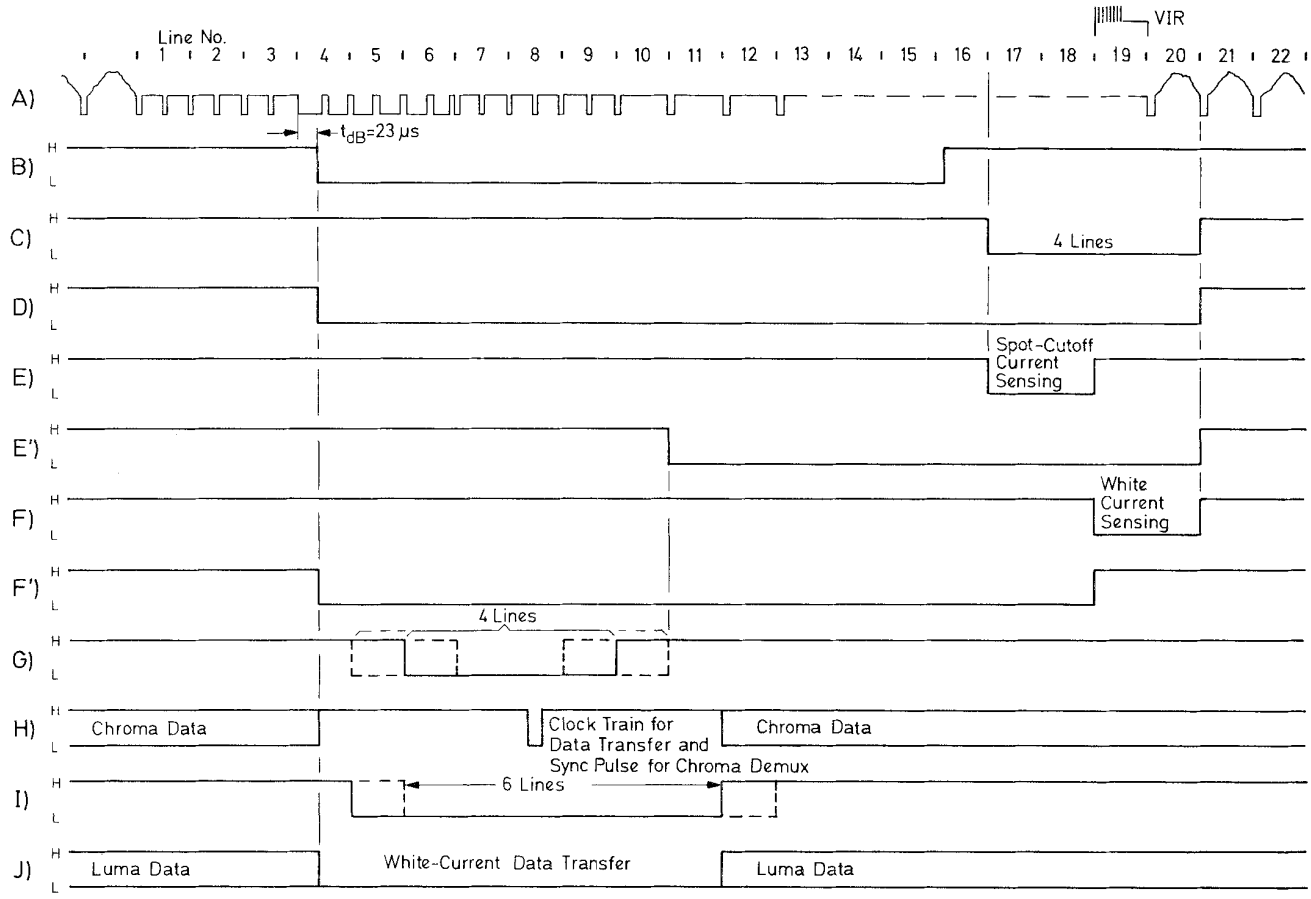


Fig. 9: Data transfer during vertical flyback

A) Video signal during vertical flyback, lines No. 1 to 22.

B) Vertical blanking pulse supplied by pin 22 of the DPU 2553 to pin 39 of the VCU 2133 (t_{aB}), duration is 13 lines and delay with respect to the start of line 4 is t_{dB} = 23 µs. With this pulse starts the 72-bit data transfer described in section 1.7., and with the end of pulse starts the picture tube's cathode current measurement.

C) Internal control pulse for CRT current measurement, generated simultaneously in VCU 2133 and VPU 2203.

D) Internal control pulse generated in VCU 2133 (pulse B + pulse C). During this pulse the cathodes of the CRT are at ultra black but the cathode under test is set to black by code bits. The D/A converters for chroma and brightness are set to zero output, and Teletext fast blanking is off.

E) Control pulse generated in VPU 2203 and VCU 2133 for CRT spot-cutoff current sensing. During this time, the measured output is set to black level.

E') Control pulse generated in VCU 2133. During this pulse, the output of the Y D/A converter delivers the white-current measuring level. This is achieved by switching off the clock for the D/A converter.

F) Control pulse generated in VPU and VCU for white current sensing. During this time, the measured output is set to white current measuring level.

F') Control pulse generated in VCU 2133 which sets the Y D/A converter to zero output by setting its reference voltage to zero.

G) Window pulse for 72-bit data transfer from VPU to VCU as described in section 1.7., duration 4 lines, generated in VCU 2133. The end of this pulse starts the clock hold-off time for the Y D/A converter (diagram E').

H) Signal at the C0/Msync output of the VPU 2203 (pin 27) supplied to the C0/Msync input of the VCU 2133 (pin 21). Normally, via this connection are transferred chroma data. With the begin of the vertical blanking, chroma data transfer is interrupted to enable the transfer of 72 clock pulses for 72-bit data transfer and transfer of the sync signal for the color difference demultiplexer contained in the VCU 2133. The clock train of 72 pulses is also used for synchronizing the counter for the chroma demultiplexer.

I) Window pulse for 72-bit data transfer, generated in VPU 2203, duration 6 lines. The end of this pulse enables Y and chroma data output from VPU to VCU.

J) Signals at the L0 to L7 outputs (pin 32 to 39) of the VPU 2203 supplied to the L0 to L7 inputs (pins 10 to 17) of the VCU 2133. With the begin of vertical blanking, luma data transfer is interrupted and the luminance output of the VPU 2203 supplies white-current measuring level during lines 19 and 20 (see diagram F).

Note: The diagram above has been drawn for NTSC. With PAL, the duration of the vertical blanking pulse is 5 lines longer, and the diagram has 25 lines instead of 20.

1.9. The Additional RGB Inputs

The three additional analog RGB inputs are provided for inputting text or other analog RGB signals. They are connected to fast voltage-to-current converters whose output current can be altered in 64 steps (6 bits) for contrast setting between 100 % and 30 %. The three inputs are clamped to a DC black level which corresponds to the level of 31 steps in the luminance channel, by means of the color key pulse. So, the same brightness level is achieved for normal and for external RGB signals. The output currents of the converters are then fed to the three RGB output amplifiers. Switchover to the external video signal is also fast.

1.10. The Reset Circuit and Pulse Detector

The reset pulse produced by the external reset RC network in common for the whole DIGIT 2000 system, switches the RGB outputs to ultra black during the power-on routine of the TV set. At other times, high level must be applied to the reset input pin 23.

There is an additional facility with pin 23 which is used only in conjunction with the DTI 2223 Digital Transient Improvement Processor. The hold pulse produced by the latter which serves for stopping the R-Y and B-Y D/A converters, is also fed to pin 23, capacitively-coupled. The pulse detector responds on positive pulses which exceed the 5 V supply by about 1 V. The two DACs are stopped as long as the hold pulse lasts, and supply a constant output signal of the amplitude at the begin of the hold pulse.

2. Outline Dimensions and Pin Connections

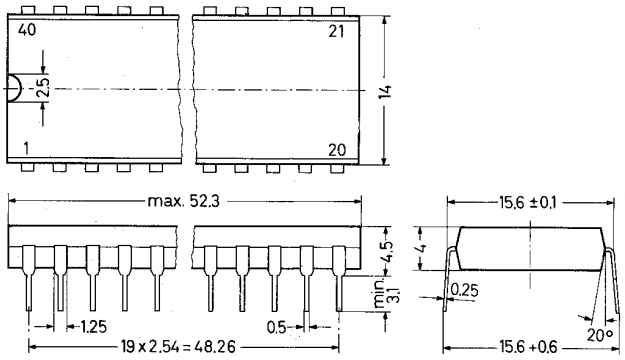


Fig. 10:
VCU 2133 in 40-pin Dil Plastic Package, 20 B 40 according to DIN 41 870

Weight approx. 6 g Dimensions in mm

Pin Connections

1	Supply Voltage, +5 V
2	V0 Output (LSB)
3	V1 Output
4	V2 Output
5	V3 Output
6	V4 Output
7	V5 Output
8	V6 Output (MSB)
9	Digital Supply Voltage, +5 V
10	L7 Input (MSB)
11	L6 Input
12	L5 Input
13	L4 Input
14	L3 Input
15	L2 Input
16	L1 Input
17	L0 Input (LSB)
18	C1 Input
19	C2 Input
20	C3 Input (MSB)
21	C0 and Msync Input (LSB)
22	ØM Main Clock Input, 17 or 14 MHz
23	$\overline{\text{Reset}}$ and Hold Pulse Input
24	Analog Ground, 0
25	Supply Voltage, +5 V
26	B Output
27	G Output
28	R Output
29	Analog Ground, 0
30	Additional B Input
31	Additional G Input
32	Additional R Input
33	Fast Switching Input
34	Beam Current Limiter Input
35	Composite Video Signal Input 1
36	Undelayed Hor. Blanking and Color Key Pulse Input
37	Composite Video Signal Input 2
38	Supply Voltage, +12 V
39	Vertical Blanking and Delayed Horizontal Blanking Input
40	Digital Ground, 0

3. Electrical Characteristics

All voltages are referred to pins 24, 29 and 40.

Absolute Maximum Ratings

	Symbol	Value	Unit
Supply Voltage			
Pins 1, 9 and 25	V_B	6	V
Pin 38	V_{38}	15	V
Input Voltages			
Pins 35 and 37	V_{35}, V_{37}	4 to 8	V
Pins 10 to 22 and 30 to 33	V_I	0 to 2	V
Pins 36 and 39	V_I	0 to 5	V
Pin 23	V_I	0 to 12	V
Pin 34*	V_I	0 to 6	V
	I_I	0 to 2	mA
Output Currents			
Pins 2 to 8	I_O	±10	mA
Pins 26 to 28	I_O	−4	mA
Load Resistance at Pins 26 to 28	R_L	min. 500	Ω
Ambient Operating Temperature Range	T_A	0 to +65	°C
Storage Temperature Range	T_S	−40 to +125	°C

* Pin 34 is internally clamped to +5 V by a diode.

Recommended Operating Conditions in Connection with the VPU 2203 and the DPU 2553

	Symbol	Min.	Typ.	Max.	Unit
Supply Voltages					
Pins 1, 9 and 25	V_B	4.75	5.0	5.25	V
Pin 38	V_{38}	11.4	12	12.6	V
Input Current, Pins 10 to 21, High Level	$-I_I$	–	–	50	µA
Input Voltages					
Pin 35 (peak-to-peak)	V_{35}	–	2	–	V
Pin 37 (peak-to-peak)	V_{37}	–	1	–	V
Pins 10 to 21, Low Level	V_{IL}	–	–	0.35	V
Pin 22					
Peak-to-Peak	$V_{\varnothing M}$	0.8	–	2.5	V
DC Level	$V_{\varnothing M}$	1.5	–	3.5	V
Clock Frequency, Pin 22					
for PAL and SECAM	$f_{\varnothing M}$	–	17.734475	–	MHz
for NTSC	$f_{\varnothing M}$	–	14.31818	–	MHz
Input Voltages					
Pins 30 to 32					
Black Level	V_I	–	0	–	V
White Level	V_I	–	1	–	V
Pin 33					
for Inputs Pins 30 to 32 On	V_I	0.8	–	–	V
for Inputs Pins 30 to 32 Off	V_I	–	–	0.3	V
Pin 23					
for Reset On	V_I	–	–	2.8	V
for Reset Off	V_I	3.5	–	–	V
for stopping the R-Y and B-Y D/A Converters	V_I	6.5	–	–	V
Pin 34 No Action	V_{34}	0.88 V_{25}	–	–	–

Recommended Operating Conditions, continued

Address	Documentation	Value (Decimal)
11	Peaking	04
12	ACC Level	33 (for PAL) 22 (for NTSC)
13	Color Killer	126 . . . 120
14	adjusts the VCO in the MCU 2632 Clock Generator to center of working range and selects the standard (PAL or NTSC)	
15	Luminance Contrast	47
16	Brightness Teletext Contrast	127 63
17 18 19	Red Green Blue Cutoff Voltages	127; White Drive 127
20	White Current Sensing Voltage	50
23	Hue Correction Color Saturation	$\alpha = 0$ 31
27	External RGB Contrast	56

Characteristics

at $V_B = 5$ V, $V_{38} = 12$ V, $f_{\varnothing M} = 17.734$ MHz, $T_A = 25$ °C, Input Signals as specified under Recommended Operating Conditions, in connection with VPU 2203 and DPU 2553, Input Signal at Pin 35 (VCU 2133) Standard Color Bars, 75 % Saturation, 2 V (p-p), the following data set by the CCU 2030, CCU 2050 or CCU 2070 or a similar test computer:

The DPU 2553 is set to normal "locked" operation depending on the selected standard (PAL or NTSC). For proper setting the input data of the DPU 2553 see data sheet of this device. Pin 33 is set to 0 V and Pin 34 to +5 V normally. They may be taken to other levels at some tests, as specified there.

	Symbol	Min.	Typ.	Max.	Unit
Current Consumption Pins 1, 9 and 25	I_B	–	70	–	mA
Pin 38	I_{38}	–	60	–	mA
Clamping Voltage at Pin 35 during Black Porch	V_{35}	–	5.5	–	V
Output Voltage, Pins 2 to 8 High Level at $-I_O = 100$ µA	V_{OH}	$0.5 \cdot V_B + 0.5$ V	–	–	V
Low Level at $I_O = 0.5$ mA	V_{OL}	–	–	$0.5 \cdot V_B - 0.5$ V	V
Input Voltage, Pins 10 to 21, High Level at $I_I = 0$	V_I	–	–	0.4	V
Input Current, Pins 10 to 21, Low Level at $V_I = 300$ mV	$-I_I$	–	2	3	mA
Output Voltages at Pins 26 to 28					
peak-to-peak	V_O	–	2.5	–	V
Cutoff Voltages Range (Black Level) when Cutoff Input is changed from 0 to 255 in Addresses 17 to 19, p-p	V_O	–	1.5	–	V
White Drive Control, p-p, when White Drive Input is changed from 0 to 127 in Addresses 17 to 19	V_O	1.8	–	3.5	V
Brightness Voltage Range, p-p, when Brightness Value is changed from 0 to 255 in Address 16	V_O	–	1.5	–	V
Reduction of RGB Signals to programmed value	V_{34}	$0.6\ V_{25}$	–	$0.88\ V_{25}$	–
Brightness Reduction to zero	V_{34}	$0.4\ V_{25}$	–	$0.6\ V_{25}$	–

Characteristics, continued

	Symbol	Min.	Typ.	Max.	Unit
Delayed Horizontal Blanking Threshold Pin 39	V_{DHB}	–	3.4	–	V
Vertical Blanking Threshold Pin 39	V_{VB}	–	2.0	–	V
Horizontal Blanking Threshold Pin 36	V_{HB}	–	3.4	–	V
Color Key Threshold Pin 36	V_{CK}	–	2.0	–	V
Test of the Additional RGB Inputs Pins 30 to 32					
Output Voltages at Pins 26 to 28, peak-to-peak, when Pin 33 at + 1 V, Standard RGB Signals (as shown in Fig. 3-11) applied to Pins 30 to 32, Amplitude 1 V p-p	V_O	–	3.0	–	V
Teletext Contrast Control, Test Conditions as before, Change Teletext Contrast Value in Address 27 from 63 to 0, peak-to-peak	V_O	–	3 V to 0.6 V	–	–

Test of Beam Current Limitation

If, at standard test condition, the voltage at pin 34 is changed from 4 V to 3 V, the peak-to-peak value of the output voltage at pins 26 to 28 will be decreased from 2 V by the value shown in Table 2.

Further, if Luminance Contrast is set to 0 (Address 15), Color Saturation to 0 (Address 23) and Brightness to 255 (Address 16), and if the voltage at pin 34 is changed from 3 V to 2 V, the peak-to-peak value of the output voltage at pins 26 to 28 will be decreased from 0.7 V to 0 V. When the voltage of pin 34 is decreased below 2 V, the three RGB outputs are set to ultra black blanking level. This is provided for security purposes.

Tests in Conjunction with the VPU 2203 The following tests mainly concern the VPU 2203 Video Processor, but are carried out with both ICs VCU 2133 and VPU 2203 acting together.

Luminance Contrast Range Test

At this test, a composite video signal is applied to pin 35 of the VCU 2133 whose chroma part is zero and the luminance part has 50 % contrast. An output signal as shown in Fig. 12 will appear at the RGB outputs pins 26 to 28 of the VCU 2133. If the luminance contrast (Address 15) is changed as follows, the output amplitude will change accordingly:

Contrast Value (Decimal)	Output Amplitude Pins 26 to 28 (p-p)
63	2 V
32	1 V
0	0 V

Color Saturation Range Test

At this test, a composite video signal is applied to pin 35 of the VCU 2133 having a total amplitude (p-p) of 2 V, a 100 % luminance contrast, a 50 % chroma saturation and an angle of $\alpha = 0°$. An output signal as shown in Figs. 11 or 12 will appear at the RGB outputs pins 26 to 28 of the VCU 2133. If the color saturation (Address 23) is changed as follows, the output signals will change accordingly. The burst amplitude (Address 12) is set to 58 for PAL or to 44 for NTSC.

Saturation Value (Decimal), Address 23		Output Signal Pins 26 to 28
31	Contrast set to 46 for all tests	as in Fig. 3-11, like 100 % color saturation
16		like 50 % color saturation
0		as in Fig. 3-12, no color

Hue Correction Test, Range of α = 0 to 360°

The values of cos α and sin α including sign are multiplied with the color saturation factor in the CCU and given, via the IM bus using address 23, to the VPU 2203. For testing this facility, there may be used a rainbow signal as chroma signal. If the hue angle α is slowly varied in steps of 1° by software, the rainbow will move across the screen with no change in color.

Characteristics, continued

Peaking Curves

The curves that can be obtained by changing the input to the CCU by the user are shown in Fig. 13. The information on this is transferred via the IM bus using address 11, to the VPU 2203. The peaking characteristic has a variable dead zone (backlash) as shown in Fig. 14. The backlash can be adjusted by the data word in address 13, Low-Byte.

Chroma Bandpass Curves

The chroma filter can be switched to symmetrical or asymmetrical response and to narrow and broad response via the IM bus using address 14 or address 15 respectively. The curves are shown in Fig. 15. The filters can be tested by applying a sweeped video signal to pin 35 of the VCU 2133 (video frequency swept from zero to 5 MHz during one line of the horizontal deflection).

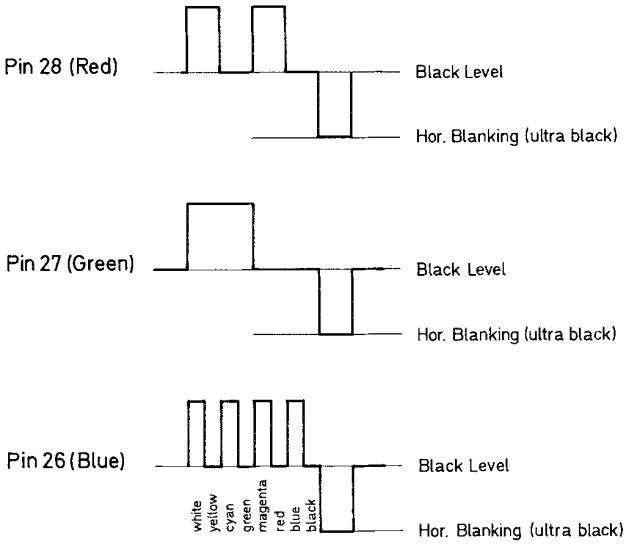


Fig. 11:
Output signals at the RGB outputs pins 26 to 28 with standard RGB signals (color bars) applied to the composite video input pin 35 of the VCU 2133, with color saturation and luminance contrast selected by the CCU via the IM bus, using addresses 15 and 23. Set values as under recommended operating conditions.

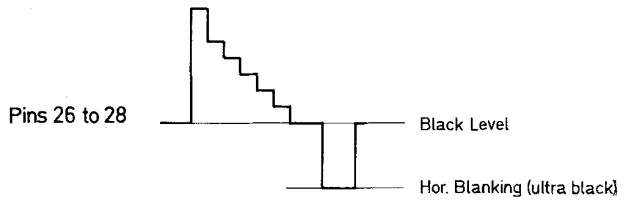
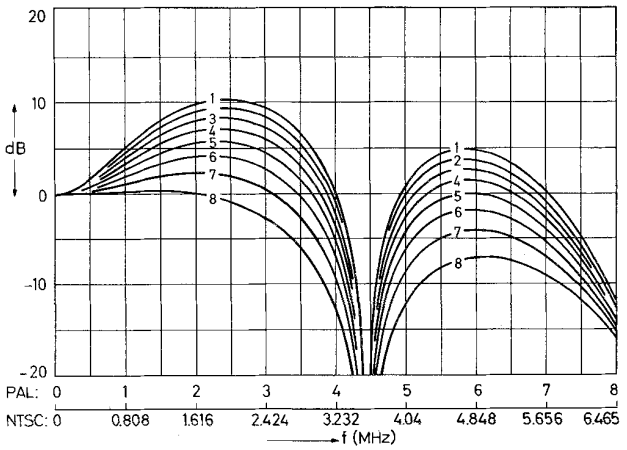
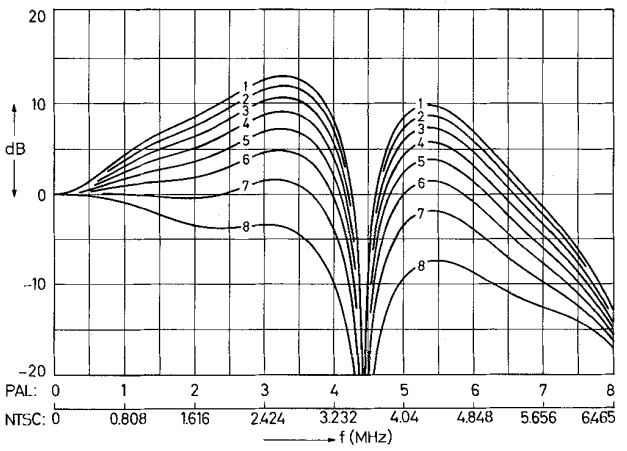


Fig. 12:
Output signals as in Fig. 11, but color saturation set to zero.



a)



b)

Fig. 13:
Peaking curves of the peaking filter included in the VPU 2203's chroma trap. The desired peaking value is set by the CCU via the IM bus using address 11.
a) normal peaking response
b) extra-wide peaking response

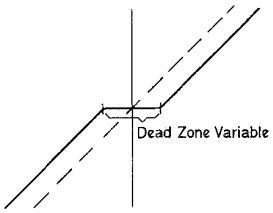


Fig. 14: Dead zone in peaked signals (Address 11 of VPU, value from 0 to ± 127)

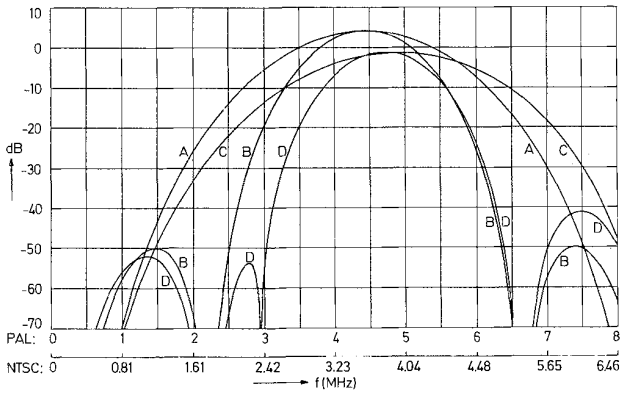


Fig. 15:
Chroma bandpass curves of the VPU 2203
A = broad band, symmetrical response
B = narrow band, symmetrical response
C = broad band, asymmetrical response
D = narrow band, asymmetrical response

4. Inner Configuration of the Connection Pins

The following figures schematically show the circuitry at the various pins.

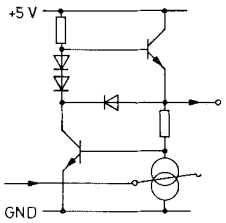


Fig. 16:
Output Pins 2 to 8

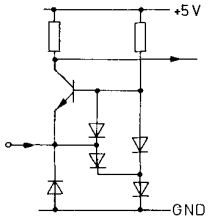


Fig. 17:
Input Pins 10 to 21

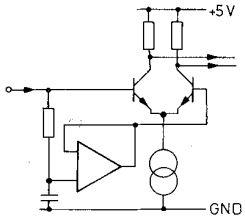


Fig. 18:
Input Pin 22

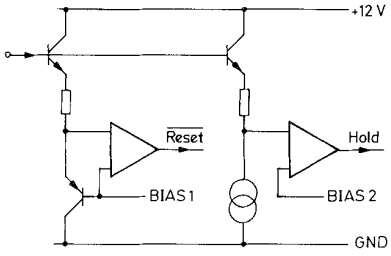


Fig. 19:
Input Pin 23

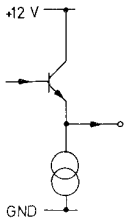


Fig. 20:
Output Pins 26 to 28

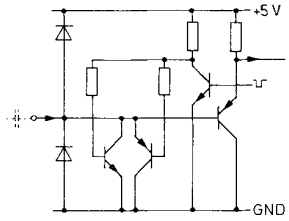


Fig. 21:
Input Pins 30 to 32

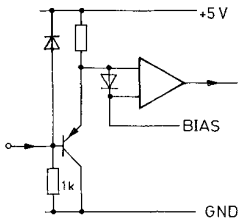


Fig. 22:
Input Pin 33

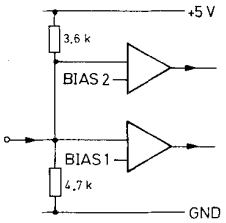


Fig. 23:
Input Pins 36 and 39

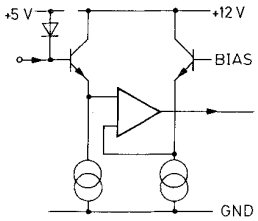


Fig. 24:
Input Pins 35 and 37

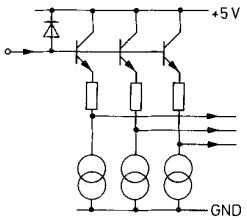


Fig. 25:
Input Pin 34

5. Description of the Connections and the Signals

Pins 1, 9, and 25 – Supply Voltage, +5 V
The supply voltage is +5 V. Pins 1 and 25 supply the analog part and must be filtered separately.

Pins 2 to 8 – Outputs V0 to V6
Via these pins the VCU 2133 supplies the digitized video signal in a parallel 7-bit Gray code to the VPU 2203 and the DPU 2553. The output configuration is shown in Fig. 16.

Pins 10 to 17 – Inputs L7 to L0
Fig. 17 shows these inputs' configuration. Via these pins, the VCU 2133 receives the digital luminance signal from the VPU 2203 in a parallel 8-bit code.

Pins 18 to 21 – Inputs C0 to C3
Via these inputs, whose circuitry and data correspond to those of pins 10 to 17, the VCU 2133 is fed with the digitized color difference signals R-Y and B-Y and with the control and alignment signals described in section 1.8., in multiplex operation. Pin 21 is additionally used for the multiplex sync signal.

Pin 22 – ØM Main Clock Input
Via this pin, whose circuitry is shown in Fig. 18, the VCU 2133 is supplied with the clock signal ØM produced by the MCU 2600 or MCU 2632 Clock Generator IC. The clock frequency is 17.7 MHz for PAL and SECAM and 14.3 MHz for NTSC. The clock signal must be DC-coupled.

Pin 23 – $\overline{\text{Reset}}$ and Hold Pulse Input (Fig. 19)
Via this pin, the VCU 2133 is supplied with the reset and hold signals which are supplied by pin 21 of the DTI 2223 Digital Transient Improvement Processor for stopping the R-Y and B-Y D/A converters, and for Reset.

Pins 24 and 29 – Analog Ground, 0
These pins serve as ground connections for the supply and for the analog signals (GND pin 24 for RGB).

Pins 26 to 28 – RGB Outputs
These three analog outputs deliver an analog signal suitable for driving the RGB output transistors. Their diagram is shown in Fig. 20. The output voltage swing is 6 V total, 3 V for the black-to-white signal and 3 V for adjusting the brightness and the black level.

Pins 30 to 32 – Additional Analog Inputs R, G and B
Fig. 21 shows the configuration of these inputs. They serve to feed analog RGB signals, for example for Teletext or similar applications, and they are clamped during the color key pulse. At a 1 V input, full brightness is reached. The bandwidth extends from 0 to 8 MHz.

Pin 33 – Fast Switching Input
This input is connected as shown in Fig. 22. It serves for fast switchover of the video channel between an internally-produced video signal and an externally-applied video signal via pins 30 to 32. With 0 V at pin 33, the RGB outputs will supply the internal video signal, and at a 1 V input level, the RGB outputs are switched to the external video signal. Bandwidth is 0 to 4 MHz, and input impedance 1 kΩ minimum.

Pin 34 – Beam Current Limiter Input
The diagram of pin 34 is shown in Fig. 25. The input voltage may be between +5 V and 0 V. The input impedance is 100 kΩ. The function of pin 34 is described in section 1.6.

Pin 35 – Composite Video Signal Input 1
To fully drive the video A/D converter the following amplitudes are required at pin 35: +5 V = sync pulse top level, all bits low; +7 V = peak white, all bits high. Fig. 24 shows the configuration of pin 35.

Pin 36 – Undelayed Horizontal Blanking and Color Key Pulse Input
The circuitry of this pin is shown in Fig. 23. Pin 36 receives the combined undelayed horizontal blanking and color key pulse which are "sandcastled" and are supplied by pin 19 of the DPU 2553 Deflection Processor. During the undelayed horizontal blanking pulse, the input amplifiers' gain is doubled, and the bit enlargement circuit is also switched by this pulse, and the counter for the data transmission gap started. The color key pulse is used for clamping the RGB inputs pins 30 to 32.

Pin 37 – Composite Video Signal Input 2
This pin has the same function and properties as pin 35, except the gain of the input amplifier which is twice the gain as that of the amplifier at pin 35. This means an input voltage range of +5 V to +6 V.

Pin 38 – Supply Voltage, +12 V
The 12 V supply is needed for certain circuit parts to obtain the required input or output voltage range, as the video input and the RGB outputs (see Figs. 20 and 24).

Pin 39 – Vertical Blanking and Delayed Horizontal Blanking Input
This pin receives the combined vertical blanking and delayed horizontal blanking pulse from pin 22 of the DPU 2553 Deflection Processor. Both pulses are "sandcastled" so that only one connection is needed for the transfer of two pulses. These two pulses are separated in the input circuitry of the VCU 2133, and are used for blanking the picture during vertical and horizontal flyback. Fig. 23 shows the circuitry of pin 39.

Pin 40 – Digital Ground, 0
This pin is used as GND connection in conjunction with the pins 2 to 8 and 10 to 21 which carry digital signals.

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