Burr-Brown Products
from Texas Instruments

VCA2618

SBOS254B – JULY 2002 – REVISED NOVEMBER 2003

Dual, VARIABLE GAIN AMPLIFIER with Input Buffer

FEATURES

- **GAIN RANGE: up to 43dB**
- **30MHz BANDWIDTH**
- **LOW CROSSTALK: 65dB at Max Gain, 5MHz**
- **HIGH-SPEED VARIABLE GAIN ADJUST**
- **POWER SHUTDOWN MODE**
- **HIGH IMPEDANCE INPUT BUFFER**

APPLICATIONS

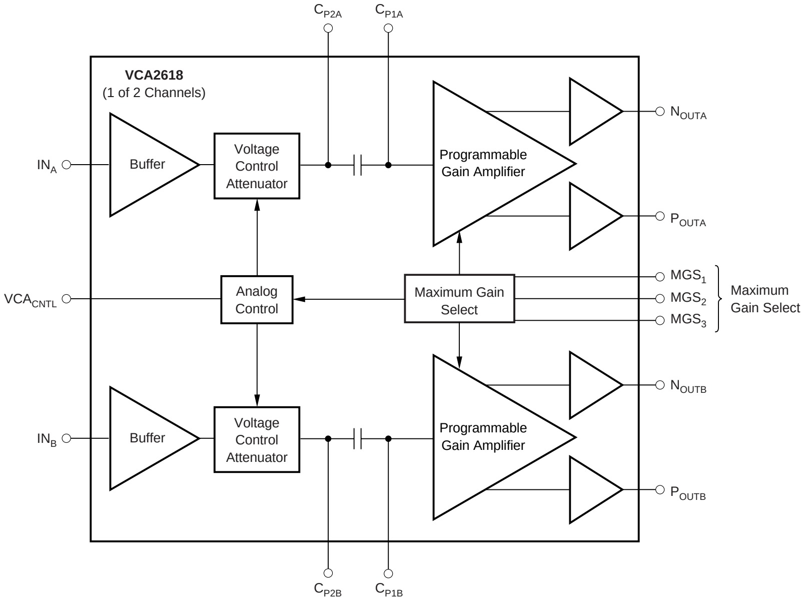
- **ULTRASOUND SYSTEMS**
- **WIRELESS RECEIVERS**
- **TEST EQUIPMENT**
- **RADAR**

DESCRIPTION

The VCA2618 is a highly integrated, dual receive channel, Variable Gain Amplifier (VGA) with analog gain control.

The VCA2618's VGA section consists of two parts: the Voltage Controlled Attenuator (VCA) and the Programmable Gain Amplifier (PGA). The gain and gain range of the PGA can be digitally programmed. The combination of these two programmable elements results in a variable gain ranging from 0dB up to a maximum gain as defined by the user through external connections. The single-ended unity gain input buffer provides predictable high input impedance. The output of the VGA can be used in either a single-ended or differential mode to drive high-performance Analog-to-Digital (A/D) converters. A separate power-down pin reduces power consumption.

The VCA2618 also features low crosstalk and outstanding distortion performance. The combination of low noise and gain range programmability make the VCA2618 a versatile building block in a number of applications where noise performance is critical. The VCA2618 is available in a TQFP-32 package.


C_{P2A}
C_{P1A}
VCA2618
(1 of 2 Channels)
IN_A
Buffer
Voltage Control Attenuator
Programmable Gain Amplifier
N_{OUTA}
P_{OUTA}
VCA_{CNTL}
Analog Control
Maximum Gain Select
MGS_1
MGS_2
MGS_3
Maximum Gain Select
IN_B
Buffer
Voltage Control Attenuator
Programmable Gain Amplifier
N_{OUTB}
P_{OUTB}
C_{P2B}
C_{P1B}

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TEXAS INSTRUMENTS
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ABSOLUTE MAXIMUM RATINGS[1]

Power Supply (+V_S)	+6V
Analog Input	–0.3V to (+V_S + 0.3V)
Logic Input	–0.3V to (+V_S + 0.3V)
Case Temperature	+100°C
Junction Temperature	+150°C
Storage Temperature	–40°C to +150°C

NOTE: (1) Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods may affect device reliability.

ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PACKAGE/ORDERING INFORMATION

PRODUCT	PACKAGE-LEAD	PACKAGE DESIGNATOR[1]	SPECIFIED TEMPERATURE RANGE	PACKAGE MARKING	ORDERING NUMBER	TRANSPORT MEDIA, QUANTITY
VCA2618Y	TQFP-32 Surface-Mount	PBS	–40°C to +85°C	VCA2618Y	VCA2618YT	Tape and Reel, 250
"	"	"	"	"	VCA2618YR	Tape and Reel, 2000

NOTE: (1) For the most current specifications and package information, refer to our web site at www.ti.com.

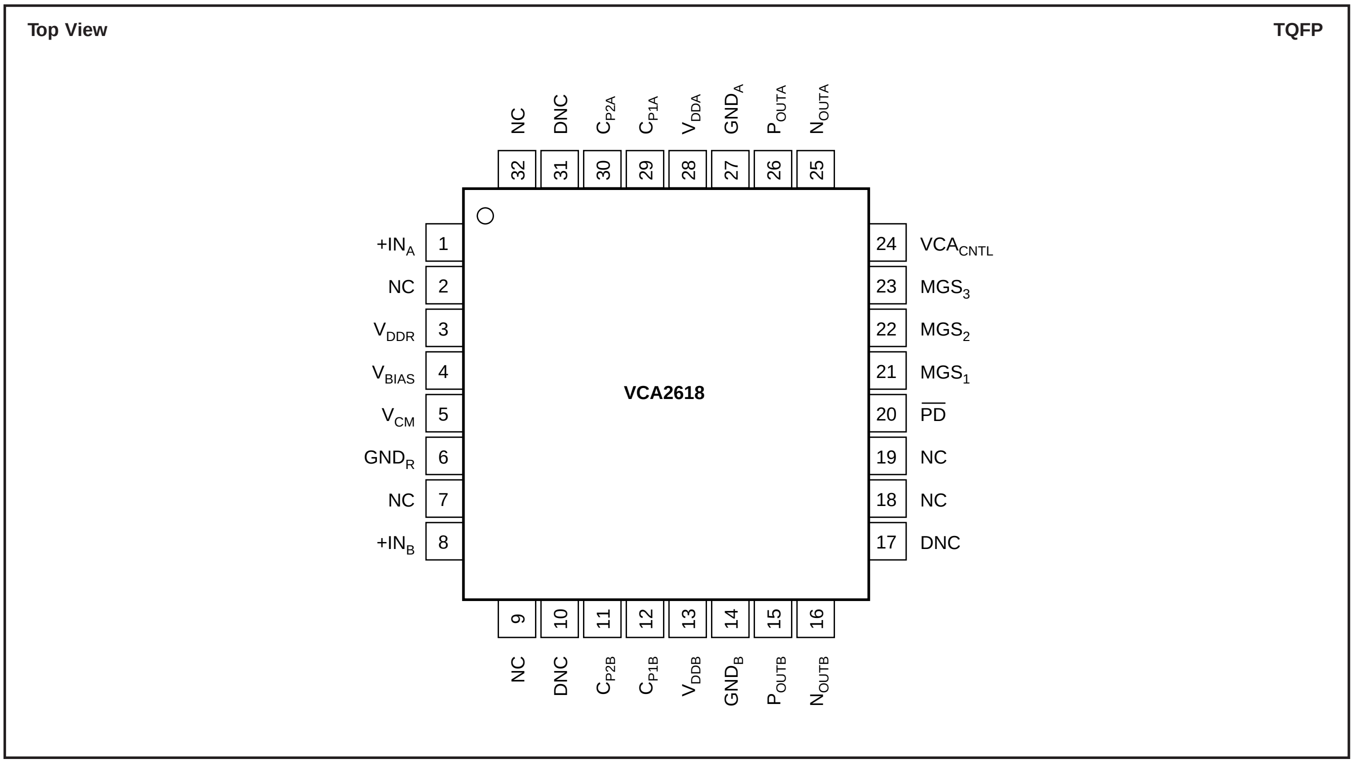
ELECTRICAL CHARACTERISTICS

At T_A = +25°C, V_{DD} = 5V, load resistance = 500Ω on each output to ground differential output ($2V_{PP}$), MGS = 111, and f_{IN} = 5MHz, unless otherwise noted.

		VCA2618Y			
PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
BUFFER					
Input Resistance			600		kΩ
Input Capacitance			5		pF
Input Bias Current			1		nA
Maximum Input Voltage			1		V_{PP}
Input Voltage Noise	PGA Gain = 45dB, R_S = 50Ω		5.4		nV/$\sqrt{Hz}$
Input Current Noise	Independent of Gain		350		fA/$\sqrt{Hz}$
Noise Figure	R_F = 550Ω, PGA Gain = 45dB, R_S = 75Ω		13		dB
Bandwidth			100		MHz
PROGRAMMABLE VARIABLE GAIN AMPLIFIER					
Peak Input Voltage			1		V_{PP}
–3dB Bandwidth			30		MHz
Slew Rate			300		V/µs
Output Signal Range	$R_L \geq$ 500Ω Each Side to Ground		2.5 ±1		V
Output Impedance			1		Ω
Output Short-Circuit Current			±40		mA
3rd-Harmonic Distortion	V_{OUT} = $2V_{PP}$, VCA_{CNTL} = 3.0V	–45	–50		dBc
2nd-Harmonic Distortion	V_{OUT} = $2V_{PP}$, VCA_{CNTL} = 3.0V	–42	–50		dBc
2nd-Harmonic Distortion	V_{OUT} = $2V_{PP}$, VCA_{CNTL} = 3.0V, MGS = 011		–60		dBc
Overload Performance (2nd-Harmonic Distortion)	Input Signal = $1V_{PP}$, VCA_{CNTL} = 2V		–40 to –45		dB
Time Delay			5		ns
IMD, 2-Tone	V_{OUT} = $2V_{PP}$, f = 9.95MHz		–59		dBc
Crosstalk			65		dB
Group Delay Variation	1MHz < f < 10MHz, Full Gain Range		13		ns
ACCURACY					
Gain Slope	VCA_{CNTL} = 0.2V to 3.0V		16		dB/V
Gain Error[1]	VCA_{CNTL} = 0.2V to 3.0V		±2.0		dB
	VCA_{CNTL} = 0.4V to 2.9V		±1.3	±2	dB
Output Offset Voltage			±50		mV
GAIN CONTROL INTERFACE					
Input Voltage (VCA_{CNTL}) Range			0.2 to 3.0		V
Input Resistance			1		MΩ
Response Time	45dB Gain Change		0.2		µs
POWER SUPPLY					
Specified Operating Range		4.75	5.0	5.25	V
Power Dissipation	Operating, Each Channel		120	150	mW
Power-Down			9.2		mW

NOTE: (1) Referenced to best fit dB-linear curve.

PIN CONFIGURATION


Top View
TQFP
VCA2618
1 $+IN_A$
2 NC
3 V_{DDR}
4 V_{BIAS}
5 V_{CM}
6 GND_R
7 NC
8 $+IN_B$
9 NC
10 DNC
11 C_{P2B}
12 C_{P1B}
13 V_{DDB}
14 GND_B
15 P_{OUTB}
16 N_{OUTB}
17 DNC
18 NC
19 NC
20 $\overline{PD}$
21 MGS_1
22 MGS_2
23 MGS_3
24 VCA_{CNTL}
25 N_{OUTA}
26 P_{OUTA}
27 GND_A
28 V_{DDA}
29 C_{P1A}
30 C_{P2A}
31 DNC
32 NC

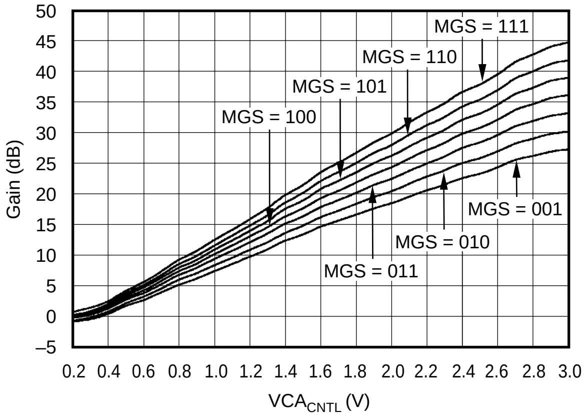
PIN DESCRIPTIONS

PIN	DESIGNATOR	DESCRIPTION	PIN	DESIGNATOR	DESCRIPTION
1	$+IN_A$	Noninverting Input Channel A	17	DNC	Do Not Connect
2	NC	No Internal Connection	18	NC	No Internal Connection
3	V_{DDR}	Internal Reference Supply	19	NC	No Internal Connection
4	V_{BIAS}	Bias Voltage	20	$\overline{PD}$	Power-Down (Active LOW)
5	V_{CM}	Common-Mode Voltage	21	MGS_1	Maximum Gain Select 1 (MSB)
6	GND_R	Internal Reference Ground	22	MGS_2	Maximum Gain Select 2
7	NC	Not Connected	23	MGS_3	Maximum Gain Select 3 (LSB)
8	$+IN_B$	Noninverting Input Channel B	24	VCA_{CNTL}	VCA Analog Control
9	NC	No Internal Connection	25	N_{OUTA}	Negative VCA Output Channel A
10	DNC	Do Not Connect	26	P_{OUTA}	Positive VCA Output Channel A
11	C_{P2B}	Coupling Capacitor Channel B	27	GND_A	Ground Channel A
12	C_{P1B}	Coupling Capacitor Channel B	28	V_{DDA}	+5V Supply Channel A
13	V_{DDB}	+5V Supply Channel B	29	C_{P1A}	Coupling Capacitor Channel A
14	GND_B	Ground Channel B	30	C_{P2A}	Coupling Capacitor Channel A
15	P_{OUTB}	Positive Output Channel B	31	DNC	Do Not Connect
16	N_{OUTB}	Negative Output Channel B	32	NC	No Internal Connection

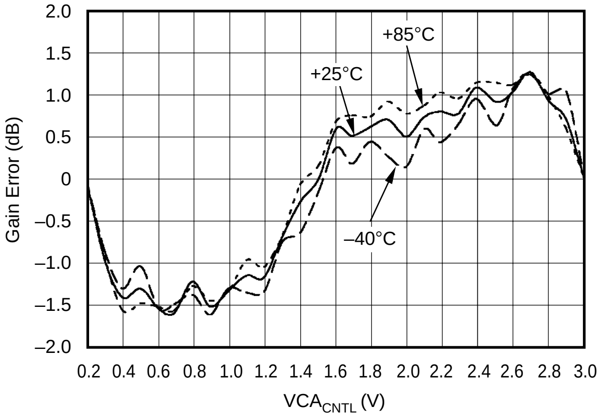
TYPICAL CHARACTERISTICS

At T_A = +25°C, V_{DD} = 5V, load resistance = 500Ω on each output to ground, differential output ($2V_{PP}$) MGS = 111, and f_{IN} = 5MHz, unless otherwise noted.

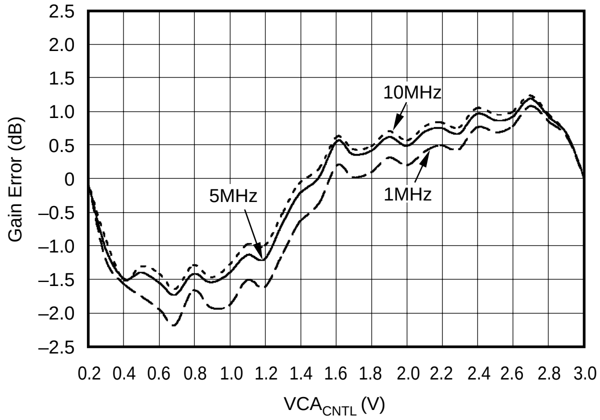
GAIN vs VCA



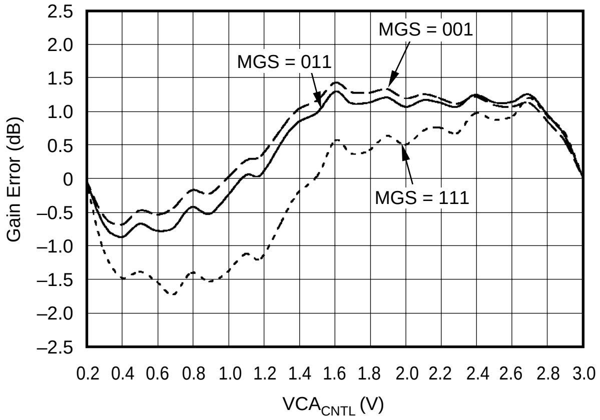
GAIN ERROR vs TEMPERATURE



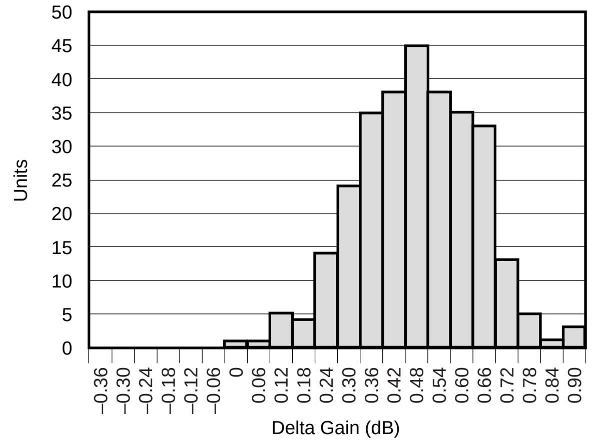
GAIN ERROR vs VCA$_{CNTL}$



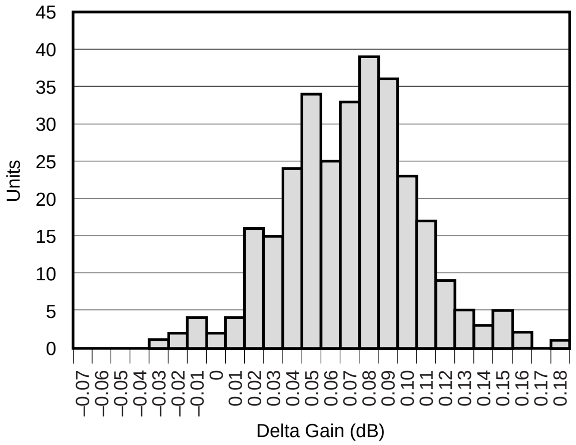
GAIN ERROR vs VCA$_{CNTL}$



GAIN MATCH: CHA to CHB, VCA$_{CNTL}$ = 0.2V

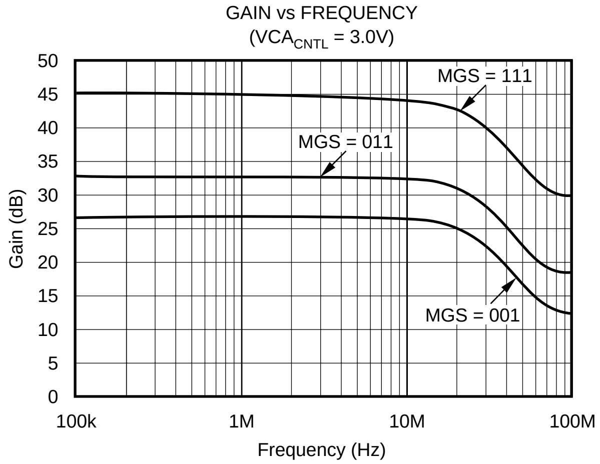


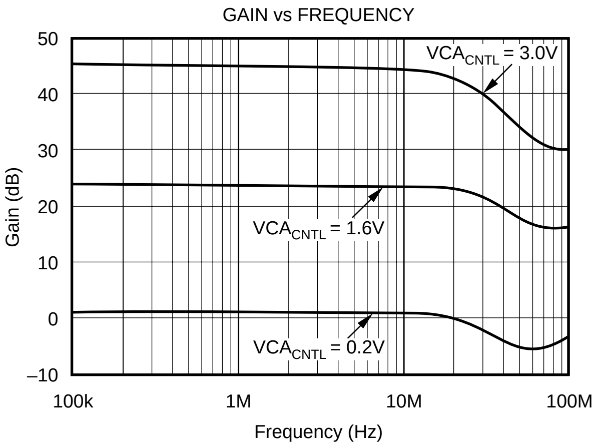
GAIN MATCH: CHA to CHB, VCA$_{CNTL}$ = 3.0V

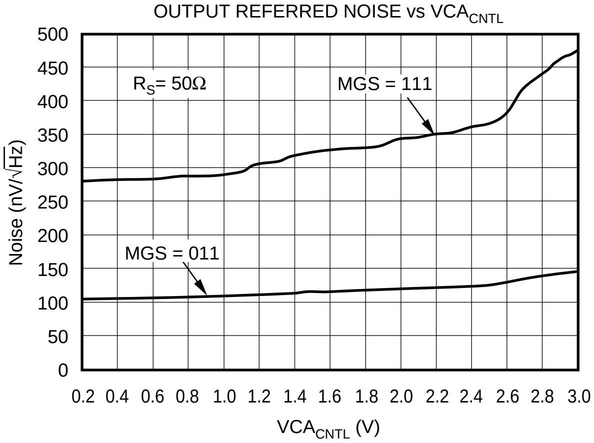


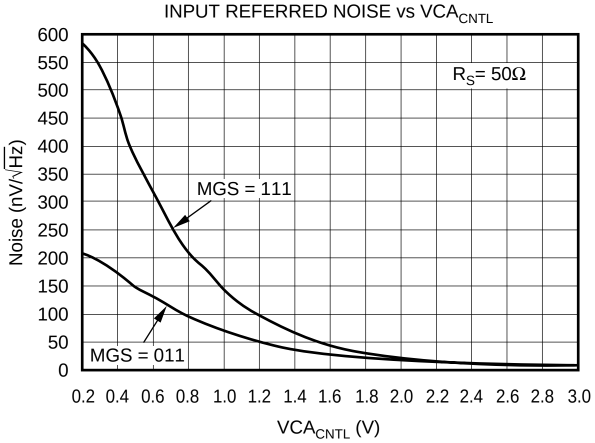
TYPICAL CHARACTERISTICS (Cont.)

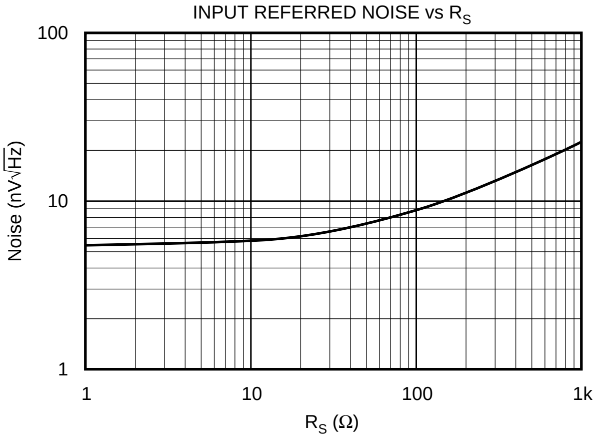
At T_A = +25°C, V_{DD} = 5V, load resistance = 500Ω on each output to ground, differential output ($2V_{PP}$) MGS = 111, and f_{IN} = 5MHz, unless otherwise noted.

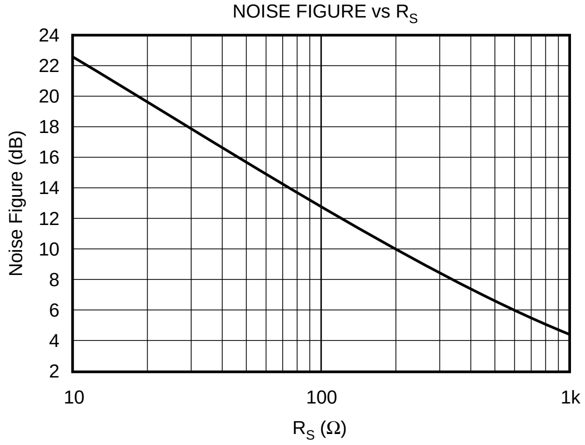

GAIN vs FREQUENCY
(VCA_{CNTL} = 3.0V)


GAIN vs FREQUENCY


OUTPUT REFERRED NOISE vs VCA_{CNTL}


INPUT REFERRED NOISE vs VCA_{CNTL}

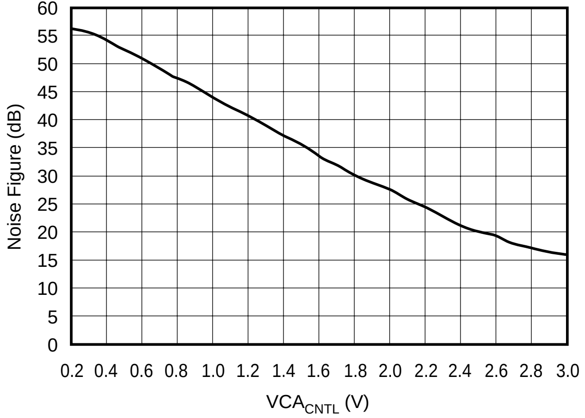

INPUT REFERRED NOISE vs R_S


NOISE FIGURE vs R_S

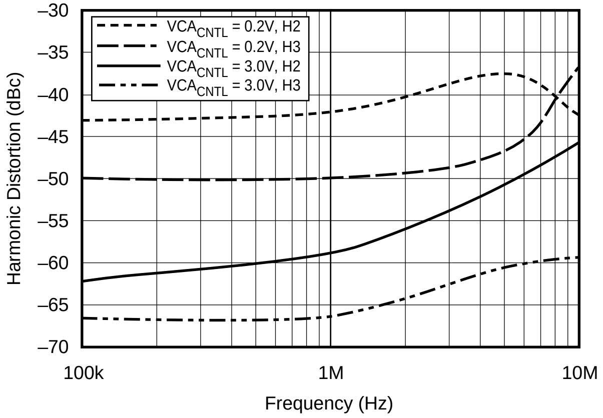
TYPICAL CHARACTERISTICS (Cont.)

At T_A = +25°C, V_{DD} = 5V, load resistance = 500Ω on each output to ground, differential output ($2V_{PP}$) MGS = 111, and f_{IN} = 5MHz, unless otherwise noted.

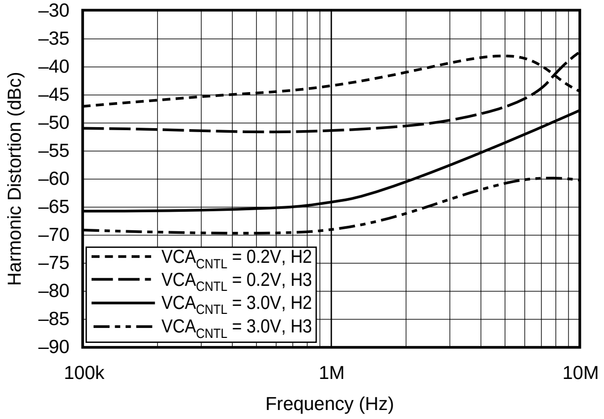
NOISE FIGURE vs VCA_{CNTL}



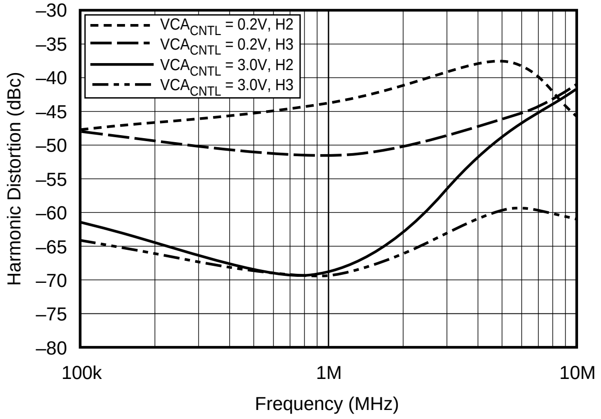
HARMONIC DISTORTION vs FREQUENCY
(Differential, 2Vp-p, MGS = 001)



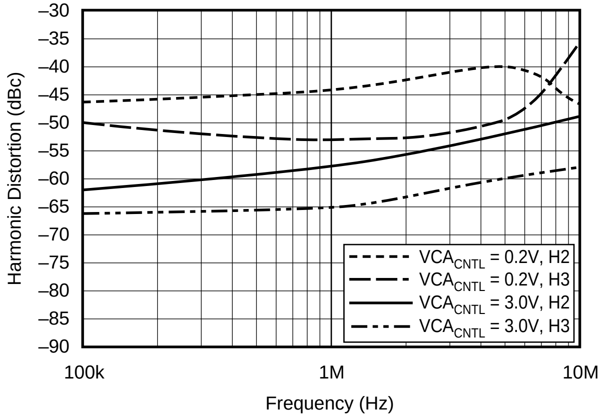
HARMONIC DISTORTION vs FREQUENCY
(Differential, 2Vp-p, MGS = 011)



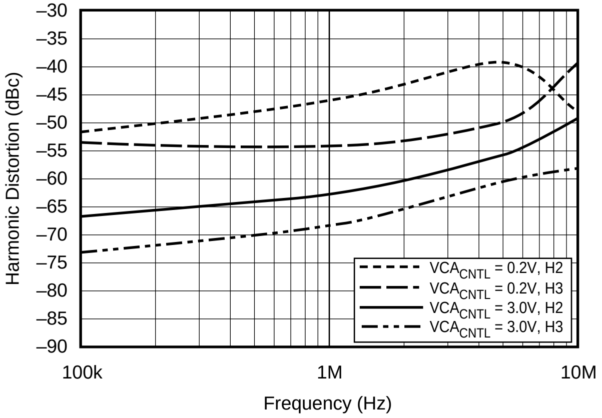
HARMONIC DISTORTION vs FREQUENCY
(Differential, 2Vp-p, MGS = 111)



HARMONIC DISTORTION vs FREQUENCY
(Single-Ended, 1Vp-p, MGS = 001)



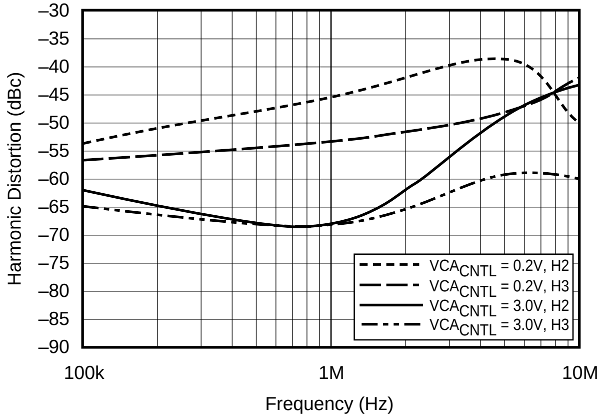
HARMONIC DISTORTION vs FREQUENCY
(Single-Ended, 1Vp-p, MGS = 011)



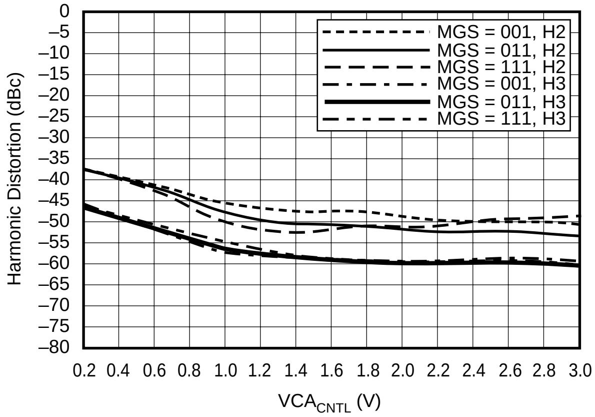
TYPICAL CHARACTERISTICS (Cont.)

At T_A = +25°C, V_{DD} = 5V, load resistance = 500Ω on each output to ground, differential output ($2V_{PP}$) MGS = 111, and f_{IN} = 5MHz, unless otherwise noted.

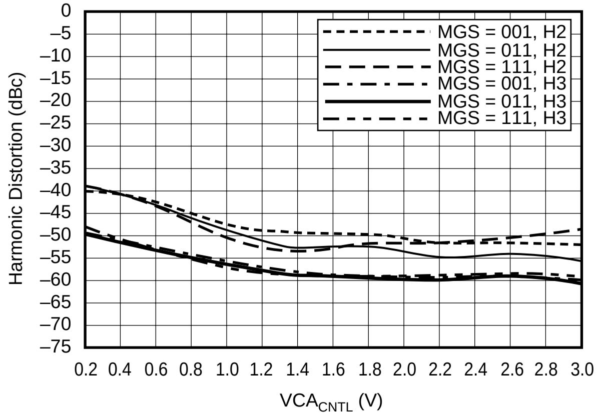
HARMONIC DISTORTION vs FREQUENCY
(Single-Ended, 1Vp-p, MGS = 111)



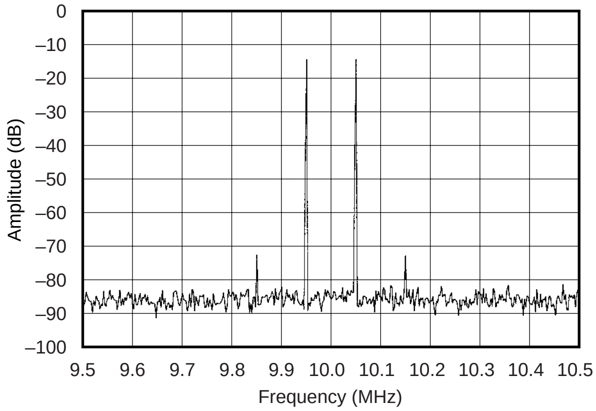
HARMONIC DISTORTION vs VCA_{CNTL}
(Differential, 2Vp-p)



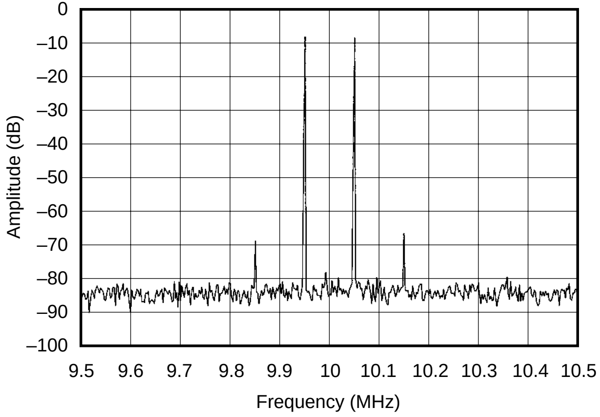
HARMONIC DISTORTION vs VCA_{CNTL}
(Single-Ended, 1Vp-p)



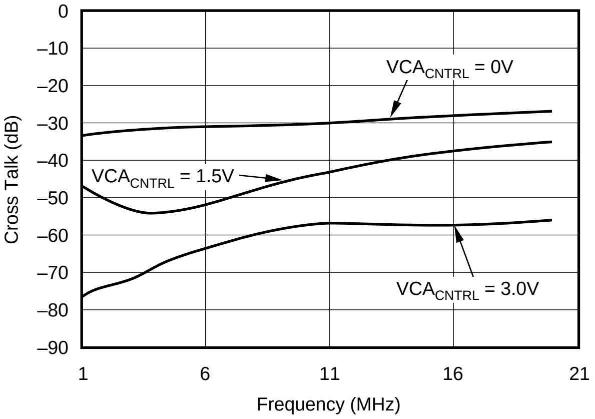
INTERMODULATION DISTORTION
(Single-Ended, 1Vp-p, f_{IN} = 10MHz, VCA_{CNTL} = 3.0V)



INTERMODULATION DISTORTION
(Differential, 2Vp-p, f_{IN} = 10MHz, VCA_{CNTL} = 3.0V)

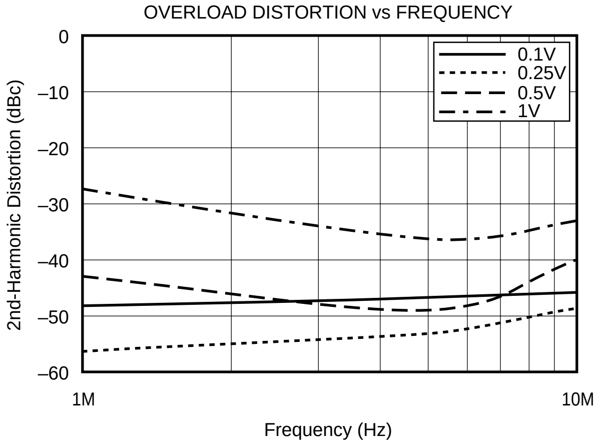


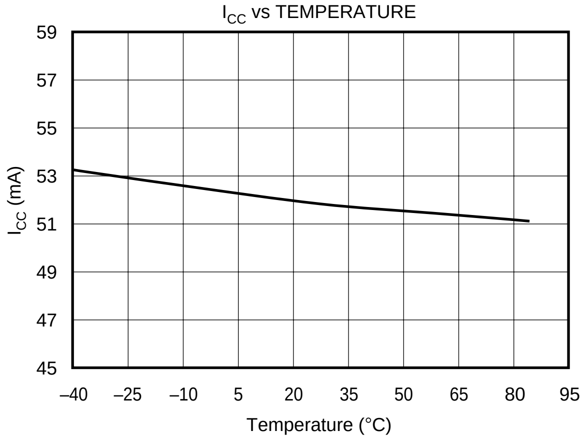
CROSS TALK vs FREQUENCY
(Differential, 2Vp-p, MGS = 011)

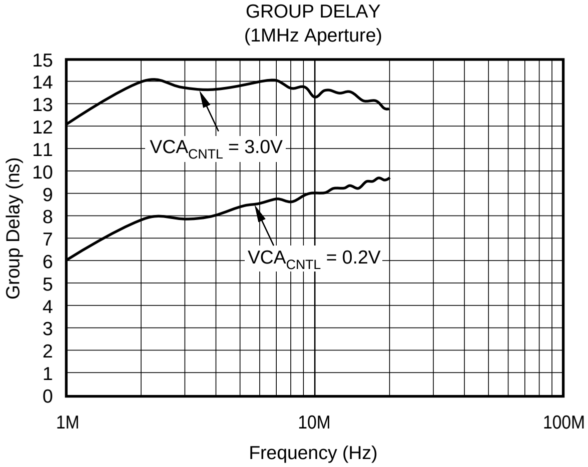


TYPICAL CHARACTERISTICS (Cont.)

At T_A = +25°C, V_{DD} = 5V, load resistance = 500Ω on each output to ground, differential output (2Vp-p) MGS = 111, and f_{IN} = 5MHz, unless otherwise noted.







OVERVIEW

The VCA2618 is a dual-channel, VGA consisting of three primary blocks, an Input Buffer, a VCA, and a PGA. All stages are AC coupled, with the coupling into the PGA stage being made variable by placing an external capacitor between the C_{P1} and C_{P2} pins. This will be discussed further in the PGA section. By using the internal coupling into the PGA, the result is a high-pass filter characteristic with cutoff at approximately 75kHz. The output PGA naturally rolls off at around 30MHz, making the usable bandwidth of the VCA2618 between 75kHz and 30MHz.

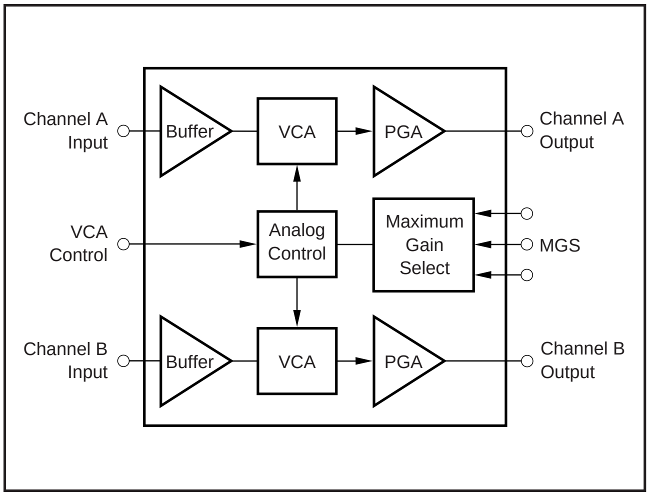


FIGURE 1. Simplified Block Diagram of the VCA2618.

INPUT BUFFER

The input buffer is a unity gain amplifier (gain of +1) with a bandwidth of 100MHz with an input resistance of approximately 600kΩ. The input buffer isolates the circuit driving the VCA2618 inputs from the internal VCA block, which would present a varying impedance to the input circuitry. To allow symmetrical operation of the input buffer, the input to the buffer must be AC coupled through an external capacitor. The recommended value of the capacitor is 0.01µF. It should be noted that if the capacitor value were increased, the power-on time of the VCA2618 would be increased. If a decrease in the power-on time is needed, the value can be decreased to no less than 100pF.

VOLTAGE-CONTROLLED ATTENUATOR

The magnitude of the VCA input signal from the input buffer is reduced by a programmable attenuation factor, set by the analog VCA Control Voltage (VCA_{CNTL}) at pin 24. The maximum attenuation is programmable by using the three MGS bits (pins 21, 22, and 23). Figure 2 illustrates this dual-adjust characteristic.

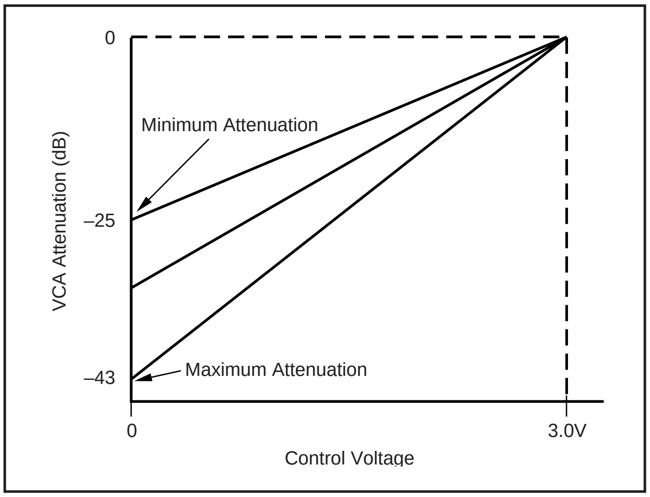


FIGURE 2. Swept Attenuator Characteristic.

The MGS bits adjust the overall range of attenuation and maximum gain while the VCA_{CNTL} voltage adjusts the actual attenuation factor. At any given maximum gain setting, the analog variable gain characteristic is linear in dB as a function of the control voltage, and is created as a piecewise approximation of an ideal dB-linear transfer function. The VCA control circuitry is common to both channels of the VCA2618. The range for the VCA_{CNTL} input spans from 0V to 3V. Although overdriving the VCA_{CNTL} input above the recommended 3V maximum will not damage the part, this condition should be avoided.

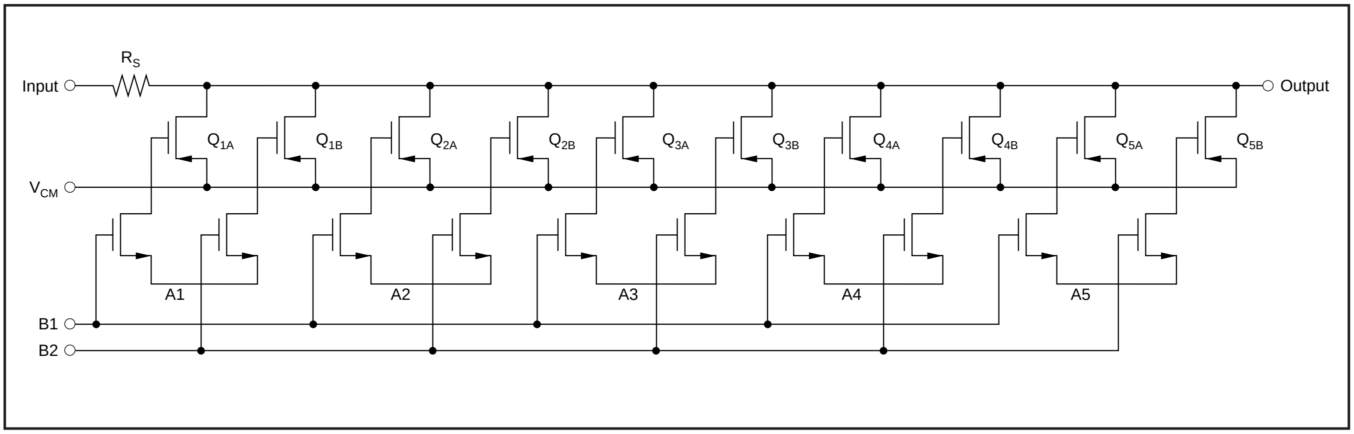


FIGURE 3. Programmable Attenuator Section.

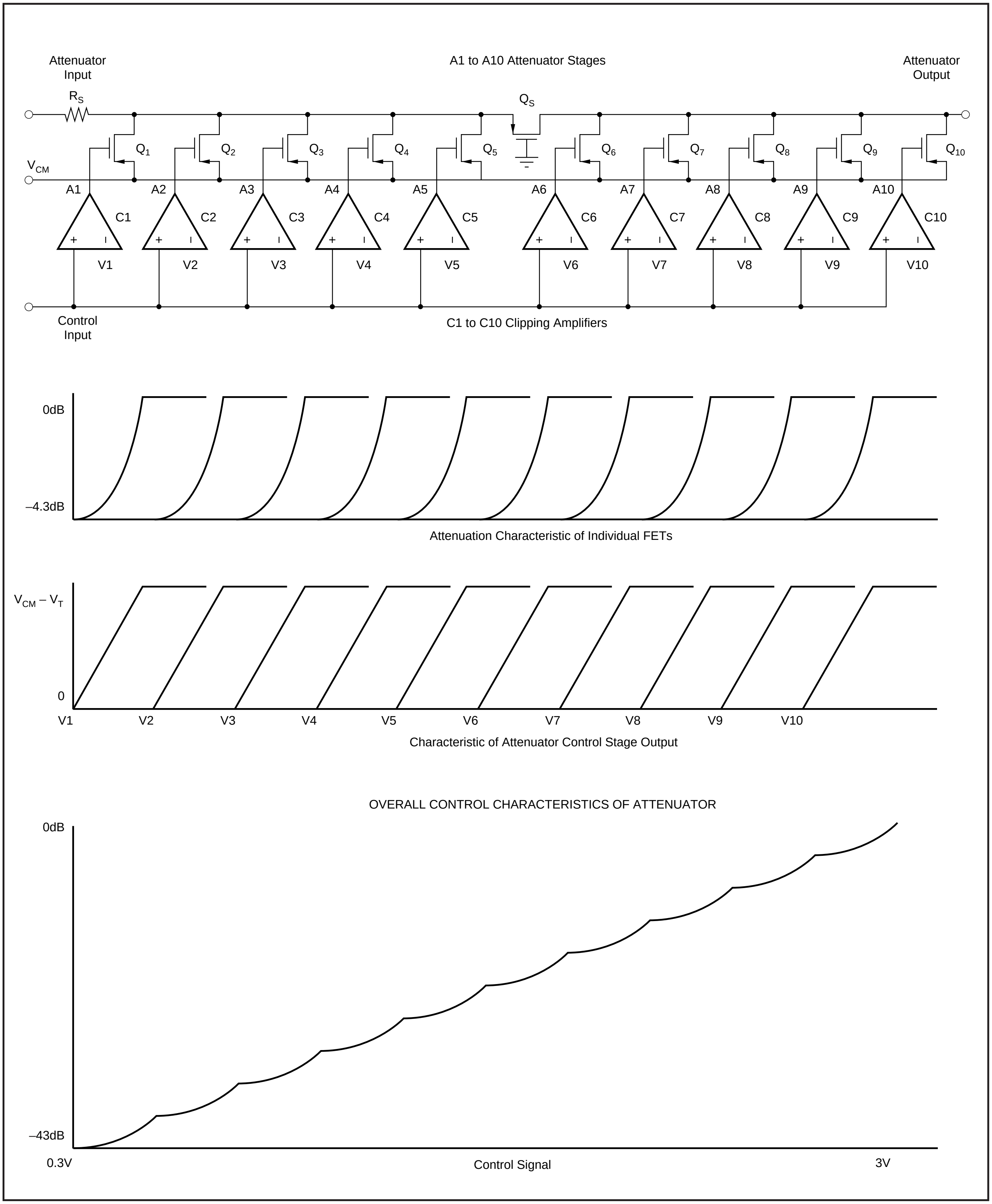

Attenuator Input
A1 to A10 Attenuator Stages
Attenuator Output
R_S
Q_S
V_{CM}
Q_1
Q_2
Q_3
Q_4
Q_5
Q_6
Q_7
Q_8
Q_9
Q_{10}
A1
A2
A3
A4
A5
A6
A7
A8
A9
A10
C1
C2
C3
C4
C5
C6
C7
C8
C9
C10
V1
V2
V3
V4
V5
V6
V7
V8
V9
V10
Control Input
C1 to C10 Clipping Amplifiers
0dB
–4.3dB
Attenuation Characteristic of Individual FETs
$V_{CM} – V_T$
0
V1
V2
V3
V4
V5
V6
V7
V8
V9
V10
Characteristic of Attenuator Control Stage Output
OVERALL CONTROL CHARACTERISTICS OF ATTENUATOR
0dB
–43dB
0.3V
Control Signal
3V

FIGURE 4. Piecewise Approximation to Logarithmic Control Characteristics.

PGA POST-AMPLIFIER

Figure 5 shows a simplified circuit diagram of the PGA block. As stated before, the input to the PGA is AC coupled by an internal capacitor. Provisions are made so that an external capacitor can be placed in parallel with the internal capacitor, thus lowering the usable low-frequency bandwidth. The low-frequency bandwidth is set by the following equation:

$$\frac{1}{\left(2 \bullet \pi \bullet 500k\Omega \bullet \left(220pF + C_{EXTERNAL}\right)\right)}$$

where $C_{EXTERNAL}$ is the external capacitor value in farads.

Care should be taken to avoid using too large a value of capacitor, as this can increase the power-on delay time.

As described previously, the PGA gain is programmed with the same MGS bits that control the VCA maximum attenuation factor. Specifically, the maximum PGA gain at each MGS setting is the inverse (reciprocal) of the maximum VCA attenuation at that setting. Therefore, the VCA + PGA overall gain will always be 0dB (unity) when the analog VCA_{CNTL} input is set to 0V (the maximum attenuation for VCA). For VCA_{CNTL} = 3V (no attenuation), the VCA + PGA gain will be controlled by the programmed PGA gain (25dB to 43dB in 3dB steps). For clarity, the gain and attenuation factors are detailed in Table I.

MGS SETTING	ATTENUATOR GAIN VCA_{CNTL} = 0V to 3V	ATTENUATOR + DIFFERENTIAL PGA GAIN
000	Not Valid	Not Valid
001	–25dB to 0dB	0dB to 25dB
010	–28dB to 0dB	0dB to 28dB
011	–31dB to 0dB	0dB to 31dB
100	–34dB to 0dB	0dB to 34dB
101	–37dB to 0dB	0dB to 37dB
110	–40dB to 0dB	0dB to 40dB
111	–43dB to 0dB	0dB to 43dB

TABLE I. MGS Settings.

The PGA architecture converts the single-ended signal from the VCA into a differential signal. Low input noise was also a requirement of the PGA design due to the large amount of signal attenuation that can be asserted before the PGA. At minimum VCA attenuation (used for small input signals), the input buffer noise dominates; at maximum VCA attenuation (large input signals), the PGA noise dominates. Note that if the PGA output is used single-ended, the apparent gain will be 6dB lower.

LAYOUT CONSIDERATIONS

The VCA2618 is an analog amplifier capable of high gain. When working on a PCB layout for the VCA2618, it is recommended to utilize a solid ground plane that is connected to analog ground. This helps to maximize the noise performance of the VCA2618.

Adequate power-supply decoupling must be used in order to achieve the best possible performance. Decoupling capacitors on the VCA_{CNTL} voltage should also be used to help minimize noise. Recommended values can be obtained from the layout diagram of Figure 6.

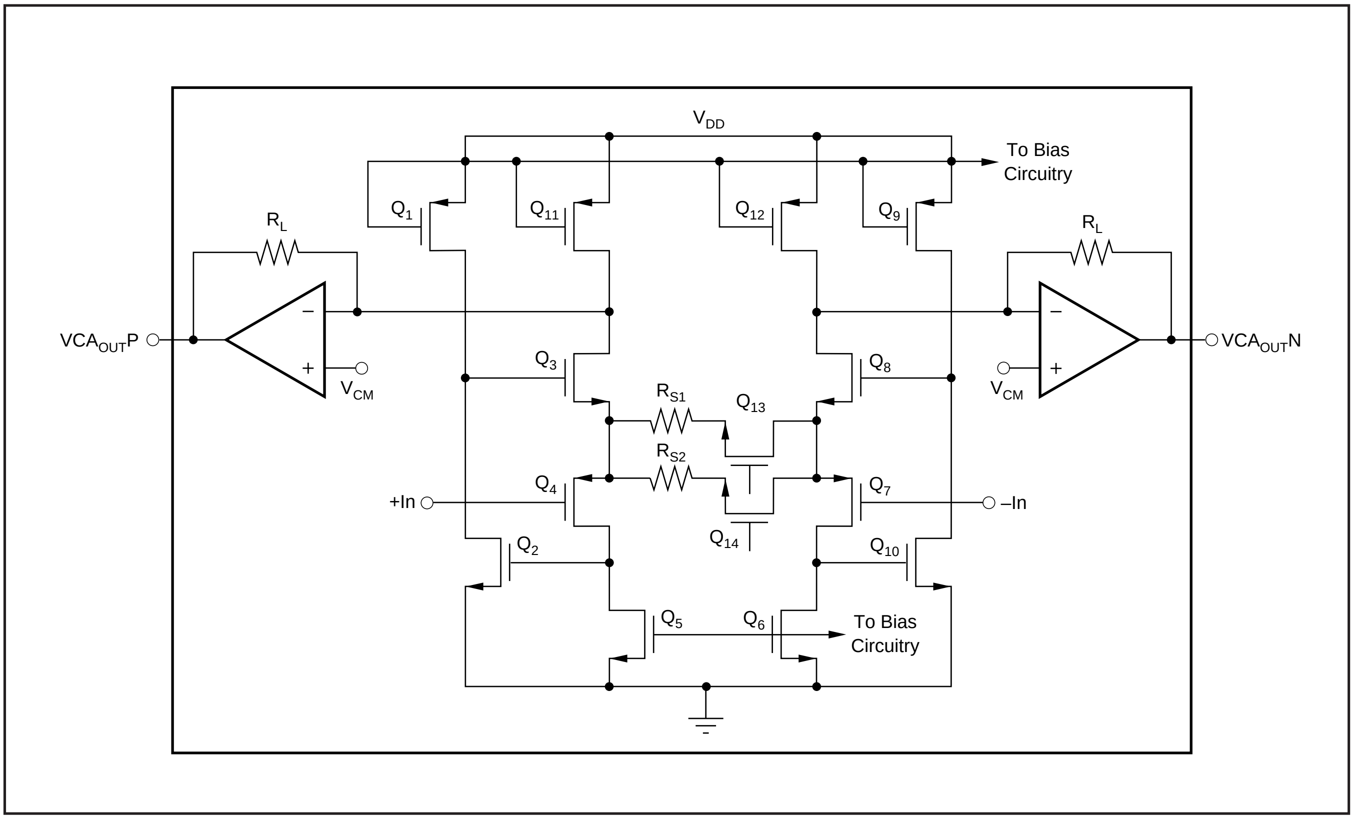


FIGURE 5. Simplified Block Diagram of the PGA Section with the VCA2618.

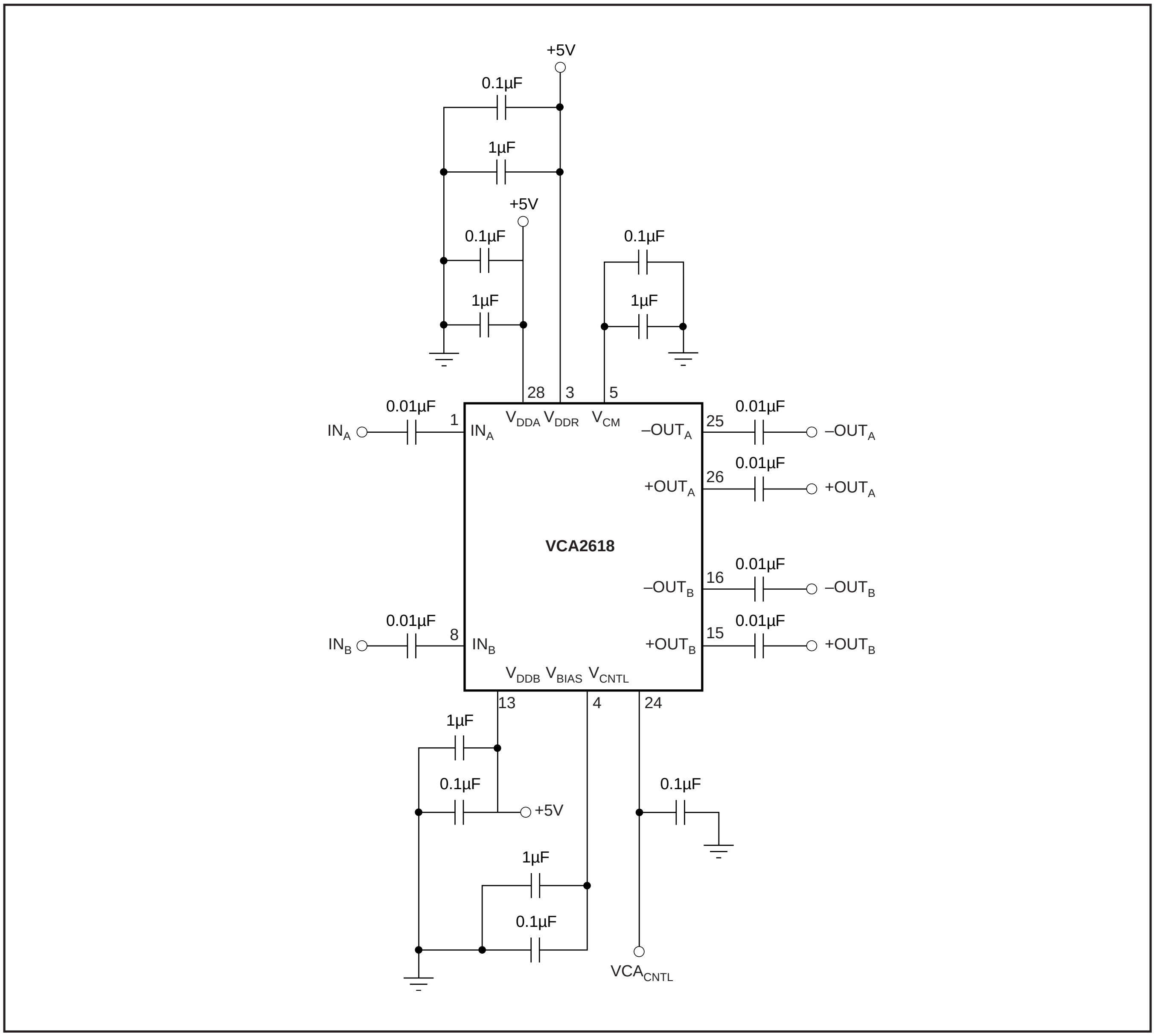

+5V
0.1µF
1µF
+5V
0.1µF
1µF
0.1µF
1µF
28
3
5
0.01µF
1
IN_A
IN_A
V_{DDA}
V_{DDR}
V_{CM}
$-OUT_A$
25
0.01µF
$-OUT_A$
26
0.01µF
$+OUT_A$
$+OUT_A$
VCA2618
16
0.01µF
$-OUT_B$
$-OUT_B$
0.01µF
8
IN_B
IN_B
15
0.01µF
$+OUT_B$
$+OUT_B$
V_{DDB}
V_{BIAS}
V_{CNTL}
13
4
24
1µF
0.1µF
+5V
0.1µF
1µF
0.1µF
VCA_{CNTL}

FIGURE 6. VCA2618 Layout.

PACKAGE OPTION ADDENDUM

PACKAGING INFORMATION

Orderable Device	Status [1]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [2]	Lead/Ball Finish	MSL Peak Temp [3]
VCA2618YT	ACTIVE	TQFP	PBS	32	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR

[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

[3] MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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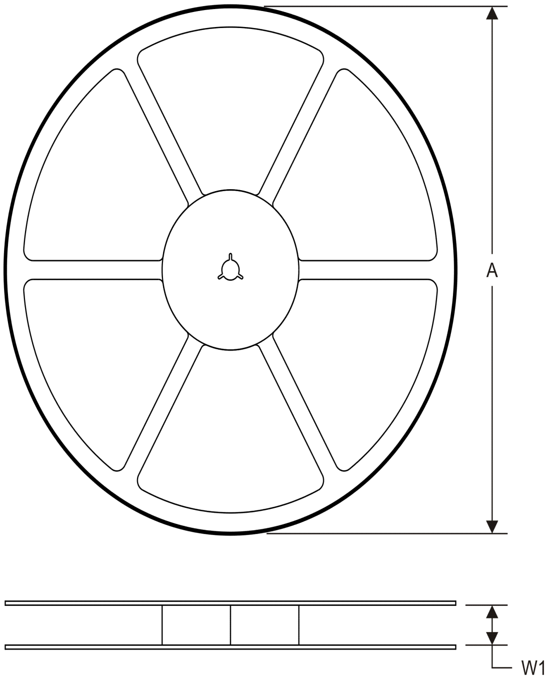
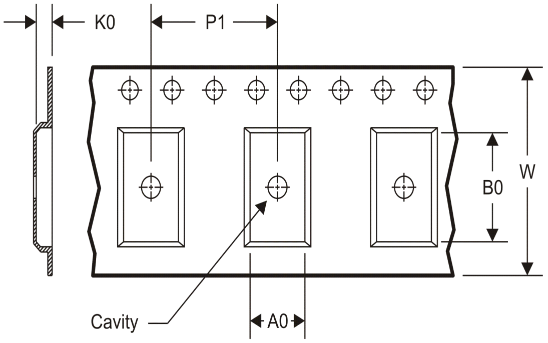
TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



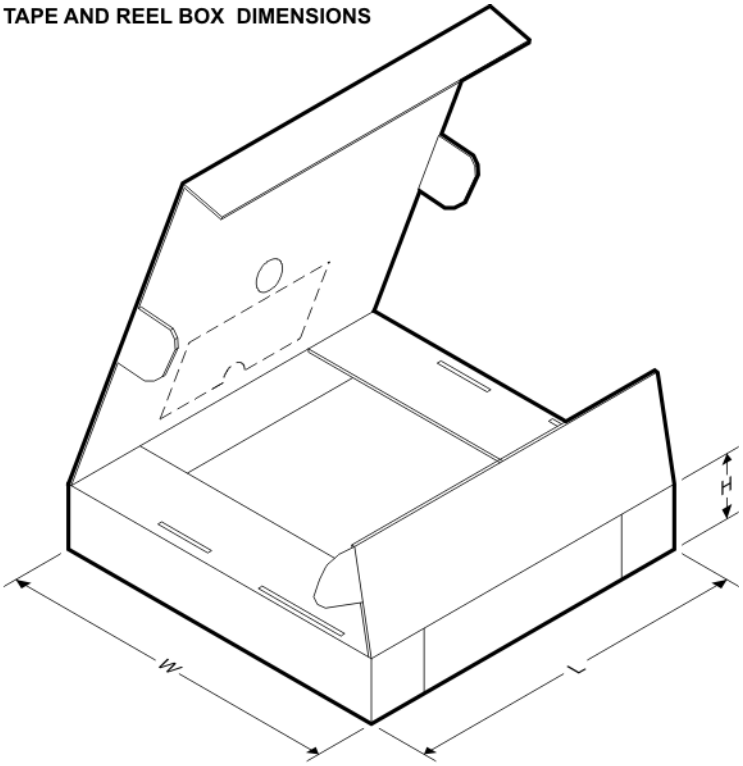
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
VCA2618YT	TQFP	PBS	32	250	177.8	16.4	7.2	7.2	1.5	12.0	16.0	Q2

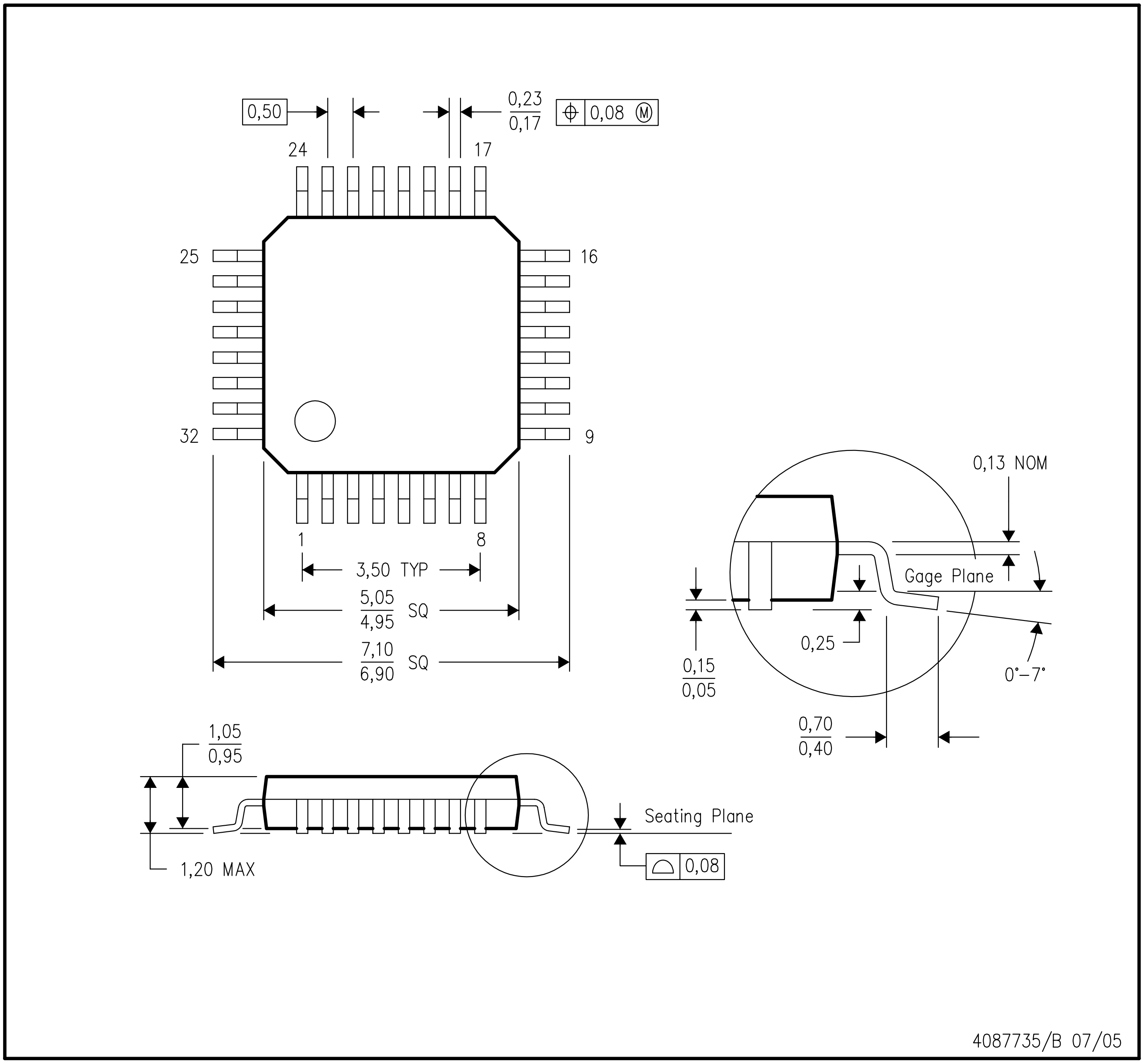
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

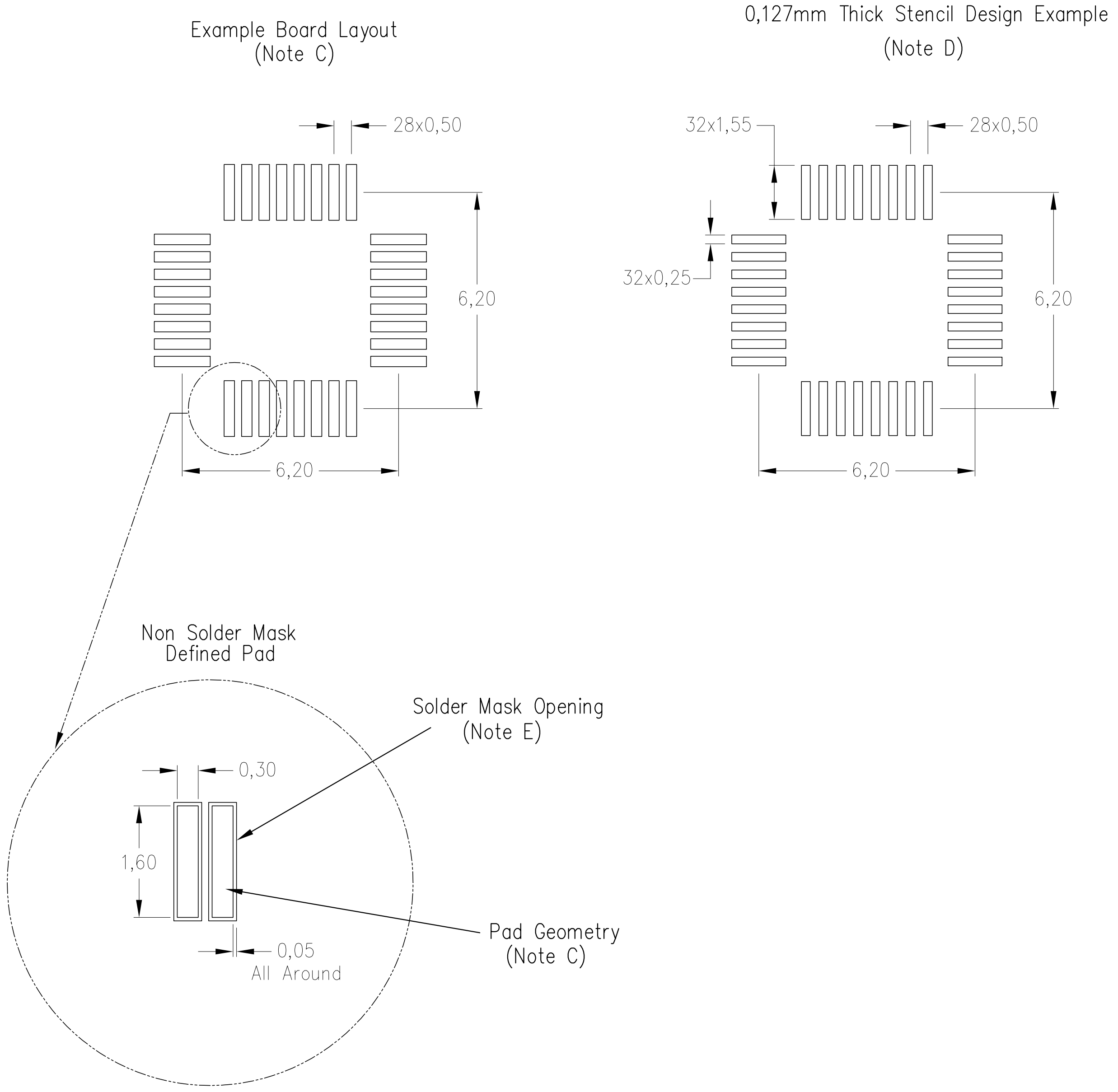
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
VCA2618YT	TQFP	PBS	32	250	210.0	185.0	35.0

PBS (S–PQFP–G32) PLASTIC QUAD FLATPACK


0,50
0,23
0,17
⌖ 0,08 Ⓜ
24
17
25
16
32
9
1
8
3,50 TYP
5,05
4,95
SQ
7,10
6,90
SQ
0,13 NOM
Gage Plane
0,25
0,15
0,05
0°–7°
0,70
0,40
1,05
0,95
1,20 MAX
Seating Plane
⌓ 0,08
4087735/B 07/05

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.

PBS (S–PQFP–G32) PLASTIC QUAD FLATPACK


Example Board Layout
(Note C)
28x0,50
6,20
6,20
0,127mm Thick Stencil Design Example
(Note D)
32x1,55
28x0,50
32x0,25
6,20
6,20
Non Solder Mask
Defined Pad
Solder Mask Opening
(Note E)
0,30
1,60
0,05
All Around
Pad Geometry
(Note C)

4212229/A 10/11

NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC–7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
- E. Customers should contact their board fabrication site for recommended solder mask tolerances between and around signal pads.

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