NEC

MOS INTEGRATED CIRCUIT

μPD78F0852

8-BIT SINGLE-CHIP MICROCONTROLLER

The μPD78F0852 is a product of the μPD780852 Subseries in the 78K/0 Series.

The μPD78F0852 has flash memory in place of the internal ROM of the μPD780852(A).

The flash memory incorporated enables program writing or erasing with the microcontroller mounted on the target board.

Detailed function descriptions are provided in the following user's manuals. Be sure to read them before designing.

μPD780852 Subseries User's Manual: U14581E
78K/0 Series User's Manual Instruction: U12326E

FEATURES

- Pin compatible with mask ROM versions (except V_{PP} pin)
- Flash memory: 40 KB[Note]
- Internal high-speed RAM: 1024 bytes
- Internal expansion RAM: 512 bytes
- Operable within the same supply voltage range as that of the mask ROM version (V_{DD} = 4.0 to 5.5 V)

Note The flash memory capacitance can be changed using the internal memory size switching register (IMS)

Remark For differences between the flash memory versions and mask ROM versions, refer to **1. DIFFERENCES BETWEEN μPD78F0852 AND MASK ROM VERSIONS**.

APPLICATIONS

Automobile meter (dashboard) control

ORDERING INFORMATION

Part Number	Package	Internal ROM
μPD78F0852GC-8BT	80-pin plastic QFP (14 × 14)	Flash memory

The information in this document is subject to change without notice. Before using this document, please confirm that this is the latest version.
Not all devices/types available in every country. Please check with local NEC representative for availability and additional information.

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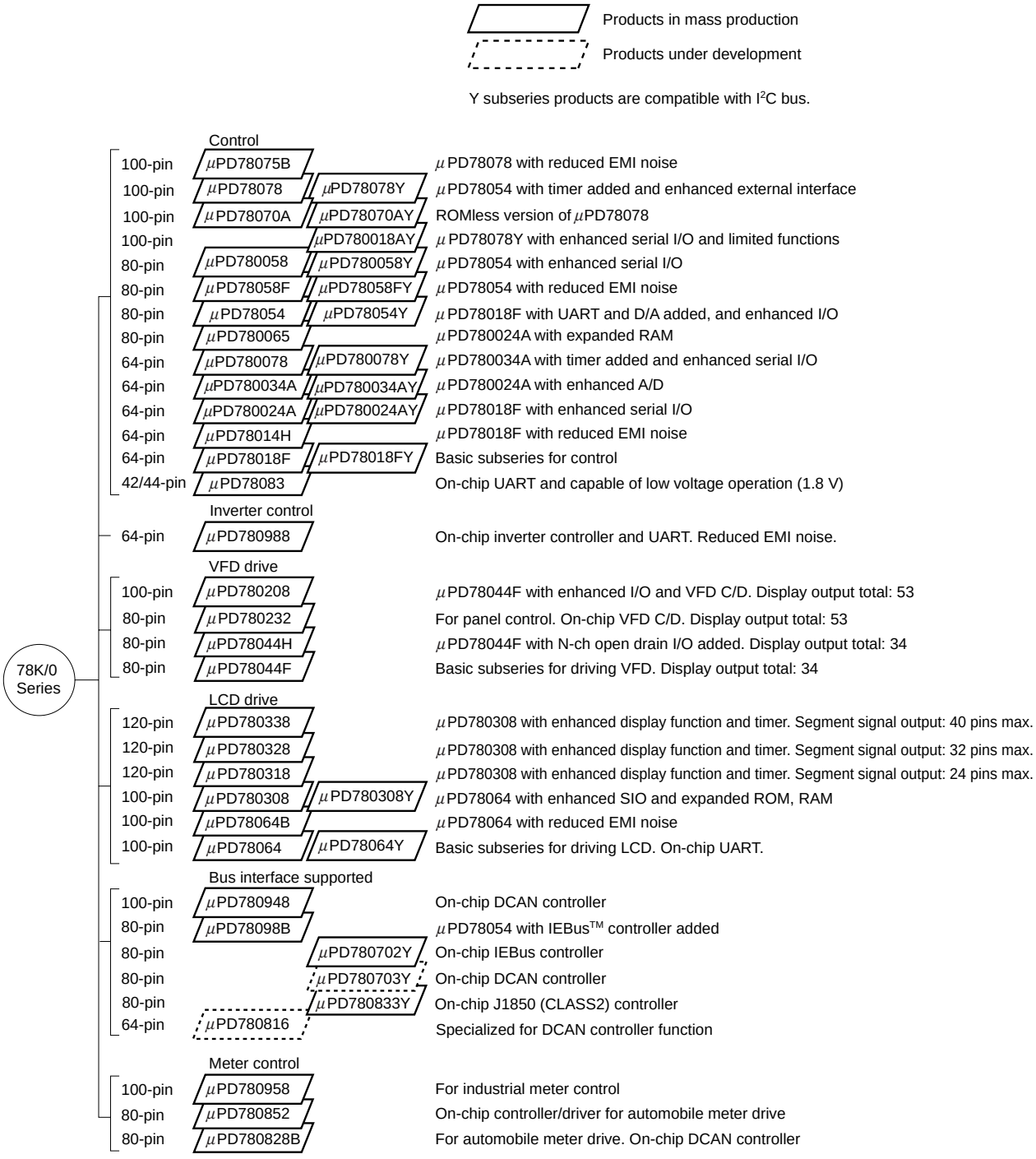
The mark ★ shows major revised points.

78K/0 SERIES LINEUP

The products in the 78K/0 Series are listed below. The names enclosed in boxes are subseries names.



Remark VFD (Vacuum Fluorescent Display) is referred to as FIP™ (Fluorescent Indicator Panel) in some documents, but the functions of the two are the same.

The major functional differences among the subseries are listed below.

Subseries Name \ Function		ROM Capacity	Timer				8-Bit A/D	10-Bit A/D	8-Bit D/A	Serial Interface	I/O	V_{DD} MIN. Value	External Expansion
			8-Bit	16-Bit	Watch	WDT							
Control	μPD78075B	32 K to 40 K	4 ch	1 ch	1 ch	1 ch	8 ch	–	2 ch	3 ch (UART: 1 ch)	88	1.8 V	√
	μPD78078	48 K to 60 K											
	μPD78070A	–									61	2.7 V	
	μPD780058	24 K to 60 K	2 ch							3 ch (time-division UART: 1 ch)	68	1.8 V	
	μPD78058F	48 K to 60 K								3 ch (UART: 1 ch)	69	2.7 V	
	μPD78054	16 K to 60 K										2.0 V	
	μPD780065	40 K to 48 K							–	4 ch (UART: 1 ch)	60	2.7 V	
	μPD780078	48 K to 60 K		2 ch			–	8 ch		3 ch (UART: 2 ch)	52	1.8 V	
	μPD780034A	8 K to 32 K		1 ch						3 ch (UART: 1 ch)	51		
	μPD780024A						8 ch	–					
	μPD78014H									2 ch	53		
	μPD78018F	8 K to 60 K											
	μPD78083	8 K to 16 K		–	–					1 ch (UART: 1 ch)	33		–
Inverter control	μPD780988	16 K to 60 K	3 ch	**Note**	–	1 ch	–	8 ch	–	3 ch (UART: 2 ch)	47	4.0 V	√
VFD drive	μPD780208	32 K to 60 K	2 ch	1 ch	1 ch	1 ch	8 ch	–	–	2 ch	74	2.7 V	–
	μPD780232	16 K to 24 K	3 ch	–	–		4 ch				40	4.5 V	
	μPD78044H	32 K to 48 K	2 ch	1 ch	1 ch		8 ch			1 ch	68	2.7 V	
	μPD78044F	16 K to 40 K								2 ch			
LCD drive	μPD780338	48 K to 60 K	3 ch	2 ch	1 ch	1 ch	–	10 ch	1 ch	2 ch (UART: 1 ch)	54	1.8 V	–
	μPD780328										62		
	μPD780318										70		
	μPD780308		2 ch	1 ch			8 ch	–	–	3 ch (time-division UART: 1 ch)	57	2.0 V	
	μPD78064B	32 K								2 ch (UART: 1 ch)			
	μPD78064	16 K to 32 K											
Bus interface supported	μPD780948	60 K	2 ch	2 ch	1 ch	1 ch	8 ch	–	–	3 ch (UART: 1 ch)	79	4.0 V	√
	μPD78098B	40 K to 60 K		1 ch					2 ch		69	2.7 V	–
	μPD780816	32 K to 60 K		2 ch			12 ch		–	2 ch (UART: 1 ch)	46	4.0 V	
Meter control	μPD780958	48 K to 60 K	4 ch	2 ch	–	1 ch	–	–	–	2 ch (UART: 1 ch)	69	2.2 V	–
Dash-board control	μPD780852	32 K to 40 K	3 ch	1 ch	1 ch	1 ch	5 ch	–	–	3 ch (UART: 1 ch)	56	4.0 V	–
	μPD780828B	32 K to 60 K									59		

Note 16-bit timer: 2 channels
10-bit timer: 1 channel

OVERVIEW OF FUNCTIONS

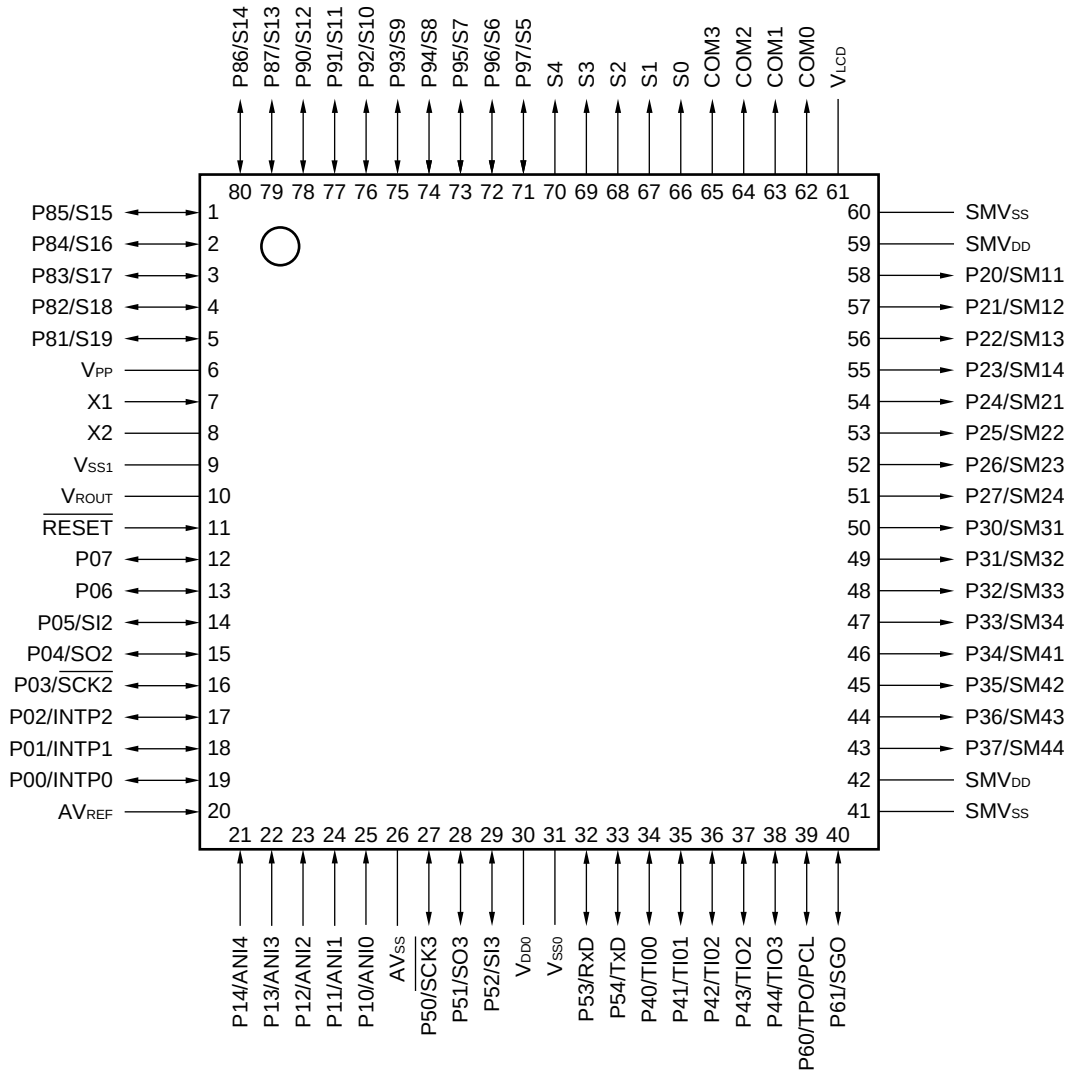
Item		Function
Internal memory	Flash memory	40 KB[Note]
	High-speed RAM	1024 bytes
	Expansion RAM	512 bytes
	RAM for LCD display	20 × 4 bits
General-purpose registers		8 bits × 32 registers (8 bits × 8 registers × 4 banks)
Minimum instruction execution time		On-chip minimum instruction execution time variable function 0.24 μs/0.48 μs/0.95 μs/1.91 μs/3.81 μs (@ 8.38 MHz operation)
Instruction set		• 16-bit operation • Multiply/divide (8 bits × 8 bits, 16 bits ÷ 8 bits) • Bit manipulation (set, reset, test, Boolean operation) • BCD adjust, etc.
I/O ports (segment signal output alternate-function pins included)		Total: 56 • CMOS input: 5 • CMOS output: 16 • CMOS I/O: 35
A/D converter		• 8-bit resolution × 5 channels • Power-fail detection function
LCD controller/driver		• Segment signal outputs: Max. 20 • Common signal outputs: Max. 4 • Bias: 1/3 bias only
Serial interface		• 3-wire serial I/O mode: 2 channels • UART mode: 1 channel
Timer		• 16-bit timer: 1 channel • 8-bit timer: 1 channel • 8-bit timer/event counter: 2 channels • Watch timer: 1 channel • Watchdog timer: 1 channel
Timer outputs		2 (8-bit PWM output capable: 2)
Meter controller/driver		PWM outputs (8-bit resolution): 16 Pulse width setting of 8 + 1 bit precision is enabled by a 1-bit addition function
Sound generator		1 channel
Clock output		65.5 kHz, 131 kHz, 262 kHz, 524 kHz, 1.04 MHz, 2.09 MHz, 4.19 MHz, 8.38 MHz (@ 8.38 MHz operation with main system clock)
Vectored interrupt sources	Maskable	Internal: 16, External: 3
	Non-maskable	Internal: 1
	Software	1
Supply voltage		V_{DD} = SMV_{DD} = 4.0 to 5.5 V
Operating ambient temperature		T_A = –40 to +85°C
Package		80-pin plastic QFP (14 × 14)

Note The flash memory capacitance can be changed using the internal memory size switching register (IMS).

PIN CONFIGURATION (TOP VIEW)

- 80-pin plastic QFP (14 × 14)

μPD78F0852GC-8BT



Cautions 1. In normal operating mode, connect the V_{PP} pin directly to V_{SS0} or V_{SS1}.

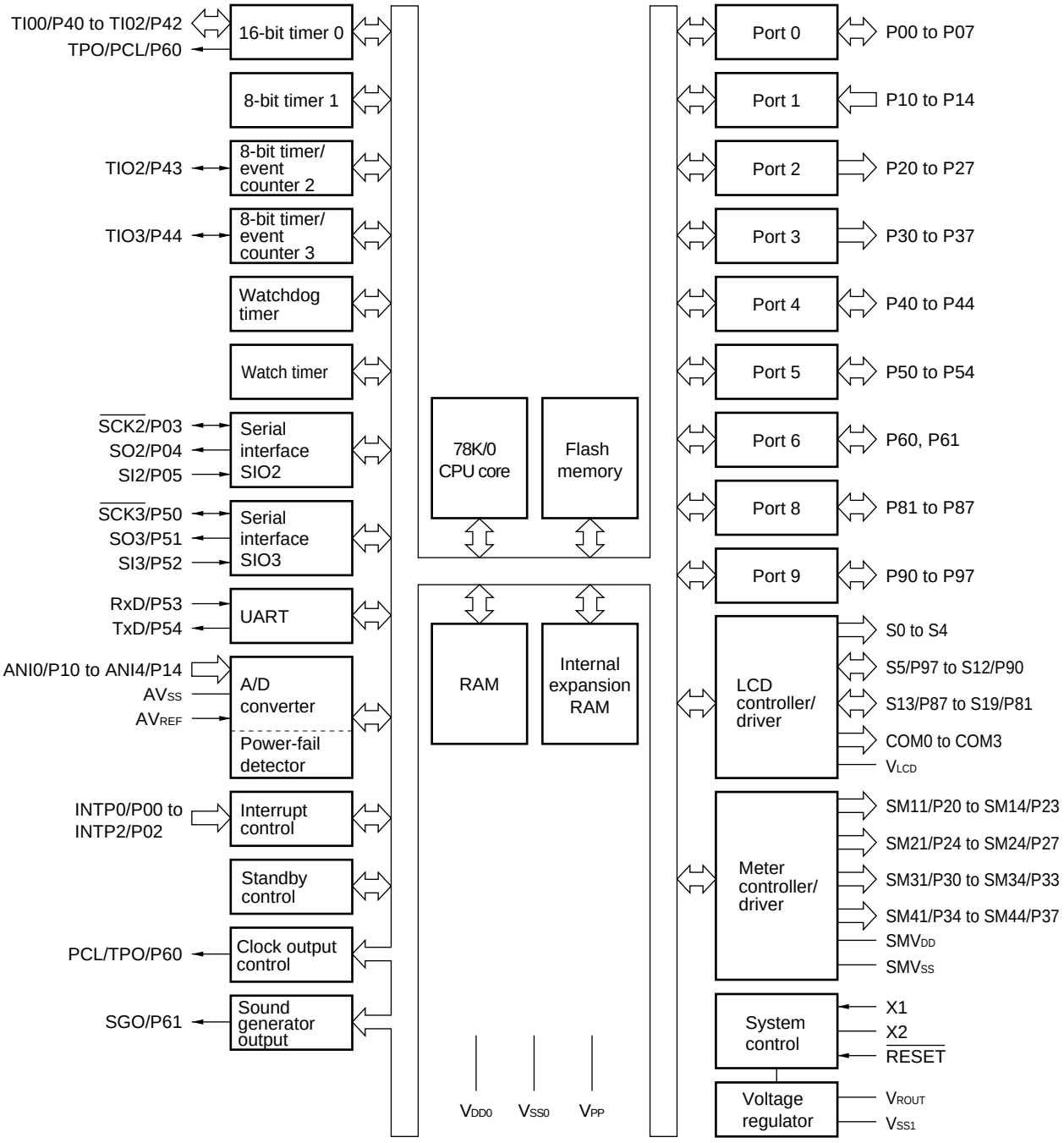
2. Connect the AV_{SS} pin to V_{SS0}.

3. Connect the AV_{REF} pin to V_{DD0}.

Remark When the μPD78F0852 is used in applications where the noise generated inside the microcontroller needs to be reduced, the implementation of noise reduction measures, such as connecting V_{SS0} and V_{SS1} to different ground lines, is recommended.

ANI0 to ANI4:	Analog input	$\overline{SCK2}$, $\overline{SCK3}$:	Serial clock
AV_{REF}:	Analog reference voltage	SGO:	Sound generator output
AV_{SS}:	Analog ground	SI2, SI3:	Serial input
COM0 to COM3:	Common output	SM11 to SM14, SM21 to SM24, SM31 to SM34,	
INTP0 to INTP2:	External interrupt input	SM41 to SM44:	Meter output
P00 to P07:	Port 0	SMV_{DD}:	Meter controller power supply
P10 to P14:	Port 1	SMV_{SS}:	Meter controller ground
P20 to P27:	Port 2	SO2, SO3:	Serial output
P30 to P37:	Port 3	TI00 to TI02:	Timer input
P40 to P44:	Port 4	TIO2, TIO3:	Timer output/event counter input
P50 to P54:	Port 5	TPO:	Prescaler output
P60, P61:	Port 6	TxD:	Transmit data
P81 to P87:	Port 8	V_{DD0}:	Power supply
P90 to P97:	Port 9	V_{LCD}:	LCD power supply
PCL:	Programmable clock output	V_{PP}:	Programming power supply
$\overline{RESET}$:	Reset	V_{ROUT}:	Power supply regulator output
RxD:	Receive data	V_{SS0}, V_{SS1}:	Ground
S0 to S19:	Segment output	X1, X2:	Crystal (main system clock)

BLOCK DIAGRAM



CONTENTS

1. DIFFERENCES BETWEEN μPD78F0852 AND MASK ROM VERSIONS

The μPD78F0852 is a product provided with flash memory, enabling writing, erasing, and rewriting of programs without being removed from the board.

Functions other than the flash memory specification can be unified with those of the mask ROM versions by setting the internal memory size switching register (IMS).

Table 1-1 shows the differences between the flash memory version (μPD78F0852) and mask ROM versions (μPD780851(A) and 780852(A)).

Table 1-1. Differences Between μPD78F0852 and Mask ROM Versions

Item	μPD78F0852	μPD780851(A)	μPD780852(A)
Internal ROM type	Flash memory	Mask ROM	
Internal ROM capacity	40 KB	32 KB	40 KB
IC pin	Not provided	Provided	
V_{PP} pin	Provided	Not provided	
Electrical specifications	Refer to the data sheet of individual products.		
Product quality	Standard (general electrical equipment)	Special (high-reliability electrical equipment)	

2. PIN FUNCTIONS

2.1 Port Pins

Pin Name	I/O	Function	After Reset	Alternate Function
P00 to P02	I/O	Port 0 8-bit I/O port Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by software.	Input	INTP0 to INTP2
P03				$\overline{SCK2}$
P04				SO2
P05				SI2
P06, P07				–
P10 to P14	Input	Port 1 5-bit input-only port	Input	ANI0 to ANI4
P20 to P23	Output	Port 2 8-bit output-only port	Hi-Z	SM11 to SM14
P24 to P27				SM21 to SM24
P30 to P33	Output	Port 3 8-bit output-only port	Hi-Z	SM31 to SM34
P34 to P37				SM41 to SM44
P40 to P42	I/O	Port 4 5-bit I/O port Input/output can be specified in 1-bit units.	Input	TI00 to TI02
P43, P44				TIO2, TIO3
P50	I/O	Port 5 5-bit I/O port Input/output can be specified in 1-bit units.	Input	$\overline{SCK3}$
P51				SO3
P52				SI3
P53				RxD
P54				TxD
P60	I/O	Port 6 2-bit I/O port Input/output can be specified in 1-bit units.	Input	PCL/TPO
P61				SGO
P81 to P87	I/O	Port 8 7-bit I/O port Input/output can be specified in 1-bit units. The I/O port/segment output function can be specified in 2-bit units using the LCD display control register (LCDC).	Input	S19 to S13
P90 to P97	I/O	Port 9 8-bit I/O port Input/output can be specified in 1-bit units. The I/O port/segment output function can be specified in 2-bit units using the LCD display control register (LCDC).	Input	S12 to S5

2.2 Non-Port Pins

Pin Name	I/O	Function	After Reset	Alternate Function
INTP0 to INTP2	Input	External interrupt request input for which the valid edge (rising edge, falling edge, or both rising and falling edges) can be specified	Input	P00 to P02
SI2	Input	Serial interface SIO2 serial data input	Input	P05
SO2	Output	Serial interface SIO2 serial data output	Input	P04
$\overline{SCK2}$	I/O	Serial interface SIO2 serial clock input/output	Input	P03
SI3	Input	Serial interface SIO3 serial data input	Input	P52
SO3	Output	Serial interface SIO3 serial data output	Input	P51
$\overline{SCK3}$	I/O	Serial interface SIO3 serial clock input/output	Input	P50
RxD	Input	Serial data input for asynchronous serial interface	Input	P53
TxD	Output	Serial data output for asynchronous serial interface	Input	P54
TI00	Input	Capture trigger signal input to capture register (CR00)	Input	P40
TI01		Capture trigger signal input to capture register (CR01)		P41
TI02		Capture trigger signal input to capture register (CR02)		P42
TIO2	I/O	8-bit timer (TM2) I/O (also used for 8-bit PWM output)	Input	P43
TIO3		8-bit timer (TM3) I/O (also used for 8-bit PWM output)		P44
TPO	Output	16-bit timer (TM0) prescaler signal output	Input	PCL/P60
PCL	Output	Clock output (for trimming of main system clock)	Input	TPO/P60
SGO	Output	Sound generator signal output	Input	P61
S0 to S4	Output	LCD controller/driver segment signal output	Output	–
S5 to S12			Input	P97 to P90
S13 to S19				P87 to P81
COM0 to COM3	Output	LCD controller/driver common signal output	Output	–
V_{LCD}	–	Power supply for LCD drive	–	–
SM11 to SM14	Output	Meter control signal output	Hi-Z	P20 to P23
SM21 to SM24				P24 to P27
SM31 to SM34				P30 to P33
SM41 to SM44				P34 to P37
ANI0 to ANI4	Input	A/D converter analog input	Input	P10 to P14
AV_{REF}	Input	A/D converter reference voltage input (also used for analog power supply)	–	–
AV_{SS}	–	A/D converter ground potential. Connect to V_{SS0}	–	–
$\overline{RESET}$	Input	System reset input	–	–
X1	Input	Connecting crystal resonator for main system clock oscillation	–	–
X2	–		–	–
SMV_{DD}	–	Meter controller/driver power supply	–	–
SMV_{SS}	–	Meter controller/driver ground potential	–	–
V_{DD0}	–	Port block positive power supply	–	–
V_{SS0}	–	Port block ground potential	–	–
V_{ROUT}	–	Regulator output pin for positive power supply other than port block. Connect to V_{SS0} or V_{SS1} via a 0.1 μF capacitor	–	–
V_{SS1}	–	Ground potential (other than port block)	–	–
V_{PP}	–	High voltage applied during program write/verify. Connect directly to V_{SS0} or V_{SS1} in normal operating mode	–	–

2.3 Pin I/O Circuits and Recommended Connection of Unused Pins

The I/O circuit type of each pin and recommended connection of unused pins are shown in Table 2-1.

For the I/O circuit configuration of each type, refer to Figure 2-1.

Table 2-1. Types of Pin I/O Circuits

Pin Name	I/O Circuit Type	I/O	Recommended Connection of Unused Pins
P00/INTP0 to P02/INTP2	8-A	I/O	Independently connect to V_{SS0} via a resistor.
P03/$\overline{SCK2}$			
P04/SO2			
P05/SI2			
P06, P07			
P10/ANI0 to P14/ANI4	9	Input	Independently connect to V_{DD0} or V_{SS0} via a resistor.
P20/SM11 to P23/SM14	4	Output	Leave open
P24/SM21 to P27/SM24			
P30/SM31 to P33/SM34			
P34/SM41 to P37/SM44			
P40/TI00 to P42/TI02	8	I/O	Independently connect to V_{DD0} or V_{SS0} via a resistor.
P43/TIO2			
P44/TIO3			
P50/$\overline{SCK3}$			
P51/SO3	5		
P52/SI3	8		
P53/RxD			
P54/TxD	5		
P60/PCL/TPO			
P61/SGO			
P81/S19 to P87/S13	17-G		
P90/S12 to P97/S5			
S0 to S4	17	Output	Leave open
COM0 to COM3	18		
V_{LCD}	–	–	
$\overline{RESET}$	2	Input	–
SMV_{DD}	–	–	Connect to V_{DD0}
SMV_{SS}			Connect to V_{SS0}
AV_{REF}			Connect to V_{DD0}
AV_{SS}			Connect to V_{SS0}
V_{PP}			Connect directly to V_{SS0} or V_{SS1}.

Figure 2-1. Pin I/O Circuits (1/2)

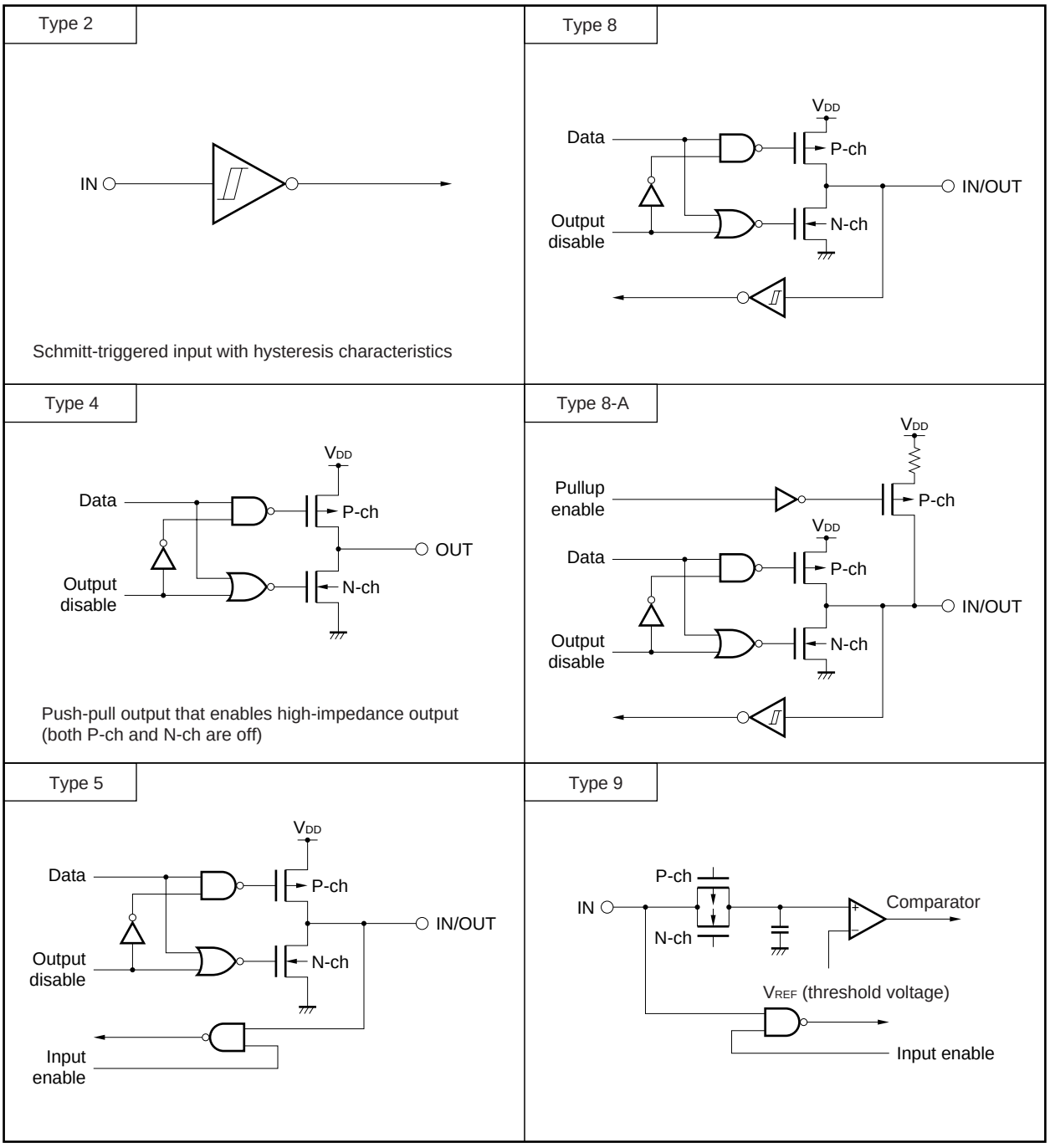
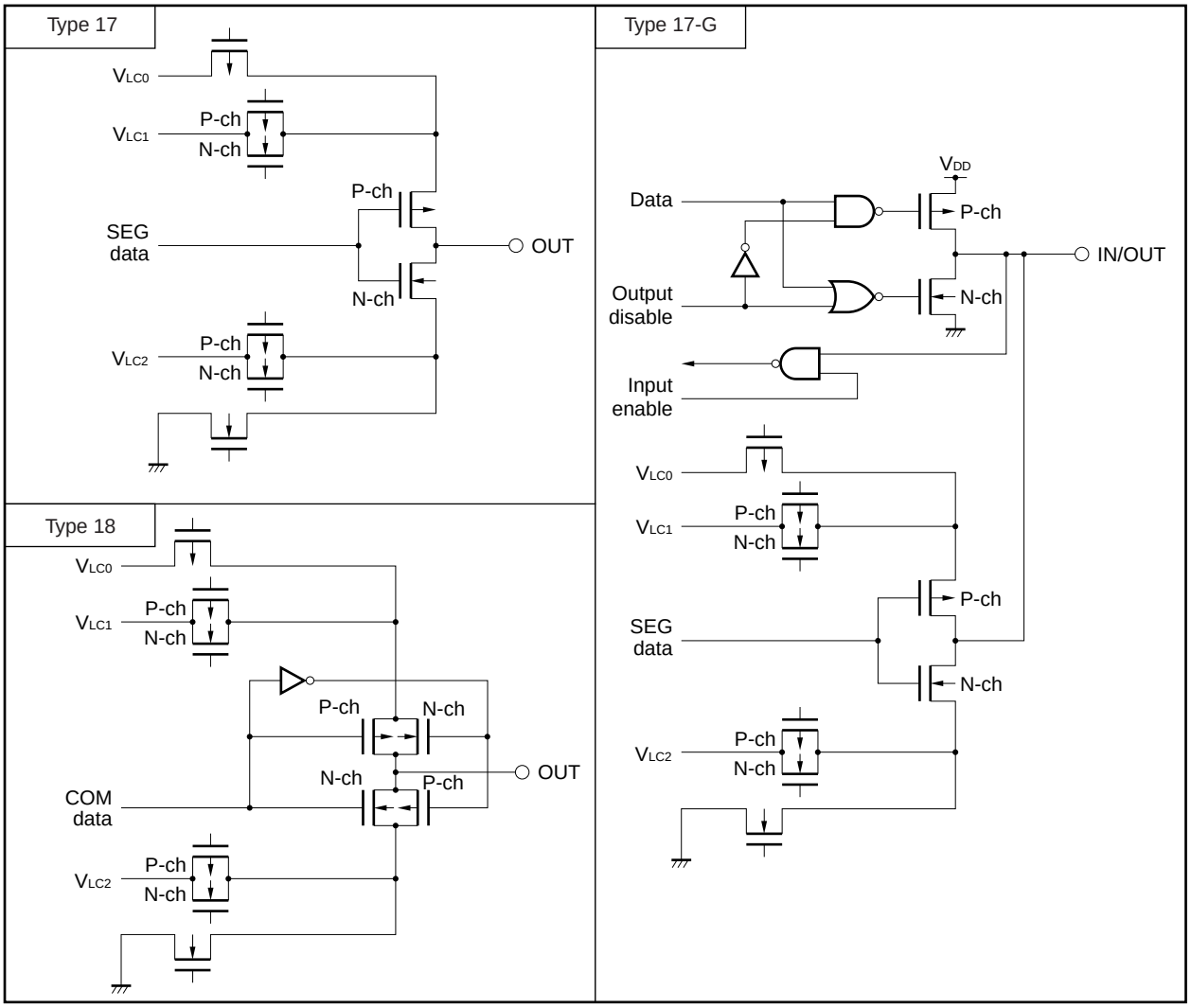


Figure 2-1. Pin I/O Circuits (2/2)



3. INTERNAL MEMORY SIZE SWITCHING REGISTER (IMS)

IMS is a register used to disable a part of the internal memory by means of software. By setting this register, the internal memory of the μPD78F0852 can be mapped identically to that of a mask ROM version with a different internal memory (ROM) capacity.

IMS is set with an 8-bit memory manipulation instruction.

$\overline{\text{RESET}}$ input sets IMS to CFH.

Figure 3-1. Format of Internal Memory Size Switching Register (IMS)

Address: FFF0H After reset: CFH R/W

Symbol	7	6	5	4	3	2	1	0
IMS	RAM2	RAM1	RAM0	0	ROM3	ROM2	ROM1	ROM0

RAM2	RAM1	RAM0	Internal high-speed RAM capacity selection
1	1	0	1024 bytes
Other than above			Setting prohibited

ROM3	ROM2	ROM1	ROM0	Internal ROM capacity selection
1	0	0	0	32 KB
1	0	1	0	40 KB
Other than above				Setting prohibited

Table 3-1 shows the IMS setting values to make the memory mapping the same as that of the mask ROM versions.

Table 3-1. Setting Values of Internal Memory Size Switching Register (IMS)

Target Mask ROM Version	IMS Setting Value
μPD780851(A)	C8H
μPD780852(A)	CAH

4. FLASH MEMORY PROGRAMMING

The flash memory can be written even while the device is mounted on the target system (on-board write). To write a program to the flash memory, connect the dedicated flash programmer (Flashpro III (model number: FL-PR3 and PG-FP3)) to both the host machine and target system.

A program can also be written by using an adapter for flash memory writing, connected to the Flashpro III.

Remark The FL-PR3 is manufactured by Naito Densei Machida Mfg. Co., Ltd.
Contact: +81-45-475-4191

4.1 Selecting Communication Mode

The Flashpro III writes to flash memory by means of serial communication. The communication mode to be used for writing is selected from those listed in Table 4-1. To select a communication mode, use the format shown in Figure 4-1, according to the number of V_{PP} pulses listed in Table 4-1.

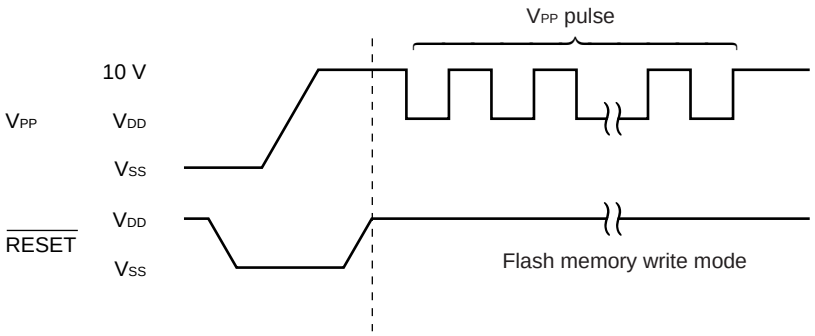
Table 4-1. Communication Mode

Communication Mode	Number of Channels	Pins Used[Note]	Number of V_{PP} Pulses
3-wire serial I/O	2	SI3/P52 SO3/P51 $\overline{SCK3}$/P50	0
		SI2/P05 SO2/P04 $\overline{SCK2}$/P03	1
UART	1	RxD/P53 TxD/P54	8

Note Shifting to the flash memory programming mode sets all pins not used for flash memory programming to the same state as immediately after reset. Therefore, all ports enter an output high-impedance state. If the external devices do not acknowledge an output high-impedance state, handling such as connecting to V_{DD} via a resister or connecting to V_{SS} via a resister is required.

Caution The communication mode must be selected by the number of V_{PP} pulses listed in Table 4-1.

Figure 4-1. Communication Mode Selection Format



4.2 Flash Memory Programming Function

Flash memory writing and other operations can be performed by transmitting/receiving commands and data according to the selected communication mode. Table 4-2 lists the major flash memory programming functions.

Table 4-2. Major Functions of Flash Memory Programming

Function	Description
Reset	Stops writing or detects communication synchronization.
Batch verify	Compares the entire contents of memory with the input data.
Batch erase	Erases the entire contents of memory.
Batch blank check	Checks that the entire contents of memory have been erased.
High-speed write	Writes to the flash memory according to the specified write start address and number of data bytes to be written.
Continuous write	Continues writing based on the information input by using the high-speed write function.
Status	Checks the current operating mode and whether the operation has ended.
Oscillation frequency setting	Inputs the frequency information of the resonator.
Erase time setting	Inputs the memory erase time.
Baud rate setting	Sets the communication rate in UART mode.
Silicon signature read	Outputs the device name, memory capacity, and device block information.

4.3 Connecting Flashpro III

The connection between the Flashpro III and μPD78F0852 varies according to the communication mode. Figures 4-2 to 4-4 show the connection for each communication mode.

Figure 4-2. Flashpro III Connection in 3-Wire Serial I/O Mode (SIO3)

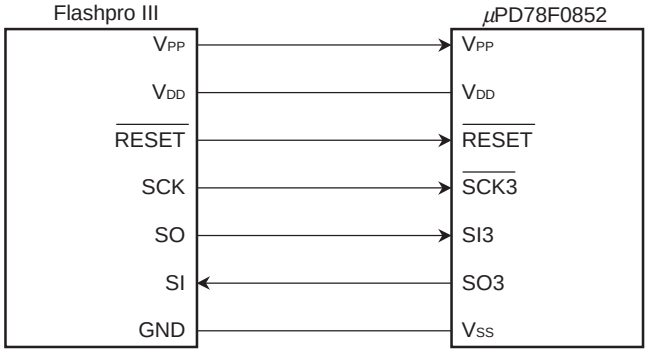


Figure 4-3. Flashpro III Connection in 3-Wire Serial I/O Mode (SIO2)

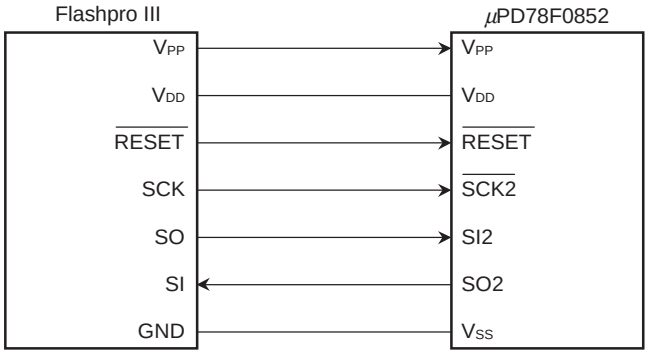
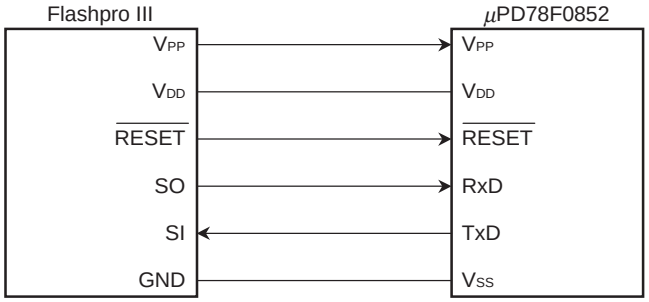


Figure 4-4. Flashpro III Connection in UART Mode



5. ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings (T_A = 25°C)

Parameter	Symbol	Conditions		Ratings	Unit
Supply voltage	V_{DD}			–0.3 to +6.5	V
	V_{PP}			–0.3 to +10.3	V
	AV_{REF}			–0.3 to V_{DD} + 0.3	V
	AV_{SS}			–0.3 to +0.3	V
	SMV_{DD}	$SMV_{DD} = V_{DD}$		–0.3 to +6.5	V
	SMV_{SS}			–0.3 to +0.3	V
Input voltage	V_I			–0.3 to V_{DD} + 0.3	V
Output voltage	V_{O1}	P00 to P07, P40 to P44, P50 to P54, P60, P61, P81 to P87, P90 to P97, $\overline{\text{RESET}}$		–0.3 to V_{DD} + 0.3	V
	V_{O2}	P20 to P27, P30 to P37		–0.5 to SMV_{DD} + 0.7	V
Analog input voltage	V_{AN}	P10 to P14	Analog input pin	AV_{SS} – 0.3 to AV_{REF} + 0.3	V
Output current, high	I_{OH}	Per pin (P00 to P07, P40 to P44, P50 to P54, P60, P81 to P87, P90 to P97)		–10	mA
		Total for P00 to P07, P40 to P44, P50 to P54, P60, P81 to P87, P90 to P97		–15	mA
		P61		–30	mA
		Per pin (P20 to P27)		–45	mA
		Total for P20 to P27		–135	mA
		Per pin (P30 to P37)		–45	mA
		Total for P30 to P37		–135	mA
Output current, low	I_{OL}	Per pin (P00 to P07, P40 to P44, P50 to P54, P60, P81 to P87, P90 to P97)		20	mA
		Total for P00 to P07, P40 to P44, P50 to P54, P60, P81 to P87, P90 to P97		50	mA
		P61		30	mA
		Per pin (P20 to P27)		45	mA
		Total for P20 to P27		135	mA
		Per pin (P30 to P37)		45	mA
		Total for P30 to P37		135	mA
Operating ambient temperature	T_A			–40 to +85	°C
Storage temperature	T_{stg}			–65 to +150	°C

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

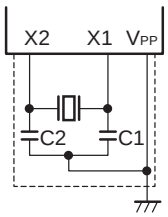
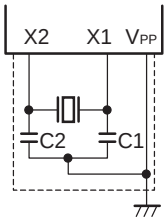
Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of port pins.

Capacitance (T_A = 25°C, V_{DD} = V_{SS} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Input capacitance	C_{IN}	f = 1 MHz				15	pF
I/O capacitance	C_{IO}	Unmeasured pins returned to 0 V.				15	pF
Output capacitance	C_{OUT}	f = 1 MHz Unmeasured pins returned to 0 V.	P00 to P07, P40 to P44, P50 to P54, P60, P81 to P87, P90 to P97			15	pF
	C_{SM}		P20 to P27, P30 to P37, P61			40	pF

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of port pins.

Main System Clock Oscillator Characteristics (T_A = –40 to +85°C, V_{DD} = 4.0 to 5.5 V)

Resonator	Recommended Circuit	Parameter	Conditions		MIN.	TYP.	MAX.	Unit
Ceramic resonator		Oscillation frequency (f_X)[Note 1]	V_{DD} = Oscillation voltage range	OSCM = 00H	4.0		8.38	MHz
				OSCM = 80H	4.0		4.19	MHz
		Oscillation stabilization time[Note 2]	After V_{DD} reaches oscillation voltage range MIN.				4	ms
Crystal resonator		Oscillation frequency (f_X)[Note 1]	V_{DD} = Oscillation voltage range	OSCM = 00H	4.0		8.38	MHz
				OSCM = 80H	4.0		4.19	MHz
		Oscillation stabilization time[Note 2]	After V_{DD} reaches oscillation voltage range MIN.				10	ms

Notes 1. Indicates only oscillator characteristics. Refer to **AC Characteristics** for instruction execution time.

2. Time required to stabilize oscillation after reset or STOP mode release.

Caution When using the main system clock oscillator, wire as follows in the area enclosed by the broken lines in the above figures to avoid an adverse effect from wiring capacitance.

- **Keep the wiring length as short as possible.**
- **Do not cross the wiring with the other signal lines.**
- **Do not route the wiring near a signal line through which a high fluctuating current flows.**
- **Always make the ground point of the oscillator capacitor the same potential as V_{SS}.**
- **Do not ground the capacitor to a ground pattern through which a high current flows.**
- **Do not fetch signals from the oscillator.**

★ **Recommended Oscillator Constant**

Main system clock: Ceramic resonator (–40 to +85°C)

8.38 MHz oscillation mode (OSCM = 00H)

Manufacturer	Part Number	Frequency (MHz)	Recommended Circuit Constant		Oscillation Voltage Range		Remarks
			C1 (pF)[Note]	C2 (pF)[Note]	MIN. (V)	MAX. (V)	
Murata Mfg. Co., Ltd	CSTLS4M00G56A-B0	4.0	47	47	4.0	5.5	On-chip capacitor
	CSTCR4M00G55A-R0	4.0	39	39			
	CSTLS4M19G56A-B0	4.194	47	47			
	CSTCR4M19G55A-R0	4.194	39	39			
	CSTLS5M00G53A-B0	5.0	15	15			
	CSTCR5M00G53A-R0	5.0	15	15			
	CSTLS8M00G53A-B0	8.0	15	15			
	CSTCC8M00G53A-R0	8.0	15	15			
	CSTLS8M38G53A-B0	8.388	15	15			
	CSTCC8M38G53A-R0	8.388	15	15			

Note Indicates the capacitance of the on-chip capacitor.

4.19 MHz oscillation mode (OSCM = 80H)

Manufacturer	Part Number	Frequency (MHz)	Recommended Circuit Constant		Oscillation Voltage Range		Remarks
			C1 (pF)[Note]	C2 (pF)[Note]	MIN. (V)	MAX. (V)	
Murata Mfg. Co., Ltd	CSTLS4M00G53A-B0	4.0	15	15	4.0	5.5	On-chip capacitor
	CSTCR4M00G53A-R0	4.0	15	15			
	CSTLS4M19G53A-B0	4.194	15	15			
	CSTCR4M19G53A-R0	4.194	15	15			

Note Indicates the capacitance of the on-chip capacitor.

DC Characteristics (T_A = –40 to +85°C, V_{DD} = 4.0 to 5.5 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Output current, high	I_{OH1}	P00 to P07, P40 to P44, P50 to P54, P60, P81 to P87, P90 to P97	Per pin			–5	mA
			Total			–10	mA
Output current, low	I_{OL1}	P00 to P07, P40 to P44, P50 to P54, P60, P81 to P87, P90 to P97	Per pin			10	mA
			Total			20	mA
Input voltage, high	V_{IH1}	P10 to P14, P51, P54, P60, P61, P81 to P87, P90 to P97		0.7V_{DD}		V_{DD}	V
	V_{IH2}	P00 to P07, P40 to P44, P50, P52, P53		0.7V_{DD}		V_{DD}	V
	V_{IH3}	$\overline{\text{RESET}}$		0.8V_{DD}		V_{DD}	V
Input voltage, low	V_{IL1}	P10 to P14, P51, P54, P60, P61, P81 to P87, P90 to P97		0		0.3V_{DD}	V
	V_{IL2}	P00 to P07, P40 to P44, P50, P52, P53		0		0.3V_{DD}	V
	V_{IL3}	$\overline{\text{RESET}}$		0		0.2V_{DD}	V
Output voltage, high	V_{OH1}	P00 to P07, P40 to P44, P50 to P54, P60, P81 to P87, P90 to P97	I_{OH} = –1 mA	V_{DD} – 1.0		V_{DD}	V
	V_{OH2}	P20 to P27, P30 to P37	I_{OH} = –27 mA (T_A = 85°C)	V_{DD} – 0.5		V_{DD} – 0.07	V
			I_{OH} = –30 mA (T_A = 25°C)	V_{DD} – 0.5		V_{DD} – 0.07	V
			I_{OH} = –40 mA (T_A = –40°C)	V_{DD} – 0.5		V_{DD} – 0.07	V
	V_{OH3}	P61	I_{OH} = –20 mA	V_{DD} – 0.5			V
Output voltage, low	V_{OL1}	P00 to P07, P40 to P44, P50 to P54, P60, P81 to P87, P90 to P97	I_{OL} = 1.6 mA			0.4	V
	V_{OL2}	P20 to P27, P30 to P37	I_{OL} = 27 mA (T_A = 85°C)	0.07		0.5	V
			I_{OL} = 30 mA (T_A = 25°C)	0.07		0.5	V
			I_{OL} = 40 mA (T_A = –40°C)	0.07		0.5	V
	V_{OL3}	P61	I_{OL} = 20 mA			0.5	V
Input leakage current, high	I_{LIH1}	P00 to P07, P10 to P14, P40 to P44, P50 to P54, P60, P61, P81 to P87, P90 to P97	V_{IN} = V_{DD}			3	μA
Input leakage current, low	I_{LIL1}	P00 to P07, P10 to P14, P40 to P44, P50 to P54, P60, P61, P81 to P87, P90 to P97	V_{IN} = 0 V			–3	μA
Output leakage current, high	I_{LOH}	V_{OUT} = V_{DD}				3	μA
Output leakage current, low	I_{LOL}	V_{OUT} = 0 V				–3	μA
Software pull-up resistor	R	V_{IN} = 0 V, P00 to P07		10	30	100	kΩ

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of port pins.

DC Characteristics (T_A = –40 to +85°C, V_{DD} = 4.0 to 5.5 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
★ Power supply current[Note 1]	I_{DD1}	8.38 MHz oscillation operating mode[Note 2]		9	27	mA
★		4.19 MHz oscillation operating mode[Note 2, 3]		5	15	mA
	I_{DD2}	8.38 MHz oscillation HALT mode		1.0	2.0	mA
		4.19 MHz oscillation HALT mode[Note 3]		0.7	1.4	mA
	I_{DD3}	STOP mode		1.0	30	μA

Notes 1. Refers to the current flowing to the CPU, peripheral functions (internal circuits), oscillator, and V_{DD} pin. The current flowing to the series resistor string of an A/D converter, on-chip pull-up resistors, LCD division resistor, sound generator (SGO/P61), and meter controller/driver (SM11/P20 to SM14/P23, SM21/P24 to SM24/P27, SM31/P30 to SM34/P33, SM41/P34 to SM44/P37) is not included.

2. High-speed mode operation (when the processor clock control register (PCC) is set to 00H)

3. Operation when the oscillator mode register (OSCM) is set to 80H

LCD Controller/Driver Characteristics (T_A = –40 to +85°C, V_{DD} = 4.0 to 5.5 V)

1/3 bias mode

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
LCD drive voltage	V_{LCD}			3.0		V_{DD}	V
LCD output voltage deviation[Note] (Common)	V_{ODC}	I_O = ±5 μA	3.0 V ≤ V_{LCD} ≤ V_{DD} V_{LCD0} = V_{LCD} V_{LCD1} = V_{LCD} × 2/3 V_{LCD2} = V_{LCD} × 1/3	0		±0.2	V
LCD output voltage deviation[Note] (Segment)	V_{ODS}	I_O = ±1 μA		0		±0.2	V
LCD division resistance current	I_{LCD}	3.0 V ≤ V_{LCD} ≤ V_{DD}		50		260	μA

Note The voltage deviation is the difference between the output voltage and the ideal value of segment and common outputs (V_{LCDn}: n = 0, 1, 2). Since pins to which a reference voltage (V_{LCD1} and V_{LCD2}) is applied do not exist in the μPD78F0852, the difference between the segment/common output voltage generated by the internal division resistance and the ideal reference potential (V_{DD} to 1/3V_{DD}) is regarded as the voltage deviation.

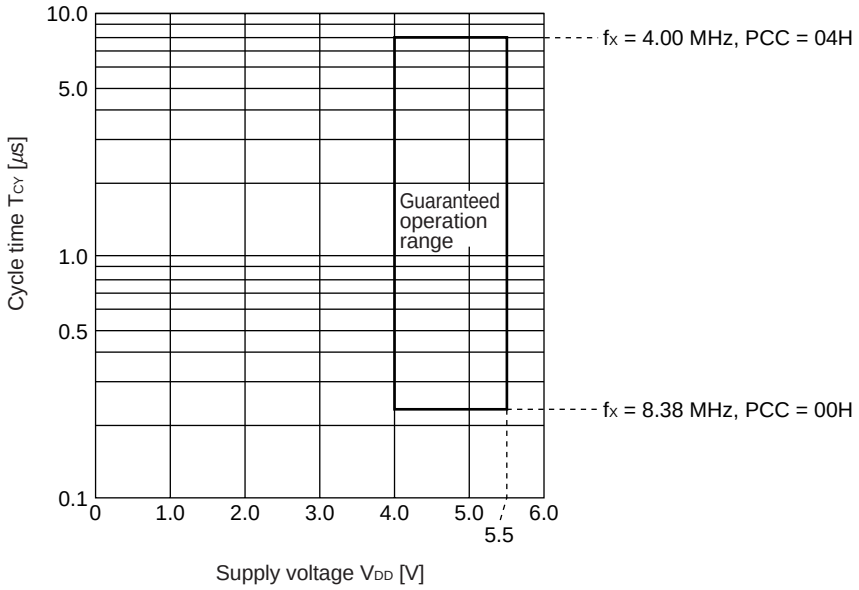
AC Characteristics

(1) Basic operation (T_A = –40 to +85°C, V_{DD} = 4.0 to 5.5 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Cycle time (minimum instruction execution time)	T_{CY}	Operating with main system clock	0.238		8	μs
TI00 to TI02 input high-/low-level width	t_{TIH2}, t_{TIL2}	At capture trigger TI00/P40 to TI02/P42	3/f_{SAM} Note			μs
TIO2, TIO3 input frequency	f_{TI5}	TIO2/P43, TIO3/P44	0		4	MHz
TIO2, TIO3 input high-/low-level width	t_{TIH5}, t_{TIL5}	TIO2/P43, TIO3/P44	100			ns
Interrupt request input high-/low-level width	t_{INTH}, t_{INTL}	INTP0 to INTP2	1			μs
$\overline{\text{RESET}}$ low-level width	t_{RSL}		10			μs

Note Selection of f_{SAM} = f_X/8, f_X/16, f_X/32, f_X/64 is possible with bits 0 and 1 (PRM00, PRM01) of the prescaler mode register (PRM0).

T_{CY} vs. V_{DD} (Main System Clock Operation)



(2) Serial interface (T_A = –40 to +85°C, V_{DD} = 4.0 to 5.5 V)

(a) UART mode (dedicated baud rate generator output)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Transfer rate					130.9	kbps

(b) 3-wire serial I/O mode (SIO3)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
$\overline{SCK3}$ cycle time	t_{KCY1}		800			ns
$\overline{SCK3}$ high-/low-level width	t_{KH1}, t_{KL1}	Internal clock selected	$t_{KCY1}/2 - 50$			ns
		External clock selected	400			ns
SI3 setup time (to $\overline{SCK3}\uparrow$)	t_{SIK1}		100			ns
SI3 hold time (from $\overline{SCK3}\uparrow$)	t_{KSI1}		400			ns
Delay time from $\overline{SCK3}\downarrow$ to SO3 output	t_{KSO1}	C = 100 pF[Note]			300	ns

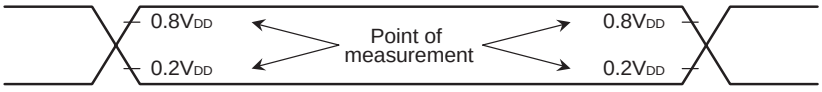
Note C is the load capacitance of the $\overline{SCK3}$ and SO3 output lines.

(c) 3-wire serial I/O mode (SIO2)

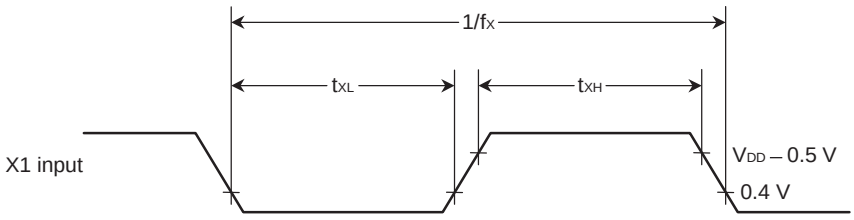
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
$\overline{SCK2}$ cycle time	t_{KCY2}		800			ns
$\overline{SCK2}$ high-/low-level width	t_{KH2}, t_{KL2}	Internal clock selected	$t_{KCY1}/2 - 50$			ns
		External clock selected	400			ns
SI2 setup time (to $\overline{SCK2}\uparrow$)	t_{SIK2}		100			ns
SI2 hold time (from $\overline{SCK2}\uparrow$)	t_{KSI2}		400			ns
Delay time from $\overline{SCK2}\downarrow$ to SO2 output	t_{KSO2}	C = 100 pF[Note]			300	ns

Note C is the load capacitance of the $\overline{SCK2}$ and SO2 output lines.

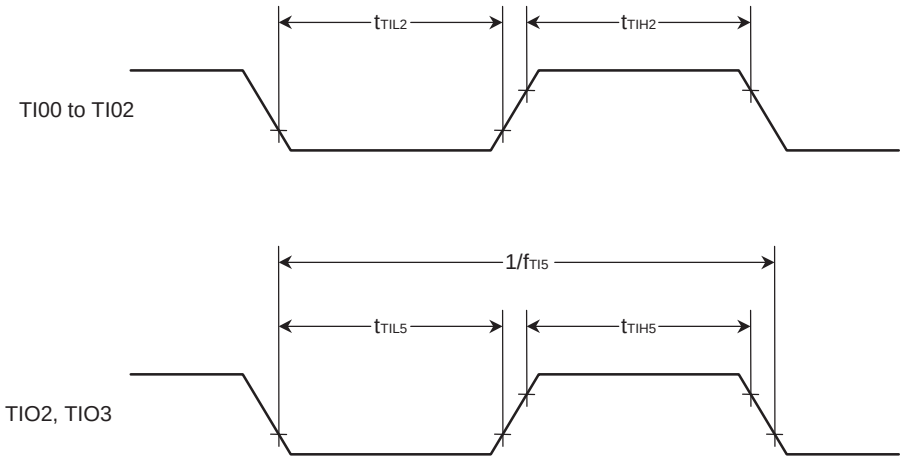
AC Timing Measurement Points (Excluding X1 Input)



Clock Timing

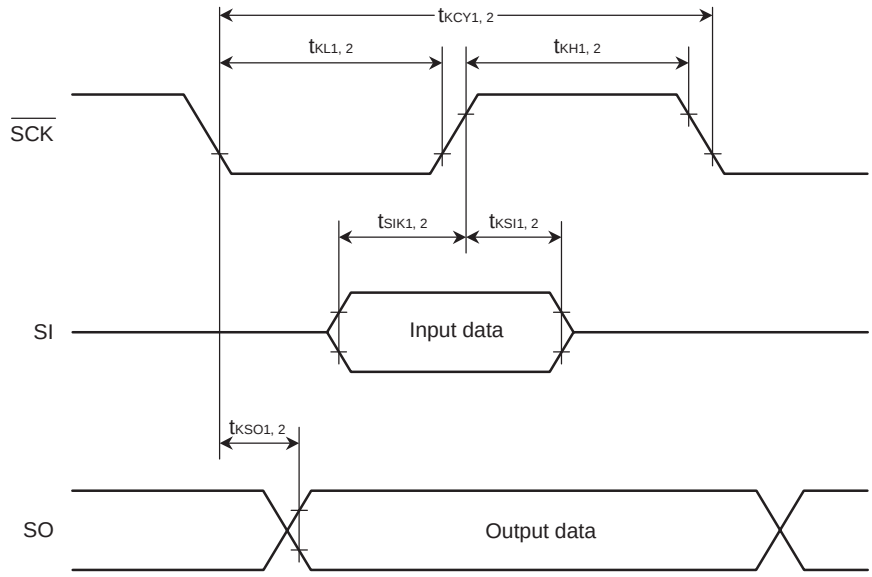


TI Timing



Serial Transfer Timing

3-wire serial I/O mode

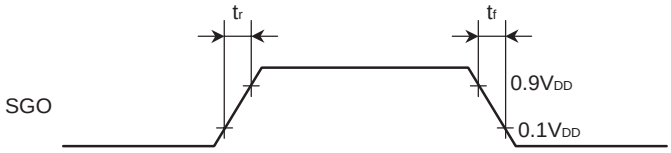


Sound Generator Characteristics (T_A = –40 to +85°C, V_{DD} = 4.0 to 5.5 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Sound generator input frequency	f_{SG1}				4.19	MHz
SGO output rise time	t_r	C = 100 pF[Note]	80		200	ns
SGO output fall time	t_f	C = 100 pF[Note]	80		200	ns

Note C is the load capacitance of the SGO output line.

Sound Generator Output Timing



Meter Controller/Driver Characteristics (T_A = –40 to +85°C, V_{DD} = 4.0 to 5.5 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Meter controller input frequency	f_{MC}[Note 1]				4.19	MHz
PWM output rise time	t_r	C = 100 pF[Note 2]	80		200	ns
PWM output fall time	t_f	C = 100 pF[Note 2]	80		200	ns
Symmetry performance[Note 3]	ΔHSPmn	I_{OH} = –30 mA ΔHSPmn = I V_{OH} (SMmn) max – V_{OH} (SMmn) min I			50	mV
	ΔLSPmn	I_{OH} = 30 mA ΔLSPmn = I V_{OL} (SMmn) max – V_{OL} (SMmn) min I			50	mV

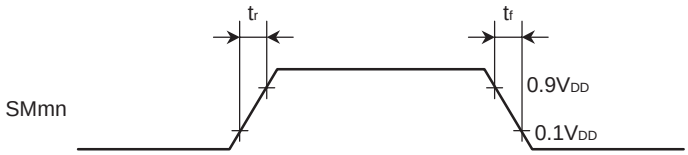
Notes 1. Source clock of the free-running counter.

2. C is the load capacitance of the PWM output line.

3. Indicates the dispersion of 16 PWM output voltages.

Remark m = 1 to 4, n = 1 to 4

Meter Controller/Driver Output Timing



Remark m = 1 to 4, n = 1 to 4

A/D Converter Characteristics (T_A = –40 to +85°C, AV_{REF} = V_{DD} = 4.0 to 5.5 V, AV_{SS} = V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Resolution					8	bit
Overall error[Note]					±0.6	%FSR
Conversion time	t_{CONV}		14.0			μs
Analog input voltage	V_{IAN}		AV_{SS}		AV_{REF} + 0.3	V
Reference voltage	AV_{REF}		4.0		V_{DD}	V
Resistance between AV_{REF} and AV_{SS}	I_{ADD}	A/D converter operating (ADCS1 = 1)		1.0	2.0	mA
		A/D converter not operating (ADCS1 = 0)		1.0	10	μA

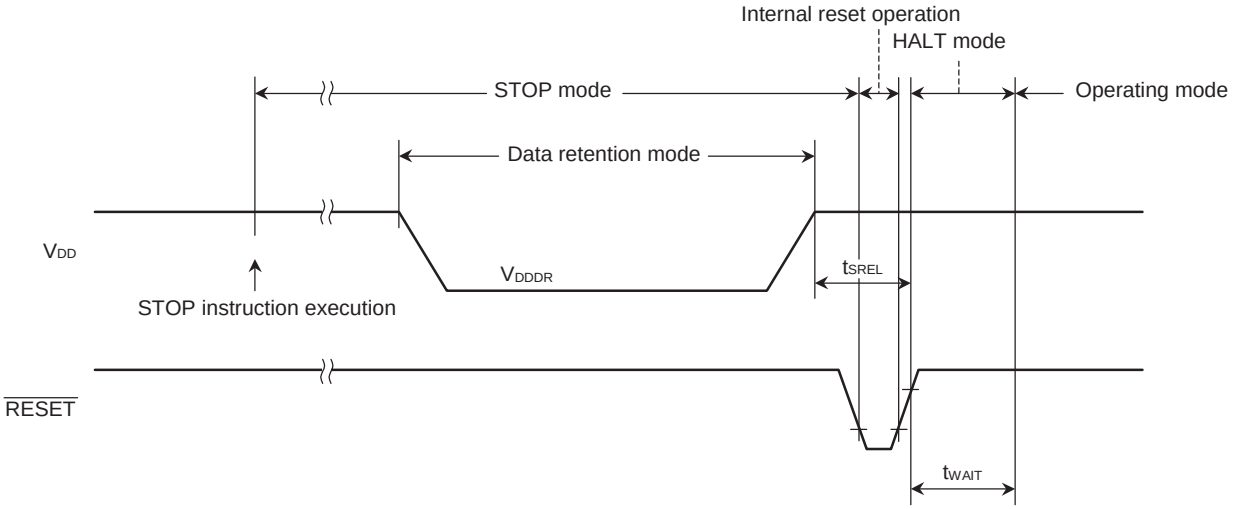
Note Excludes quantization error (±1/2 LSB). This value is indicated as a ratio to the full-scale value.

Data Memory STOP Mode Low Supply Voltage Data Retention Characteristics (T_A = –40 to +85°C)

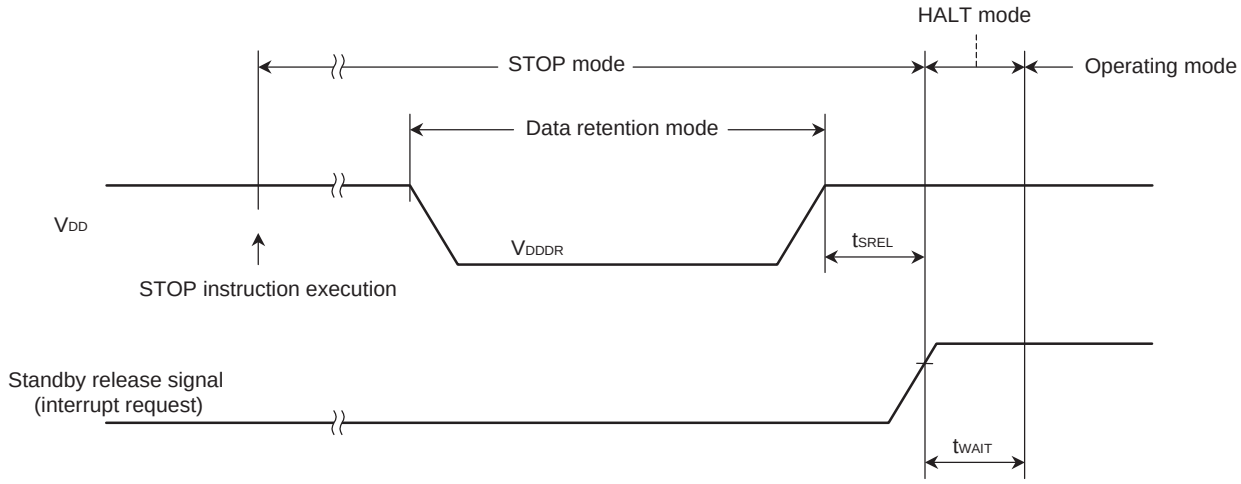
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Data retention supply voltage	V_{DDDR}		2.0		5.5	V
Data retention power supply current	I_{DDDR}	V_{DDDR} = 2.0 V		0.1	10	μA
Release signal set time	t_{SREL}		0			μs
Oscillation stabilization wait time	t_{WAIT}	Release by $\overline{\text{RESET}}$		$2^{17}/f_X$		s
		Release by interrupt request		**Note**		s

Note Selection of $2^{12}/f_X$ and $2^{14}/f_X$ to $2^{17}/f_X$ is possible with bits 0 to 2 (OSTS0 to OSTS2) of the oscillation stabilization time select register (OSTS).

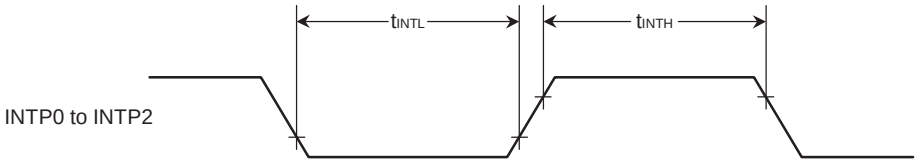
Data Retention Timing (STOP Mode Release by $\overline{\text{RESET}}$)



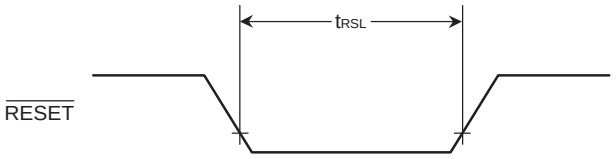
Data Retention Timing (Standby Release Signal: STOP Mode Release by Interrupt Request Signal)



Interrupt Request Input Timing



$\overline{\text{RESET}}$ Input Timing



Flash Memory Programming Characteristics

(1) Basic characteristics

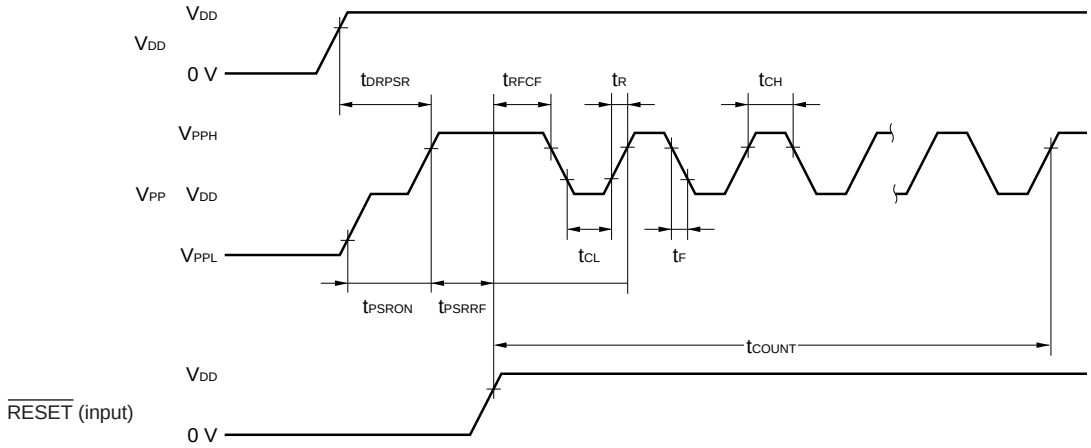
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Operating frequency	f_X	Main system clock operation	4.0		8.38	MHz
Supply voltage	V_{DD}		4.0		5.5	V
	V_{PPL}	V_{PP} low-level detection	0		$0.2V_{DD}$	V
	V_{PP}	V_{PP} high-level detection	$0.8V_{DD}$	V_{DD}	$1.2V_{DD}$	V
★	V_{PPH}	V_{PP} high-voltage detection	9.8	10.0	10.3	V
V_{DD} power supply current	I_{DD}				50	mA
V_{PP} power supply current	I_{PP}	V_{PP} = 10.0 V			50	mA
Write time (per byte)	t_{WRT}		40	50	120	μs
Number of rewrites	C_{WRT}	T_{PRG} = +10 to +40°C			20	Times
Erase time	t_{ERASE}			2		s
Programming temperature	T_{PRG}		+10		+40	°C

Remark For the input/output voltage and input/output leakage current, refer to **DC Characteristics**.

(2) Serial write operation characteristics

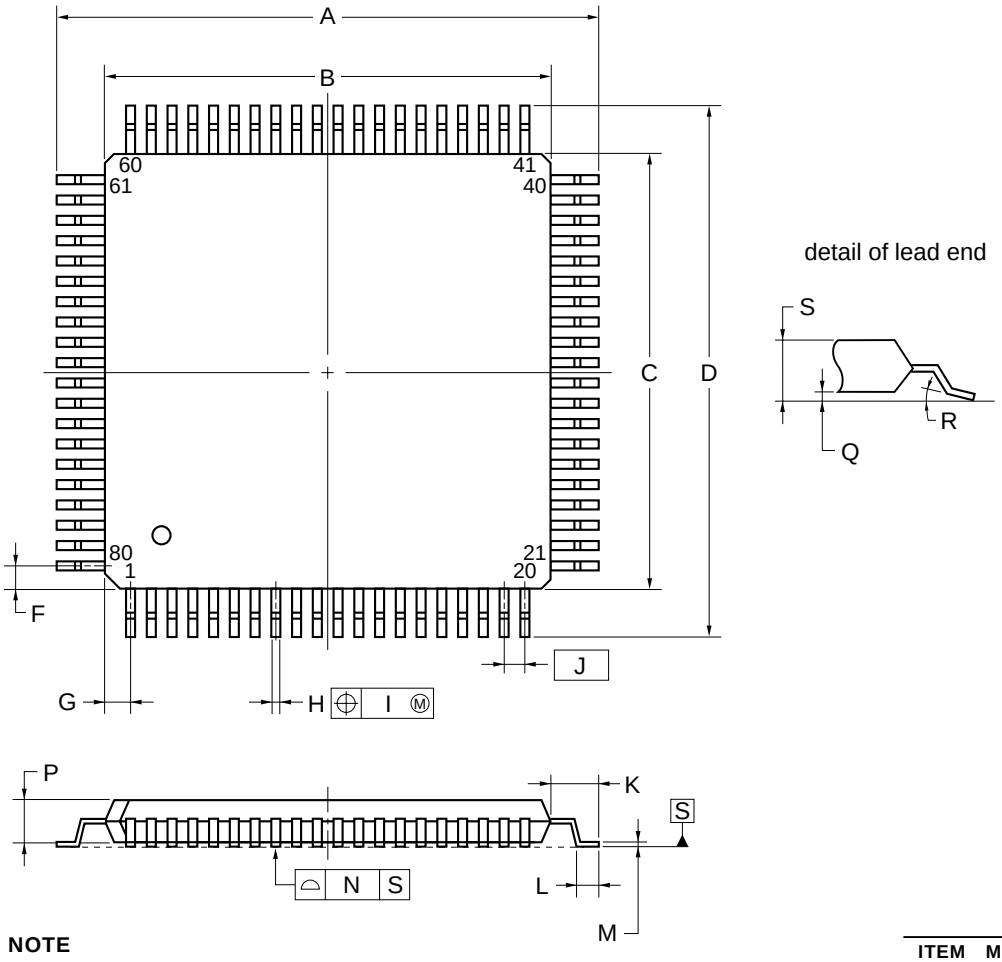
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
V_{PP} setup time	t_{PSRON}	V_{PP} high voltage	1.0			μs
Setup time from V_{DD}↑ to V_{PP}↑	t_{DRPSR}	V_{PP} high voltage	1.0			μs
Setup time from V_{PP}↑ to $\overline{RESET}$↑	t_{PSRRF}	V_{PP} high voltage	1.0			μs
Count start time from $\overline{RESET}$↑ to V_{PP}↑	t_{RFCF}		1.0			μs
Count execution time	t_{COUNT}				2.0	ms
V_{PP} counter high-/low-level width	t_{CH}, t_{CL}		8.0			μs
V_{PP} counter rise/fall time	t_R, t_F		1.0			μs

Flash Write Mode Setting Timing



6. PACKAGE DRAWING

80-PIN PLASTIC QFP (14x14)



NOTE

Each lead centerline is located within 0.13 mm of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS
A	17.20±0.20
B	14.00±0.20
C	14.00±0.20
D	17.20±0.20
F	0.825
G	0.825
H	0.32±0.06
I	0.13
J	0.65 (T.P.)
K	1.60±0.20
L	0.80±0.20
M	$0.17^{+0.03}_{-0.07}$
N	0.10
P	1.40±0.10
Q	0.125±0.075
R	$3^{\circ}{}^{+7^{\circ}}_{-3^{\circ}}$
S	1.70 MAX.

P80GC-65-8BT-1

★ 7. RECOMMENDED SOLDERING CONDITIONS

The μPD78F0852 should be soldered and mounted under the following recommended conditions.

For details of the recommended soldering conditions, refer to the document **Semiconductor Device Mounting Technology Manual (C10535E)**.

For soldering methods and conditions other than those recommended below, contact your NEC sales representative.

Table 7-1. Surface Mounting Type Soldering Conditions

μPD78F0852GC-8BT: 80-pin plastic QFP (14 × 14)

Soldering Method	Soldering Conditions	Recommended Condition Symbol
Interface reflow	Package peak temperature: 235°C, Time: 30 seconds max. (at 210°C or higher), Count: Two times or less, Exposure limit: 7 days[Note] (after that, prebake at 125°C for 10 hours)	IR35-107-2
VPS	Package peak temperature: 215°C, Time: 40 seconds max. (at 200°C or higher), Count: Two times or less, Exposure limit: 7 days[Note] (after that, prebake at 125°C for 10 hours)	VP15-107-2
Wave soldering	Solder bath temperature: 260°C max., Time: 10 sec. max., Count: once, Preheating temperature: 120°C max.(package surface temperature), Exposure limit: 7 daysNote (after that, prebake at 125°C for 10 hours)	WS60-107-1
Partial heating	Pin temperature: 300°C max., Time: 3 seconds max. (per pin row)	–

Note After opening the dry peak, store it at 25°C or less and 65% RH or less for the allowable storage period.

Caution Do not use different soldering methods together (except for partial heating).

APPENDIX A. DEVELOPMENT TOOLS

The following development tools are available for system development using the μPD78F0852. Also refer to **(6) Cautions on Using Development Tools**.

(1) Software Package

SP78K0	Software Package common to 78K/0 Series

(2) Language Processing Software

RA78K0	Assembler package common to 78K/0 Series
CC78K0	C compiler package common to 78K/0 Series
DF780852	Device file for μPD780852 Subseries
CC78K0-L	C compiler library source file common to 78K/0 Series

(3) Flash Memory Writing Tools

Flashpro III (Part No. FL-PR3, PG-FP3)	Dedicated flash programmer for microcomputers incorporating flash memory

(4) Debugging Tools

IE-78K0-NS(-A)	In-circuit emulator common to 78K/0 Series
IE-70000-MC-PS-B	Power supply unit for IE-78K0-NS
IE-78K0-NS-PA	Performance board to enhance/expand functions of IE-78K0-NS
IE-780852-NS-EM4, IE-78K0-NS-P04	Probe board and I/O board used to emulate μPD780852 Subseries products
IE-70000-98-IF-C	Interface adapter necessary when using PC-9800 series PC (except notebook type) as host machine (C bus supported)
IE-70000-CD-IF-A	PC card and interface cable necessary when using notebook PC as host machine (PCMCIA socket supported)
IE-70000-PC-IF-C	Interface adapter necessary when using IBM PC/AT™ compatible as host machine (ISA bus supported)
IE-70000-PCI-IF-A	Adapter necessary when using personal computer incorporating PCI bus as host machine
NP-80GC-TQ	Emulation probe for 80-pin plastic QFP (GC-8BT type)
SM78K0	System simulator common to 78K/0 Series
ID78K0-NS	Integrated debugger for IE-78K0-NS
DF780852	Device file for μPD780852 Subseries

(5) Real-time OS

RX78K0	Real-time OS for 78K/0 Series
MX78K0	OS for 78K/0 Series

(6) Cautions on Using Development Tools

- The ID78K0-NS and SM78K0 are used in combination with the DF780852.
- The CC78K0 and RX78K0 are used in combination with the RA78K0 and DF780852.
- The FL-PR3 and NP-80GC-TQ are products made by Naitou Densei Machidaseisakusho Co., Ltd. (TEL +81-45-475-4191).
- For third party development tools, see the **Single-Chip Microcontroller Development Tool Selection Guide (U11069E).**
- The host machine and OS suitable for each software are as follows:

Software \ Host Machine [OS]	PC PC-9800 series [Japanese Windows™] IBM PC/AT and compatibles [Japanese/English Windows]	EWS HP9000 series 700™ [HP-UX™] SPARCstation™ [SunOS™, Solaris™]
RA78K0	√Note	√
CC78K0	√Note	√
ID78K0-NS	√	–
SM78K0	√	–
RX78K0	√Note	√
MX78K0	√Note	√

Note DOS-based software

APPENDIX B. RELATED DOCUMENTS

The related documents indicated in this publication may include preliminary versions. However, preliminary versions are not marked as such.

- Documents Related to Devices

Document Name	Document No.
μPD780852 Subseries User's Manual	U14581E
μPD780851(A), 780852(A) Data Sheet	U14577E
μPD78F0852 Data Sheet	This document
78K/0 Series User's Manual Instructions	U12326E

- Documents Related to Development Tools (User's Manuals)

Document Name		Document No.
RA78K0 Assembler Package	Operation	U11802E
	Language	U11801E
	Structured Assembly Language	U11789E
CC78K0 C Compiler	Operation	U11517E
	Language	U11518E
PG-FP3 Flash Memory Programmer		U13502E
IE-78K0-NS In-Circuit Emulator		U13731E
IE-78K0-NS-A In-Circuit Emulator		U14889E
IE-780701-NS-EM1		To be prepared
SM78K0S, SM78K0 System Simulator Ver. 2.10 or Later Windows Based	Operation	U14611E
SM78K Series System Simulator Ver. 2.10 or Later	External Part User Open Interface Specifications	U15006E
ID78K0-NS Integrated Debugger Ver. 2.00 or Later Windows Based	Operation	U14379E
ID78K0-NS, ID78K0S-NS Integrated Debugger Ver. 2.20 or Later Windows Based	Operation	U14910E
ID78K0 Integrated Debugger Windows Based	Guide	U11649E
	Reference	U11539E

- Documents Related to Embedded Software (User's Manuals)

Document Name		Document No.
78K/0 Series Real-Time OS	Fundamental	U11537E
	Installation	U11536E
78K/0 Series OS MX78K0	Fundamental	U12257E

- Other Related Documents

Document Name	Document No.
SEMICONDUCTOR SELECTION GUIDE Products & Packages (CD-ROM)	X13769E
Semiconductor Device Mounting Technology Manual	C10535E
Quality Grades on NEC Semiconductor Devices	C11531E
NEC Semiconductor Device Reliability/Quality Control System	C10983E
Guide to Prevent Damage for Semiconductor Devices by Electrostatic Discharge (ESD)	C11892E

Caution The related documents listed above are subject to change without notice. Be sure to use the latest version of each document for designing.

[MEMO]

NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note:

Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note:

No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note:

Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

Regional Information

Some information contained in this document may vary from country to country. Before using any NEC product in your application, please contact the NEC office in your country to obtain a list of authorized representatives and distributors. They will verify:

- Device availability
- Ordering information
- Product release schedule
- Availability of related technical literature
- Development environment specifications (for example, specifications for third-party tools and components, host computers, power plugs, AC supply voltages, and so forth)
- Network requirements

In addition, trademarks, registered trademarks, export restrictions, and other legal issues may also vary from country to country.

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