

MOS INTEGRATED CIRCUIT μ PD16676

1/16, 1/32 DUTY LCD CONTROLLER/DRIVER WITH RAM

DESCRIPTION

 μ PD16676 is a controller/driver containing RAMs capable of full-dot LCD displays. One of these IC chips can drive the full-dot LCD up to 61-by-16 dots.

These ICs are the most suitable for Kanji character or Chinese character pagers, as well as graphic pagers, displaying 16-by-16 dots per character.

FEATURES

- LCD driver with built-in display RAM
- Dot display RAM: 2560 bits
- Output: 61 segments & 16 commons
- 8-bit parallel interface
- · Oscillation circuit incorporated

★ ORDERING INFORMATION

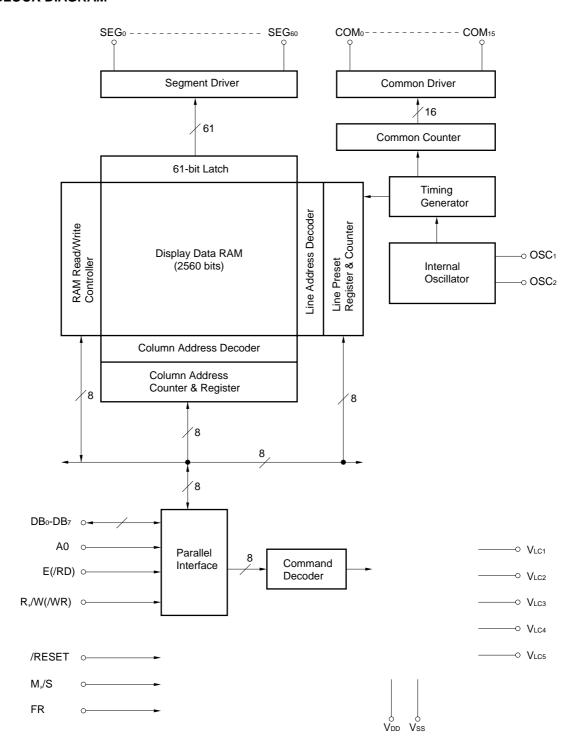
Part Number	Package
μ PD16676P	Chips
μ PD16676W	Wafer

Remark Purchasing the above products in terms of chips per wafer requires an exchange of other documents as well, including a memorandum of the product quality. Therefore, those who are interested in this regard are advised to contact one of our sales representatives for further details.

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Not all devices/types available in every country. Please check with local NEC representative for availability and additional information.

★ 1. BLOCK DIAGRAM



Remark /xxx indicates active low signals.

***** 2. PIN CONFIGURATION (PAD LAYOUT)

Chip Size : $4.04 \times 5.53 \text{ mm}^2$ Pad Size Al Area : $120 \times 120 \mu\text{m}^2$ Pad Size Open Area : $108 \times 108 \mu\text{m}^2$

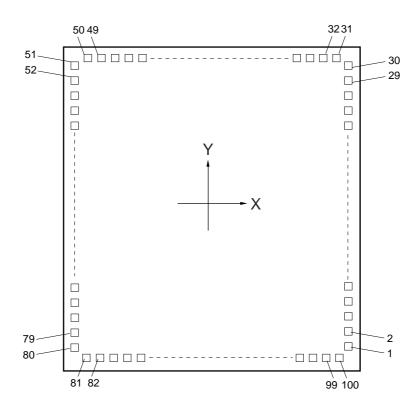


Table2-1. Pad Connection

Pin No.	Pin Symbol	I/O
1	COM₅	Output
2	COM ₆	Output
3	COM ₇	Output
4	COM ₈	Output
5	COM ₉	Output
6	COM ₁₀	Output
7	COM ₁₁	Output
8	COM ₁₂	Output
9	COM ₁₃	Output
10	COM ₁₄	Output
11	COM ₁₅	Output
12	SEG ₆₀	Output
13	SEG ₅₉	Output
14	SEG ₅₈	Output
15	SEG ₅₇	Output
16	SEG ₅₆	Output
17	SEG55	Output
18	SEG ₅₄	Output
19	SEG ₅₃	Output
20	SEG ₅₂	Output
21	SEG ₅₁	Output
22	SEG ₅₀	Output
23	SEG ₄₉	Output
24	SEG ₄₈	Output
25	SEG ₄₇	Output
26	SEG ₄₆	Output
27	SEG ₄₅	Output
28	SEG ₄₄	Output
29	SEG ₄₃	Output
30	SEG ₄₂	Output
31	SEG ₄₁	Output
32	SEG ₄₀	Output
33	SEG ₃₉	Output
34	SEG ₃₈	Output
35	SEG ₃₇	Output
36	SEG ₃₆	Output
37	SEG ₃₅	Output
38	SEG ₃₄	Output
39	SEG33	Output
40	SEG ₃₂	Output
41	SEG ₃₁	Output
42	SEG ₃₀	Output
43	SEG ₂₉	Output
44	SEG ₂₈	Output
45	SEG ₂₇	Output
46	SEG ₂₇	Output
47	SEG ₂₅	Output
48	SEG ₂₅	Output
49	SEG ₂₄	Output
50	SEG ₂₃	·
JU	SEG22	Output

Pin No.	Pin Symbol	I/O
51	SEG ₂₁	Output
52	SEG ₂₀	Output
53	SEG ₁₉	Output
54	SEG ₁₈	Output
55	SEG ₁₇	Output
56	SEG ₁₆	Output
57	SEG ₁₅	Output
58	SEG ₁₄	Output
59	SEG ₁₃	Output
60	SEG ₁₂	Output
61	SEG ₁₁	Output
62	SEG ₁₀	Output
63	SEG ₉	Output
64	SEG ₈	Output
65	SEG ₇	Output
66	SEG ₆	Output
67	SEG₅	Output
68	SEG ₄	Output
69	SEG₃	Output
70	SEG ₂	Output
71	SEG ₁	Output
72	SEG₀	Output
73	A0	Input
74	OSC ₁	Input
75	OSC ₂	Output
76	E(/RD)	Input
77	R,/W(/WR)	Input
78	Vss	_
79	DB ₀	Input/Output
80	DB ₁	Input/Output
81	DB ₂	Input/Output
82	DB₃	Input/Output
83	DB ₄	Input/Output
84	DB₅	Input/Output
85	DB ₆	Input/Output
86	DB ₇	Input/Output
87	V_{DD}	_
88	/RESET	Input
89	FR	Input/Output
90	V _{LC5}	_
91	V _{LC3}	_
92	V _{LC2}	_
93	M,/S	Input
94	V _{LC4}	_
95	V _{LC1}	_
96	COMo	Output
97	COM ₁	Output
98	COM ₂	Output
99	СОМз	Output
100	COM ₄	Output

Table2-2. Pad Layout

Pin No.	Χ (μm)	Υ (μm)	Pin No.	Χ (μm)	Υ (μm)	Pin No.	X (μm)	Υ (μm)
1	1771	-2230	36	668.8	2517.2	71	-1771	-757.2
2	1771	-2076	37	518.8	2517.2	72	-1771	-907.2
3	1771	-1922	38	368.8	2517.2	73	-1767.8	-1149.4
4	1771	-1768	39	218.8	2517.2	74	-1767.8	-1299.4
5	1771	-1614	40	68.8	2517.2	75	-1767.8	-1489.4
6	1771	-1460	41	-81.2	2517.2	76	-1767.8	-1639.4
7	1771	-1306	42	-231.2	2517.2	77	-1767.8	-1839.4
8	1771	-1152	43	-381.2	2517.2	78	-1767.8	-1989.4
9	1771	-998	44	-531.2	2517.2	79	-1767.8	-2139.4
10	1771	-844	45	-681.2	2517.2	80	-1767.8	-2289.4
11	1771	-690	46	-831.2	2517.2	81	-1745	-2513.4
12	1771	-536	47	-981.2	2517.2	82	-1595	-2513.4
13	1771	-382	48	-1131.2	2517.2	83	-1395	-2513.4
14	1771	-228	49	-1281.2	2517.2	84	-1245	-2513.4
15	1771	-74	50	-1431.2	2517.2	85	-1045	-2513.4
16	1771	80	51	-1771	2242.8	86	-895	-2513.4
17	1771	234	52	-1771	2092.8	87	-682.6	-2513.4
18	1771	388	53	-1771	1942.8	88	-532.2	-2513.4
19	1771	542	54	-1771	1792.8	89	-382.2	-2513.4
20	1771	696	55	-1771	1642.8	90	-106.6	-2513.4
21	1771	850	56	-1771	1492.8	91	69.8	-2513.4
22	1771	1004	57	-1771	1342.8	92	219.8	-2513.4
23	1771	1158	58	-1771	1192.8	93	369.8	-2513.4
24	1771	1312	59	-1771	1042.8	94	569.8	-2513.4
25	1771	1466	60	-1771	892.8	95	719.8	-2513.4
26	1771	1620	61	-1771	742.8	96	952.4	-2513.4
27	1771	1774	62	_1771	592.8	97	1102.4	-2513.4
28	1771	1928	63	-1771	442.8	98	1252.4	-2513.4
29	1771	2082	64	-1771	292.8	99	1402.4	-2513.4
30	1771	2236	65	-1771	142.8	100	1552.4	-2513.4
31	1418.8	2517.2	66	-1771	-7.2			
32	1268.8	2517.2	67	-1771	-157.2			
33	1118.8	2517.2	68	-1771	-307.2			
34	968.8	2517.2	69	-1771	-457.2			
35	818.8	2517.2	70	-1771	-607.2			



5. PIN FUNCTIONS

5.1 Power System

Pin Symbol	Pin Name	Pin No.	I/O	Description
V _{DD}	Power supply pin	87		Power supply
Vss	Ground	78	_	Ground
VLC1 to VLC5	Reference power supply	90,91,92,94,	_	Reference power supply for LCD driving
	for drivers	95		

5.2 Logic system

Pin Symbol	Pin Name	Pin No.	I/O	Description
M,/S	Master/Slave selection	93	Input	Switches between the master chip and the slave chip.
FR	LCD to AC signal	89	Input/ Output	Exchanges synchronizing signals (LCD-to-AC signals) in connecting cascades. This pin is for output if the chip is the master, and for input if the chip is the slave.
DB ₀ to DB ₇	Data Bus	79 to 86	Input/ Output	Data inputs/outputs
A0	Data/Instruction Switching	73	Input	This pin is used for switching between the display data and the instruction. High level: Display data Low level: Instruction
/RESET	Reset and 68/80-series switching	88	Input	This pin performs reset at the edge of the low-level pulse. At that level, it performs switching 68/80 series modes. High level: 68 series CPU interface Low level: 80 series CPU interface
E(/RD)	Enable and read enable	76	Input	68 series mode : Enable signal 80 series mode : Read enable signal
R,/W(/WR)	Read/Write and Write enable	77	Input	68 series mode : Read/Write signal 80 series mode : Write enable signal
OSC ₁	Oscillation pin	74	Input	Oscillation (connected with a register between OSC ₂)
OSC ₂	Oscillation pin	75	Output	Oscillation (connected with a register between OSC ₁)

5.3 Driver System

Pin Symbol	Pin Name	Pin No.	I/O	Description
SEG₀ to	Segment	72 to 12	Output	Segment output pins
SEG ₆₀				
COM ₀ to	Common	96 to 100,	Output	Common output pins
COM ₁₅		1 to 11		If the chip is a slave, these pins correspond to COM ₁₆
				to COM ₃₁ .

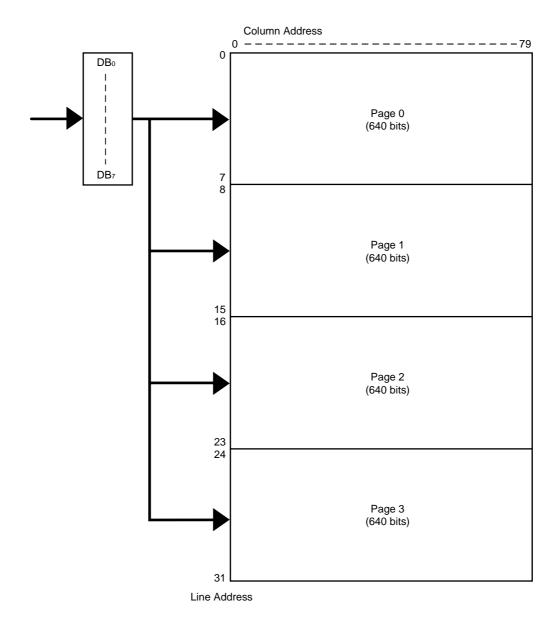


4. COMMANDS

	Command	/RD	/WR	A0	DB ₇	DB ₆	DB ₅	DB ₄	DВз	DB ₂	DB ₁	DB ₀	Function				
1	Display ON/OFF	1	0	0	1	0	1	0	1	1	1	0/1	ON/OFF of the whole display is performed independent of the display RAM's data or internal state. 1: ON, 0: OFF (Power save at static drive ON)				
2	Display start line	1	0	0	1	1	0	[start a	addres I)	S	Determines the RAM line displayed on the uppermost line (COM ₀) of the display.				
3	Page address set	1	0	0	1	0	1	1	1	0		ges o 3)	Sets display RAM pages in the page address register.				
4	Column(segment) address set	1	0	0	0				n add 0 to 79				Sets display RAM's column address in the column address register.				
5	Status read	0	1	0	B U S Y	A D C	O N / O F F	R E S E T	0	0	0	0	Reads status BUSY 1: During internal operation 0: READY status ADC 1: Clockwise output(Normal rotation) 0: Counterclockwise output (Reverse) ON/OFF 1: Display OFF, 0: Display ON RESET				
6	Display data write	1	0	1				Write	Data		l		1: Being reset, 0: Normal Displays the data bus data and writes it onto the display RAM. Accesses the display RAM of a pre-specified address. After				
7	Display data read	0	1	1				Read	l data				Reads the data in the display RAM address is onto the data bus. incremented.				
8	ADC select	1	0	0	1	0	1	0	0	0	0	0/1	This command is used to reverse the correspondence relationship between display RAM's column addresses and segment driver outputs. 0: Clockwise output (Normal rotation) 1: Counterclockwise output (Reverse)				
9	Static drive ON/OFF	1	0	0	1	0	1	0	0	1	0	0/1	Selects between the normal display operation and the static all-lamp-driven display. 1: Static drive (Power save) 0: Normal display operation				
10	Duty select	1	0	0	1	0	1	0	1	0	0	0/1	Selects between two different liquid- crystal cell driving duties. 1: 1/32 duty 0: 1/16 duty				
11	Read modify write	1	0	0	1	1	1	0	0	0	0	0	Increments the column address counte only when writing the display data; but not when reading it.				
12	END	1	0	0	1	1	1	0	1	1	1	0	Cancels read modify write mode				
13	Reset	1	0	0	1	1	1	0	0	0	1	0	Sets the display start line register to the first line. Sets the column address counter and the page address register to 0.				

Note If the static drive is turned ON in the display OFF state, the machine is placed in the power save state.

5. DISPLAY RAM MAP





6. Line Address Circuit

As is shown in Figure 6–1, the line address circuit specifies the line address that corresponds to a COM output for displaying the contents of display data RAM. The display start line address set command specifies line address of to the COM₀ output.

The screen can be scrolled by dynamically changing the line address via the display start line address set command.

COM Output COMo DB₀ COM₁ 01H 02H COM₃ DB₃ 03H Page0 0 0 DB₄ DB₅ 04H COM₅ DB₆ 06H COM COM₉ DB₀ 08H DB₁ 09H COM₁₀ COM₁₁ DB₃ 0 0BH Page1 0CH COM₁₂ COM₁₃ DB₅ 0DH COM₁₄ DB₆ 0EH COM₁₅ COM₁₆ COM₁₇ 0FH 10H DB DB₂ 12H COM₁₈ Page2 13H COM₁₉ 0 DB₄ 14H COM₂₀ COM₂₁ DB₅ 15H DB₆ 16H COM₂ 17H 18H DB₁ 19H COM₂ DB₂ COM₂₆ 1AH DB₃ Page3 1BH COM₂ DB₄ COM₂₈ 1CH DB₅ 1DH COM₃₀ DB₆ 1FH 49H 06H SEG53 1AH 35H DB₀DB₀ EG56 17H 38H SEG54 19H 48H 18H 16H 15H 14H LCD žEG₆ SEG7

Figure 6-1. Specification of Display Start Line Address in Display Data RAM

Remark COM₁₆ to COM₃₁ are valid in only 1/32 duty.



7. ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings (T_A = 25°C, Vss = 0 V)

<u> </u>		,	
Parameter	Symbol	Rating	Unit
Supply voltage	V _{DD}	-0.3 to +6.5	V
Driver reference supply input voltage	VLC1 to VLC4	C4 VDD - 13 to VDD + 0.3	
	V _{LC5}	V _{DD} – 13 to +0.3	V
Logic system input voltage	rige V _{IN1} -0.3 to V _{DD} + 0.3		V
Logic system output voltage	Vout1	−0.3 to V _{DD} + 0.3	V
Logic system input/output voltage	V _{I/O1}	−0.3 to V _{DD} + 0.3	V
Driver system output voltage	V _{OUT2}	V_{LC5} – 0.3 to V_{DD} + 0.3	V
Operating ambient temperature	TA	-40 to +85	°C
Storage temperature	T _{stg}	-65 to +150	°C

- Cautions1. Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.
 - 2. Ensure that the phase relationship is $V_{DD} \ge V_{LC1} \ge V_{LC2} \ge V_{LC3} \ge V_{LC4} \ge V_{LC5}$.

* Recommended Operating Range (TA = -40 to +85°C, Vss = 0 V)

Parameter	Symbol	MIN.	TYP.	MAX.	Unit
Supply voltage	V _{DD}	2.7		5.5	V
Reference supply voltage	VLC1 to VLC4	VDD – 12		VDD	V
	V _{LC5}	V _{DD} – 12		0	V
Logic system input voltage	VIN1	0		VDD	V



Electrical Characteristics (Unless otherwise specified, T_A = -40 to +85°C, V_{DD} = 2.7 to 5.5 V)

Parameter	Symbol	Condition	MIN.	TYP. Note	MAX.	Unit
High-level input voltage	V _{IH1}	A0, DBo to DB7, E, R,/W	0.8 V _{DD}			V
	V _{IH2}	FR, M,/S, /RESET	0.8 V _{DD}			V
Low-level input voltage	V _{IL1}	A0, DBo to DB7, E, R,/W			0.2 V _{DD}	V
	V _{IL2}	FR, M,/S, /RESET			0.2 V _{DD}	V
High-level input current	Iн	A0, E, R,/W, /RESET			1	μΑ
Low-level input current	lı∟	A0, E, R,/W, /RESET			-1	μΑ
High-level output voltage	V _{OH1}	Ioυτ = −3 mA, DB₀ to DB ₇ ,	0.8 V _{DD}			٧
		V _{DD} = 4.5 to 5.5 V				
	Voн2	IOUT = -2 mA, FR, VDD = 4.5 to 5.5 V	0.8 Vdd			V
	Vонз	Iо∪т = −120 μ A, OSC ₂ ,	0.8 V _{DD}			٧
		VDD = 4.5 to 5.5 V				
Low-level output voltage	V _{OL1}	$IOUT = 3 \text{ mA}, DB_0 \text{ to } DB_7,$			0.2 V _{DD}	V
		V _{DD} = 4.5 to 5.5 V				
	Vol2	$I_{OUT} = 2 \text{ mA}, FR, V_{DD} = 4.5 \text{ to } 5.5 \text{ V}$			0.2 Vdd	V
	Vol3	$I_{OUT} = 120 \ \mu A, OSC_2,$			0.2 Vdd	V
High-level output voltage	V _{OH1}	V _{DD} = 4.5 to 5.5 V I _{OUT} = -1.5 mA, DB ₀ to DB ₇ ,	0.8 V _{DD}			V
riigii-level output voltage	V OH1	$V_{DD} = 2.7 \text{ to } 4.5 \text{ V}$	U.O VDD			V
	V _{OH2}	$I_{OUT} = -1 \text{ mA, FR, V}_{DD} = 2.7 \text{ to } 4.5 \text{ V}$	0.8 V _{DD}			V
	Vонз	$I_{OUT} = -80 \ \mu A, OSC_2,$	0.8 V _{DD}			V
		$V_{DD} = 2.7 \text{ to } 4.5 \text{ V}$	0.0 155			·
Low-level output voltage	V _{OL1}	lо∪т = 1.5 mA, DB₀ to DB ₇ ,			0.2 V _{DD}	٧
		V _{DD} = 2.7 to 4.5 V				
	V _{OL2}	IOUT = 1 mA, FR, VDD = 2.7 to 4.5 V			0.2 V _{DD}	V
	Vol3	IOUT = 80 μ A, OSC ₂ ,			0.2 VDD	V
		V _{DD} = 2.7 to 4.5 V				
High-level leak current	Ісон	DBo to DB7, VIN/OUT = VDD			3	μΑ
Low-level leak current	ILOL	DB ₀ to DB ₇ , VIN/OUT = Vss			-3	μΑ
Driver output ON resistor	Ron1	$T_A = 25^{\circ}C$, $V_{DD} = 5$ V, $V_{LC5} = V_{SS}$			7.5	kΩ
	Ron2	TA = 25°C, VDD = 3.5 V, VLC5 = VSS			50	kΩ
Static current consumption	I _{DD0}				1.0	μΑ
Dynamic current consumption	I _{DD1}	External clock: 18 kHz			15.0	μΑ
		Self-oscillation: R = 1.3 M Ω			30.0	μΑ
	I _{DD2}	During access: tcyc = 200 kHz			500	μΑ
Input capacitance	Cin	T _A = 25°C, f = 1 MHz			8.0	pF
Oscillator frequency	fosc1	In self-oscillation, V _{DD} = 5.0 V,	15	18	21	kHz
		$R = 1.3 \text{ M}\Omega \pm 2\%$				
	fosc2	In self-oscillation, VDD = 3.0 V, $R = 1.3 \ M\Omega \pm 2\%$	11	16	21	kHz
Reset time	t R	/RESET↓ →Internal reset release	1.0		1000	μs

Remark The TYP. value is a reference value when $T_A = 25$ °C.



AC Characteristics 1 (Unless otherwise specified, $T_A = -40$ to +85°C, $V_{DD} = 4.5$ to 5.5 V)

80 Series CPU Read/Write Timing

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Address hold time	t _{AH8}	A0	10			ns
Address setup time	t _{AW8}		20			ns
System cycle time	tcyc8	/WR, /RD	1000			ns
Control pulse width	tcc		200			ns
Data setup time	t _{DS8}	DBo to DB7	80			ns
Data hold time	t _{DH8}		10			ns
/RD access time	t _{ACC8}	DB ₀ to DB ₇ , C _L = 100 pF			90	ns
Output disable time	t он8		10		60	ns

68 Series CPU Read/Write Timing

Parameter		Symbol	Condition	MIN.	TYP.	MAX.	Unit
System cycle time		tcyc6	A0, R,/W	1000			ns
Address setup time		t _{AW6}		20			ns
Address hold time		t _{AH6}		10			ns
Data setup time		t _{DS6}	DB ₀ to DB ₇	80			ns
Data hold time		t _{DH6}		10			ns
Output disable time		t он6	DB ₀ to DB ₇ , C _L = 100 pF	10		60	ns
Access time		t _{ACC6}				90	ns
Enable pulse width	Read	tew	Е	100			ns
	Write			80			ns



AC Characteristics 2 (Unless otherwise specified, $T_A = -40$ to +85°C, $V_{DD} = 2.7$ to 4.5 V)

80 Series CPU Read/Write Timing

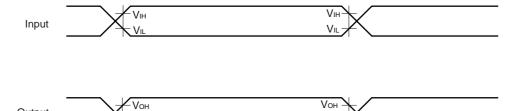
Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Address hold time	t _{AH8}	A0	20			ns
Address setup time	t _{AW8}		40			ns
System cycle time	tcyc8	/WR, /RD	2000			ns
Control pulse width	tcc		400			ns
Data setup time	t _{DS8}	DB ₀ to DB ₇	160			ns
Data hold time	t _{DH8}		20			ns
/RD access time	t _{ACC8}	DB ₀ to DB ₇ , C _L = 100 pF			180	ns
Output disable time	t он8		20		120	ns

68 Series CPU Read/Write Timing

Parameter		Symbol	Condition	MIN.	TYP.	MAX.	Unit
System cycle time		tcyc6	A0, R,/W	2000			ns
Address setup time		t _{AW6}		40			ns
Address hold time		t _{AH6}		20			ns
Data setup time		t _{DS6}	DB ₀ to DB ₇	160			ns
Data hold time		t _{DH6}		20			ns
Output disable time		t он6	DB ₀ to DB ₇ , C _L = 100 pF	20		120	ns
Access time		tACC6				180	ns
Enable pulse width	Read	tew	Е	200			ns
	Write			160			ns



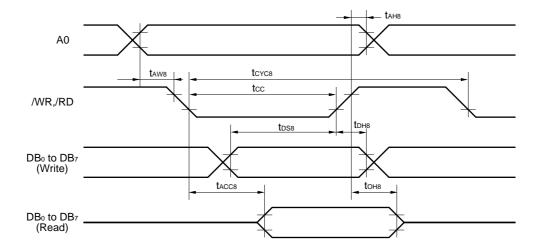
Test Point of Switching Characteristics



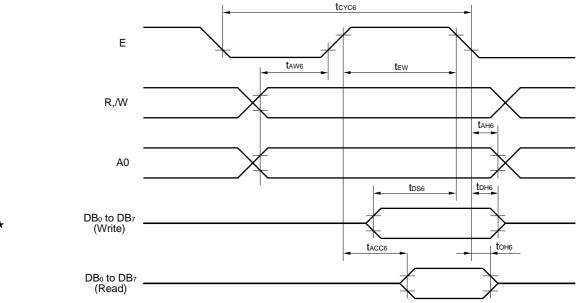
Waveforms of Switching Characteristics

80 Series CPU Read/Write Timing

Output

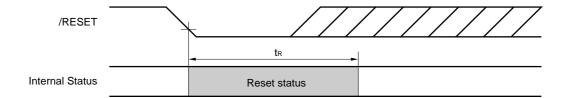


68 Series CPU Read/Write Timing

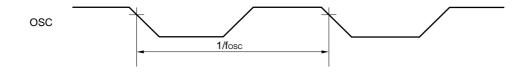


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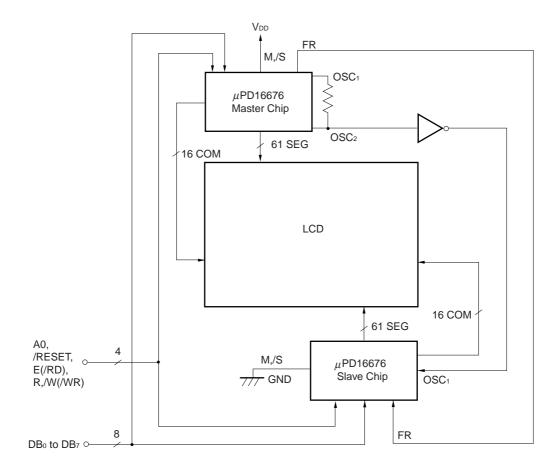
Reset



osc



8. EXAMPLE of APPLICATION CIRCUIT



NEC μ PD16676

[MEMO]

[MEMO]

NOTES FOR CMOS DEVICES

1) PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note:

Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

2 HANDLING OF UNUSED INPUT PINS FOR CMOS

Note:

No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to VDD or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

3) STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note:

Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.



★ Reference Documents

NEC Semiconductor Device Reliability/Quality Control System (C10983E)
Quality Grades to NEC's Semiconductor Devices (C11531E)

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