

## 402/384-OUTPUT TFT-LCD SOURCE DRIVER (64-GRAY SCALES)

## DESCRIPTION

The  $\mu$ PD16647 is a source driver for TFT-LCD 64-gray-scale display. Its logic circuit operates at 3.3 V and the driver circuit operates at 5.0 V. The input data is digital data at 6 bits x 3 dots, and 260,000 colors can be displayed in 64-value

★ outputs  $\gamma$ -corrected by the internal D/A converter and 10 external power supplies. The clock frequency is 50 MHz MAX.  $\mu$ PD16647 can be used in TFT-LCD panels conforming to the SVGA standards.

## FEATURES

- CMOS level input
- 402/384 outputs
- 6 bits (gray scale data) x 3 dots input
- 64-value output by 10 external power supplies and internal D/A converter
- Output dynamic range:  $V_{SS2} + 0.1$  V to  $V_{DD2} - 0.1$  V
- ★ • High-speed data transfer:  $f_{CLK} = 50$  MHz MAX. (internal data transfer rate at supply voltage  $V_{DD1}$  of logic circuit = 3.0 V)
- Level of  $\gamma$ -corrected power supply can be inverted
- Precharge-less output buffer
- Input data inversion function (INV)
- Logic supply voltage ( $V_{DD1}$ ): 3.3 V  $\pm$  0.3 V
- Driver supply voltage ( $V_{DD2}$ ): 5.0 V  $\pm$  0.5 V
- Slim TCP
- ★ • Current consumption reduction function (Bcont)

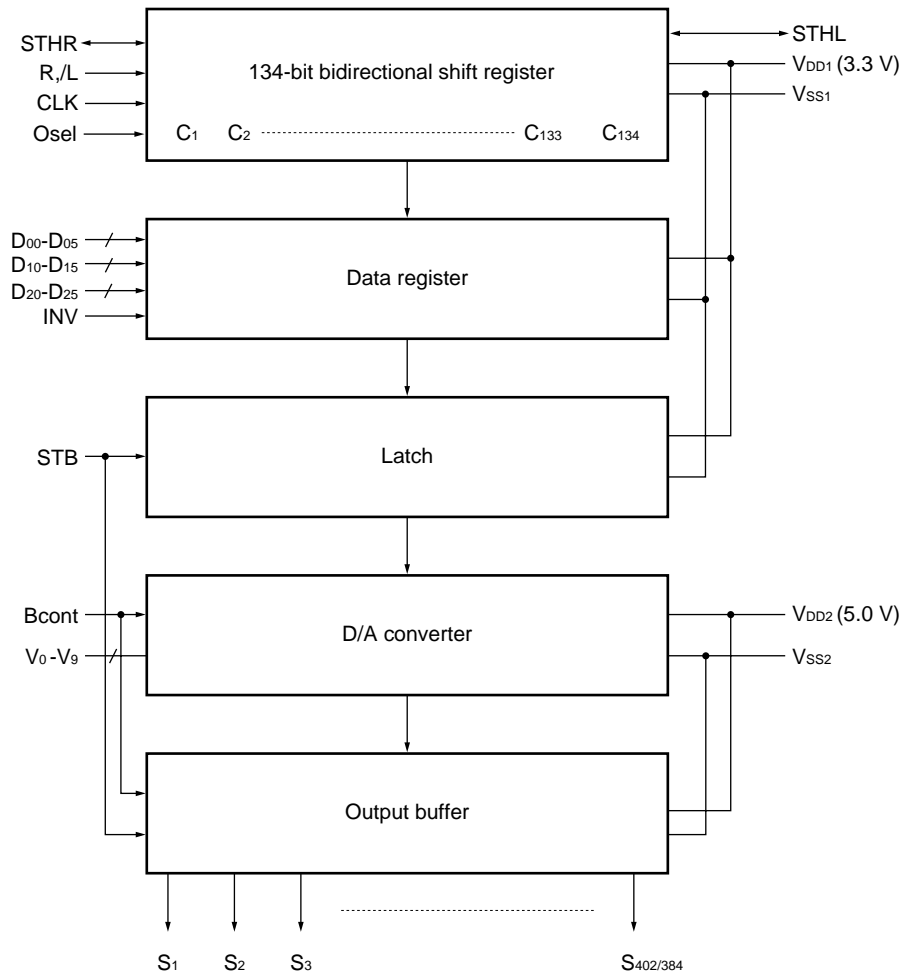
## ORDERING INFORMATION

Part Number	Package
$\mu$ PD16647N-xxx	TCP (TAB package)

- ★ **Remark** The TCP's external shape is customized. To order the required shape, please contact one of our sales representatives.

The information in this document is subject to change without notice. Before using this document, please confirm that this is the latest version.  
Not all devices/types available in every country. Please check with local NEC representative for availability and additional information.

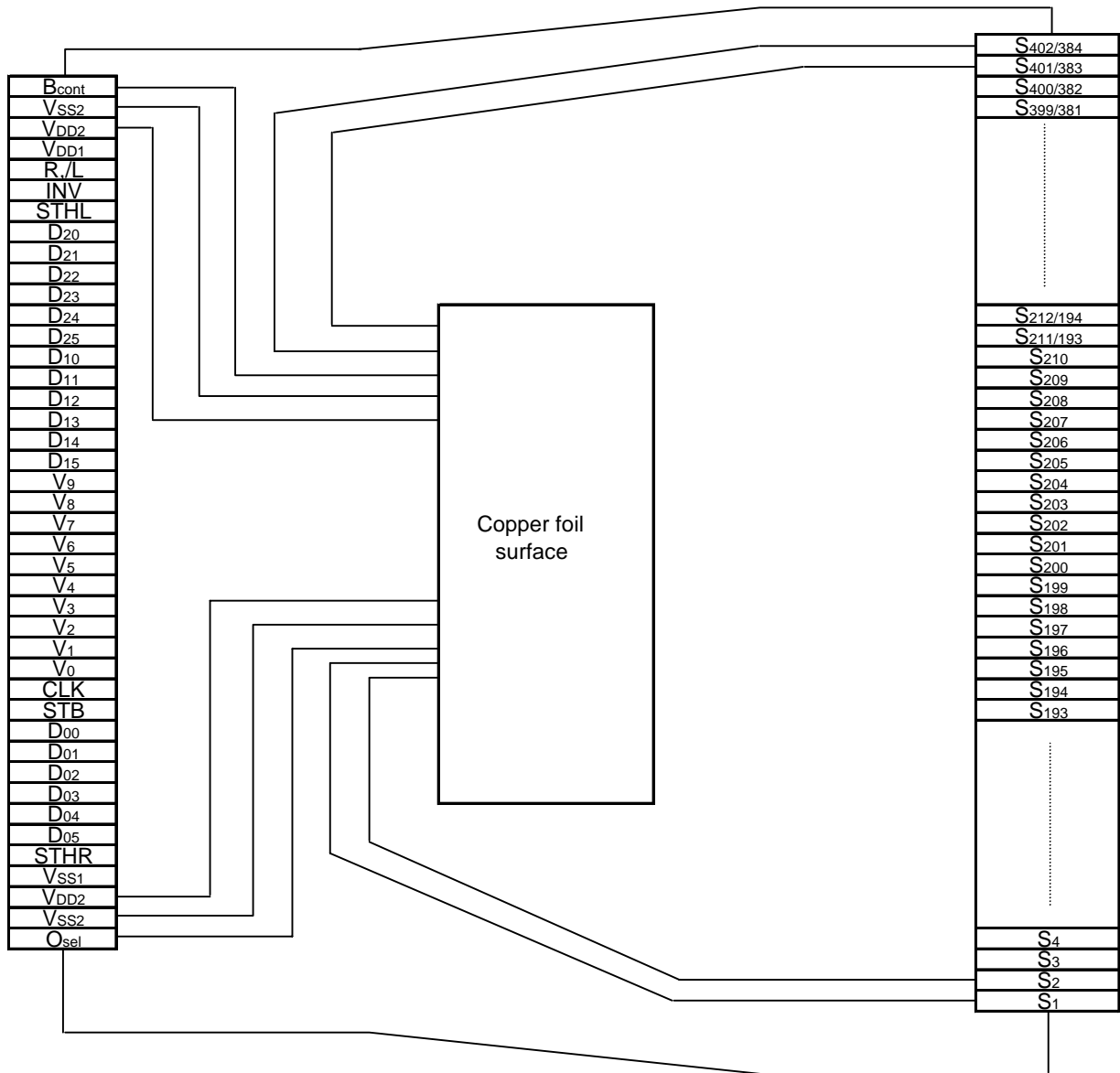
1. BLOCK DIAGRAM



**Remark** /xxx indicates active low signal.

★ 2. PIN CONFIGURATION (Top view of copper foil surface, Face-up)

μ PD16647N-xxx: TCP (TAB package)



**Remark** This figure does not specify the TCP package.

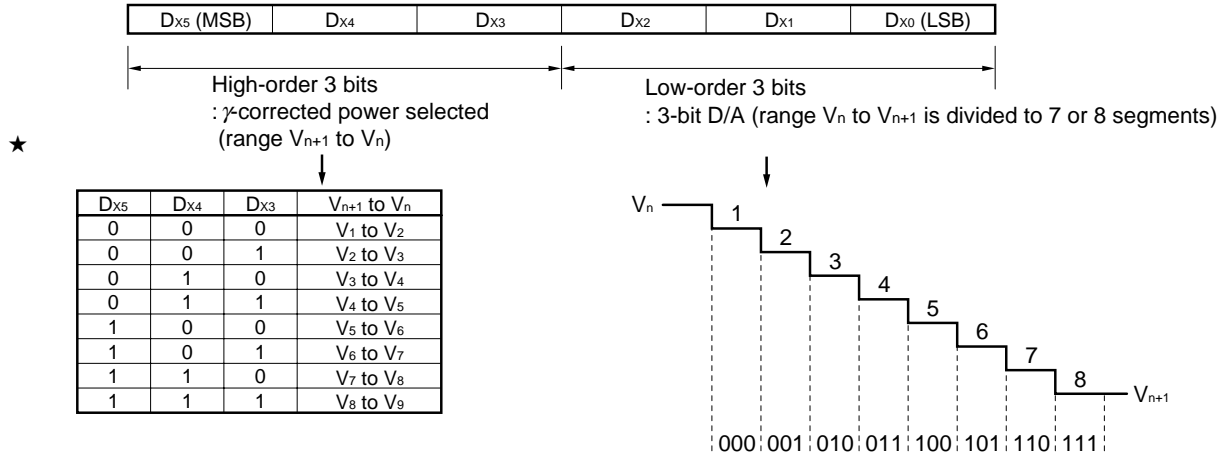
3. PIN DESCRIPTION

Pin Symbol	Pin Name	I/O	Description
S <sub>1</sub> to S <sub>402/384</sub>	Driver output	O	Output 64 gray-scale analog voltages converted from digital signals. Osel = H or open: 402 outputs (S <sub>1</sub> to S <sub>402/384</sub> ) Osel = L : 384 outputs (S <sub>1</sub> to S <sub>192</sub> , S <sub>211/193</sub> to S <sub>402/384</sub> ) S <sub>193</sub> to S <sub>210</sub> outputs are invalid in 384 outputs.
★ D <sub>00</sub> to D <sub>05</sub>	Display data input	I	Inputs 18-bit-wide display gray scale data (6 bits) x 3 dots. D <sub>X0</sub> : LSB, D <sub>X5</sub> : MSB
D <sub>10</sub> to D <sub>15</sub>			
D <sub>20</sub> to D <sub>25</sub>			
★ R, /L	Shift direction control input	I	Shift direction control pins. The shift directions are as follows. R, /L = H : STHR input, S <sub>1</sub> → S <sub>402</sub> , STHL output R, /L = L : STHL input, S <sub>402</sub> → S <sub>1</sub> , STHR output
★ STHR	Right shift start pulse I/O	I/O	This is the start pulse I/O pin when connected in cascade. Loading of display data starts when a high level is read at 1clock after from rising edge of CLK. For right shift, STHR is input and STHL is output. For left shift, STHL is input and STHR is output.
STHL	Left shift start pulse I/O		
★ Bcont	Bias control	I	This pin can be used to finely control the bias current inside the output amplifier. In cases when fine-control is necessary, connect this pin to V <sub>DD2</sub> using a resistor of 10 to 100 kΩ (per IC). When this fine-control function is not required, short-circuit this pin to V <sub>DD2</sub> . Refer to 7. <b>CURRENT CONSUMPTION REDUCTION FUNCTION.</b>
★ CLK	Shift clock input	I	Inputs shift clock to shift register. Display data is loaded to data register at rising edge of this pin (value in parentheses is for 384 outputs). Start pulse output goes high at rising edge of 134 (128) th clock after start pulse has been input, and serves as start pulse to driver in next stage. 134 (128) th clock of driver in first stage serves as start pulse of driver in next stage.
STB	Latch input	I	Contents of data register are latched at rising edge, transferred to D/A converter, and output as analog voltage corresponding to display data. Contents of internal shift register are cleared after STB has been input. One pulse of this signal is input when μPD16647 is started, and then device operates normally. For STB input timing, refer to 8. <b>ELECTRICAL SPECIFICATIONS SWITCHING CHARACTERISTICS WAVEFORM.</b>
Osel	Selection of number of outputs	I	Selects number of outputs. This pin is internally pulled up to V <sub>DD1</sub> . Osel = H or open : 402 outputs (S <sub>1</sub> to S <sub>402/384</sub> ) Osel = L : 384 outputs (S <sub>1</sub> to S <sub>192</sub> , S <sub>211/193</sub> to S <sub>402/384</sub> )
V <sub>0</sub> to V <sub>9</sub>	γ-corrected power supply	–	Inputs γ-corrected power from external source. V <sub>SS2</sub> ≤ V <sub>9</sub> ≤ V <sub>8</sub> ≤ V <sub>7</sub> ≤ V <sub>6</sub> ≤ V <sub>5</sub> ≤ V <sub>4</sub> ≤ V <sub>3</sub> ≤ V <sub>2</sub> ≤ V <sub>1</sub> ≤ V <sub>0</sub> ≤ V <sub>DD2</sub> or V <sub>SS2</sub> ≤ V <sub>0</sub> ≤ V <sub>1</sub> ≤ V <sub>2</sub> ≤ V <sub>3</sub> ≤ V <sub>4</sub> ≤ V <sub>5</sub> ≤ V <sub>6</sub> ≤ V <sub>7</sub> ≤ V <sub>8</sub> ≤ V <sub>9</sub> ≤ V <sub>DD2</sub> Maintain gray scale power supply during gray scale voltage output.
INV	Data inversion input	I	Input data can be inverted when display data is loaded. INV = H : Inverts and loads input data. INV = L : Does not invert input data.
V <sub>DD1</sub>	Logic circuit power supply	–	3.3 V ± 0.3 V
V <sub>DD2</sub>	Driver circuit power supply	–	5.0 V ± 0.5 V
V <sub>SS1</sub>	Logic ground	–	Ground
V <sub>SS2</sub>	Driver ground	–	Ground

**Caution** Be sure to turn on power in the order V<sub>DD1</sub>, logic input, V<sub>DD2</sub>, and gray scale power (V<sub>0</sub> to V<sub>9</sub>), and turn off power in the reverse order, to prevent the μPD16647 from being damaged by latch-up. Be sure to observe this power sequence even during a transition period.

### 4. RELATION BETWEEN INPUT DATA AND OUTPUT VOLTAGE VALUE

The 10 major points on the  $\gamma$ -characteristic curve of the LCD panel are arbitrarily set by external power supplies  $V_0$  through  $V_9$ . If the display data is 00H or 3FH, gray-scale voltage  $V_0$  or  $V_9$  is output. If the display data is in the range 01H to 3EH, the high-order 3 bits select an external power pair  $V_{n+1}$ ,  $V_n$ . The low-order 3 bits evenly divide the range of  $V_{n+1}$  to  $V_n$  into eight segments by means of D/A conversion (however, the ranges from  $V_8$  to  $V_7$  and from  $V_1$  to  $V_0$  are divided into seven segments) to output a 64-gray-scale voltage.



★ **Figure 4-1. Relationship between Input Data and  $\gamma$ -corrected Power Supplies**

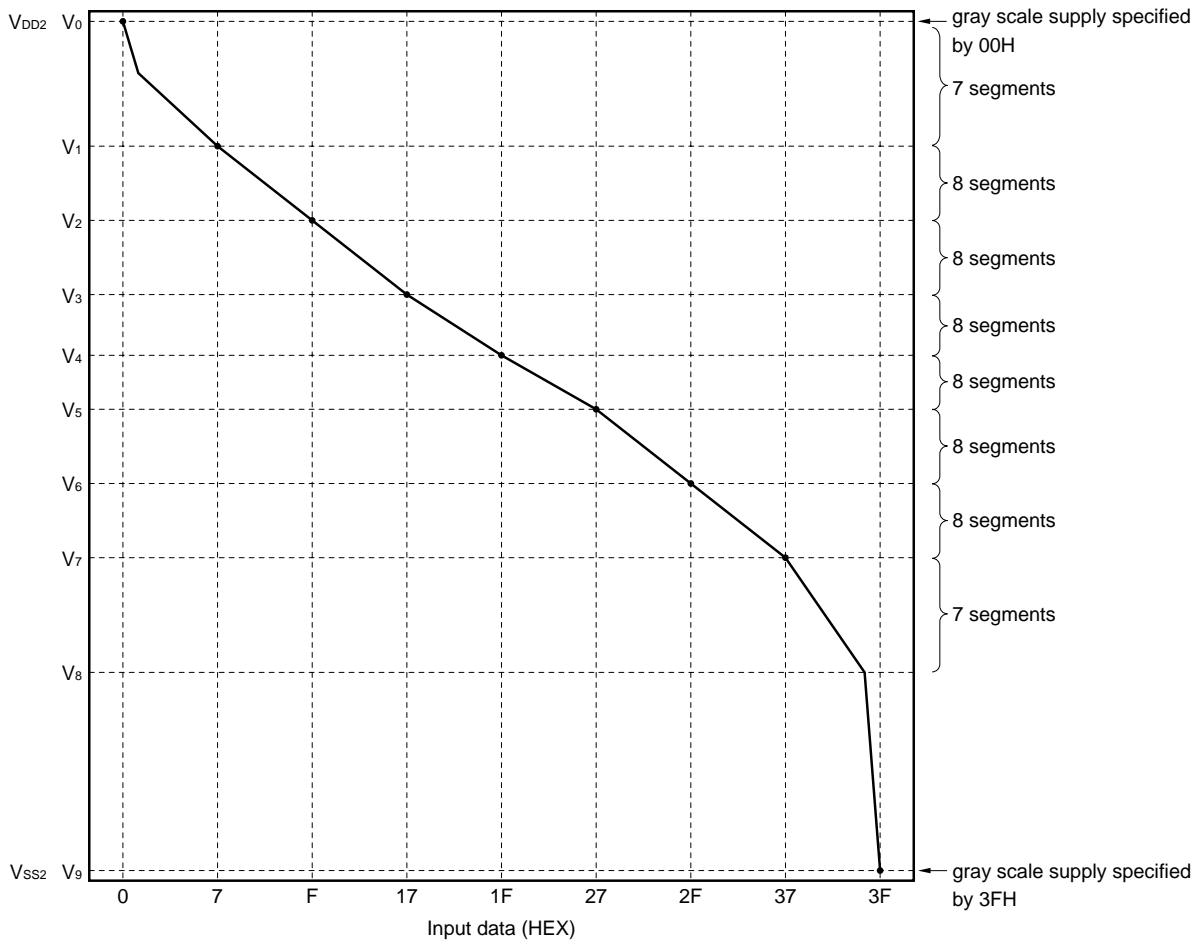


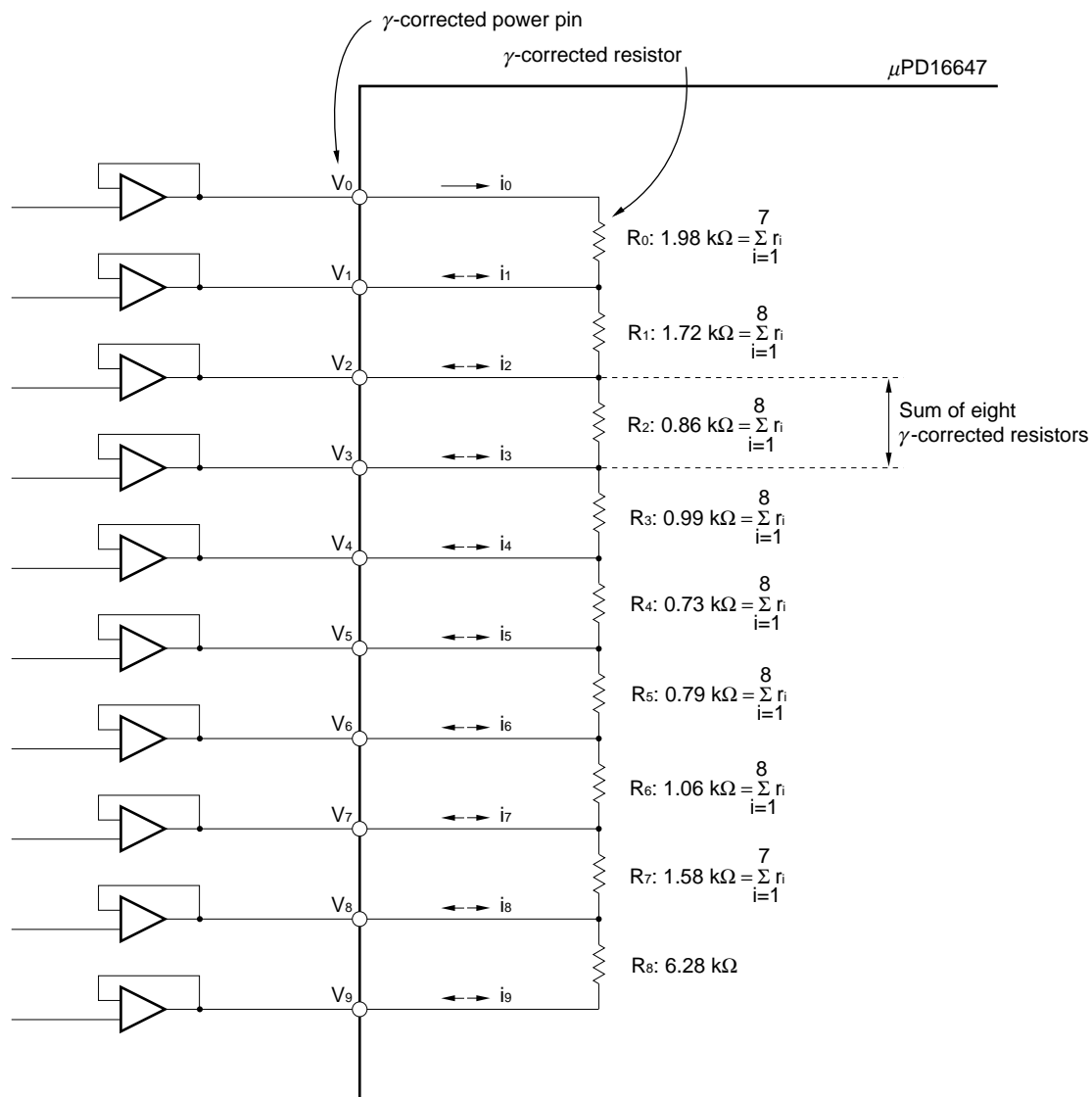
Table 4-1. Relationship between Input Data and Output Voltage

Input Data	Dx5	Dx4	Dx3	Dx2	Dx1	Dx0	Output Voltage
00H	0	0	0	0	0	0	V <sub>0</sub>
01H	0	0	0	0	0	1	V <sub>1</sub> + (V <sub>0</sub> - V <sub>1</sub> ) × 6/7
02H	0	0	0	0	1	0	V <sub>1</sub> + (V <sub>0</sub> - V <sub>1</sub> ) × 5/7
03H	0	0	0	0	1	1	V <sub>1</sub> + (V <sub>0</sub> - V <sub>1</sub> ) × 4/7
04H	0	0	0	1	0	0	V <sub>1</sub> + (V <sub>0</sub> - V <sub>1</sub> ) × 3/7
05H	0	0	0	1	0	1	V <sub>1</sub> + (V <sub>0</sub> - V <sub>1</sub> ) × 2/7
06H	0	0	0	1	1	0	V <sub>1</sub> + (V <sub>0</sub> - V <sub>1</sub> ) × 1/7
07H	0	0	0	1	1	1	V <sub>1</sub>
08H	0	0	1	0	0	0	V <sub>2</sub> + (V <sub>1</sub> - V <sub>2</sub> ) × 7/8
09H	0	0	1	0	0	1	V <sub>2</sub> + (V <sub>1</sub> - V <sub>2</sub> ) × 6/8
0AH	0	0	1	0	1	0	V <sub>2</sub> + (V <sub>1</sub> - V <sub>2</sub> ) × 5/8
0BH	0	0	1	0	1	1	V <sub>2</sub> + (V <sub>1</sub> - V <sub>2</sub> ) × 4/8
0CH	0	0	1	1	0	0	V <sub>2</sub> + (V <sub>1</sub> - V <sub>2</sub> ) × 3/8
0DH	0	0	1	1	0	1	V <sub>2</sub> + (V <sub>1</sub> - V <sub>2</sub> ) × 2/8
0EH	0	0	1	1	1	0	V <sub>2</sub> + (V <sub>1</sub> - V <sub>2</sub> ) × 1/8
0FH	0	0	1	1	1	1	V <sub>2</sub>
10H	0	1	0	0	0	0	V <sub>3</sub> + (V <sub>2</sub> - V <sub>3</sub> ) × 7/8
11H	0	1	0	0	0	1	V <sub>3</sub> + (V <sub>2</sub> - V <sub>3</sub> ) × 6/8
12H	0	1	0	0	1	0	V <sub>3</sub> + (V <sub>2</sub> - V <sub>3</sub> ) × 5/8
13H	0	1	0	0	1	1	V <sub>3</sub> + (V <sub>2</sub> - V <sub>3</sub> ) × 4/8
14H	0	1	0	1	0	0	V <sub>3</sub> + (V <sub>2</sub> - V <sub>3</sub> ) × 3/8
15H	0	1	0	1	0	1	V <sub>3</sub> + (V <sub>2</sub> - V <sub>3</sub> ) × 2/8
16H	0	1	0	1	1	0	V <sub>3</sub> + (V <sub>2</sub> - V <sub>3</sub> ) × 1/8
17H	0	1	0	1	1	1	V <sub>3</sub>
18H	0	1	1	0	0	0	V <sub>4</sub> + (V <sub>3</sub> - V <sub>4</sub> ) × 7/8
19H	0	1	1	0	0	1	V <sub>4</sub> + (V <sub>3</sub> - V <sub>4</sub> ) × 6/8
1AH	0	1	1	0	1	0	V <sub>4</sub> + (V <sub>3</sub> - V <sub>4</sub> ) × 5/8
1BH	0	1	1	0	1	1	V <sub>4</sub> + (V <sub>3</sub> - V <sub>4</sub> ) × 4/8
1CH	0	1	1	1	0	0	V <sub>4</sub> + (V <sub>3</sub> - V <sub>4</sub> ) × 3/8
1DH	0	1	1	1	0	1	V <sub>4</sub> + (V <sub>3</sub> - V <sub>4</sub> ) × 2/8
1EH	0	1	1	1	1	0	V <sub>4</sub> + (V <sub>3</sub> - V <sub>4</sub> ) × 1/8
1FH	0	1	1	1	1	1	V <sub>4</sub>
20H	1	0	0	0	0	0	V <sub>5</sub> + (V <sub>4</sub> - V <sub>5</sub> ) × 7/8
21H	1	0	0	0	0	1	V <sub>5</sub> + (V <sub>4</sub> - V <sub>5</sub> ) × 6/8
22H	1	0	0	0	1	0	V <sub>5</sub> + (V <sub>4</sub> - V <sub>5</sub> ) × 5/8
23H	1	0	0	0	1	1	V <sub>5</sub> + (V <sub>4</sub> - V <sub>5</sub> ) × 4/8
24H	1	0	0	1	0	0	V <sub>5</sub> + (V <sub>4</sub> - V <sub>5</sub> ) × 3/8
25H	1	0	0	1	0	1	V <sub>5</sub> + (V <sub>4</sub> - V <sub>5</sub> ) × 2/8
26H	1	0	0	1	1	0	V <sub>5</sub> + (V <sub>4</sub> - V <sub>5</sub> ) × 1/8
27H	1	0	0	1	1	1	V <sub>5</sub>
28H	1	0	1	0	0	0	V <sub>6</sub> + (V <sub>5</sub> - V <sub>6</sub> ) × 7/8
29H	1	0	1	0	0	1	V <sub>6</sub> + (V <sub>5</sub> - V <sub>6</sub> ) × 6/8
2AH	1	0	1	0	1	0	V <sub>6</sub> + (V <sub>5</sub> - V <sub>6</sub> ) × 5/8
2BH	1	0	1	0	1	1	V <sub>6</sub> + (V <sub>5</sub> - V <sub>6</sub> ) × 4/8
2CH	1	0	1	1	0	0	V <sub>6</sub> + (V <sub>5</sub> - V <sub>6</sub> ) × 3/8
2DH	1	0	1	1	0	1	V <sub>6</sub> + (V <sub>5</sub> - V <sub>6</sub> ) × 2/8
2EH	1	0	1	1	1	0	V <sub>6</sub> + (V <sub>5</sub> - V <sub>6</sub> ) × 1/8
2FH	1	0	1	1	1	1	V <sub>6</sub>
30H	1	1	0	0	0	0	V <sub>7</sub> + (V <sub>6</sub> - V <sub>7</sub> ) × 7/8
31H	1	1	0	0	0	1	V <sub>7</sub> + (V <sub>6</sub> - V <sub>7</sub> ) × 6/8
32H	1	1	0	0	1	0	V <sub>7</sub> + (V <sub>6</sub> - V <sub>7</sub> ) × 5/8
33H	1	1	0	0	1	1	V <sub>7</sub> + (V <sub>6</sub> - V <sub>7</sub> ) × 4/8
34H	1	1	0	1	0	0	V <sub>7</sub> + (V <sub>6</sub> - V <sub>7</sub> ) × 3/8
35H	1	1	0	1	0	1	V <sub>7</sub> + (V <sub>6</sub> - V <sub>7</sub> ) × 2/8
36H	1	1	0	1	1	0	V <sub>7</sub> + (V <sub>6</sub> - V <sub>7</sub> ) × 1/8
37H	1	1	0	1	1	1	V <sub>7</sub>
38H	1	1	1	0	0	0	V <sub>8</sub> + (V <sub>7</sub> - V <sub>8</sub> ) × 6/7
39H	1	1	1	0	0	1	V <sub>8</sub> + (V <sub>7</sub> - V <sub>8</sub> ) × 5/7
3AH	1	1	1	0	1	0	V <sub>8</sub> + (V <sub>7</sub> - V <sub>8</sub> ) × 4/7
3BH	1	1	1	0	1	1	V <sub>8</sub> + (V <sub>7</sub> - V <sub>8</sub> ) × 3/7
3CH	1	1	1	1	0	0	V <sub>8</sub> + (V <sub>7</sub> - V <sub>8</sub> ) × 2/7
3DH	1	1	1	1	0	1	V <sub>8</sub> + (V <sub>7</sub> - V <sub>8</sub> ) × 1/7
3EH	1	1	1	1	1	0	V <sub>8</sub>
3FH	1	1	1	1	1	1	V <sub>9</sub>

### 4.1 γ-Corrected Power Circuit

The reference power supply of the D/A converter consists of a ladder circuit with a total of 64 resistors, and resistance  $\Sigma r_i$  between  $\gamma$ -corrected power pins differs depending on each pair of  $\gamma$ -corrected power pins. One pair of  $\gamma$ -corrected power pins consists of seven or eight series resistors, and resistance  $\Sigma r_i$  in the figure below is indicated as the sum of the seven or eight resistors. The resistance ratio between the  $\gamma$ -corrected power pins ( $\Sigma r_i$  ratio) is designed to be a value relatively close to the ratio of the  $\gamma$ -corrected voltages  $V_1$  through  $V_8$  (gray scale voltages in 7 steps) used in an actual LCD panel. Under ideal conditions where there is no difference between the two, therefore, there is no voltage difference between the voltage of the  $\gamma$ -corrected power supplies and the gray scale voltages in 7 steps of the resistor ladder circuits of the μPD16647, and no current flows into the  $\gamma$ -corrected power pins  $V_1$  through  $V_8$ . As a result, a voltage follower circuit is not necessary.

Figure 4-2. γ-Corrected Power Circuit



### 5. RELATION BETWEEN INPUT DATA AND OUTPUT VOLTAGE

Data format : 6 bits x RGB (3 dots)

Input width : 18 bits (1 pixel data)

(1) R,/L = H (right shift)

Output	S <sub>1</sub>	S <sub>2</sub>	S <sub>3</sub>	S <sub>4</sub>	...	S <sub>401/383</sub>	S <sub>402/384</sub>
Data	D <sub>00</sub> to D <sub>05</sub>	D <sub>10</sub> to D <sub>15</sub>	D <sub>20</sub> to D <sub>25</sub>	D <sub>00</sub> to D <sub>05</sub>	...	D <sub>10</sub> to D <sub>15</sub>	D <sub>20</sub> to D <sub>25</sub>

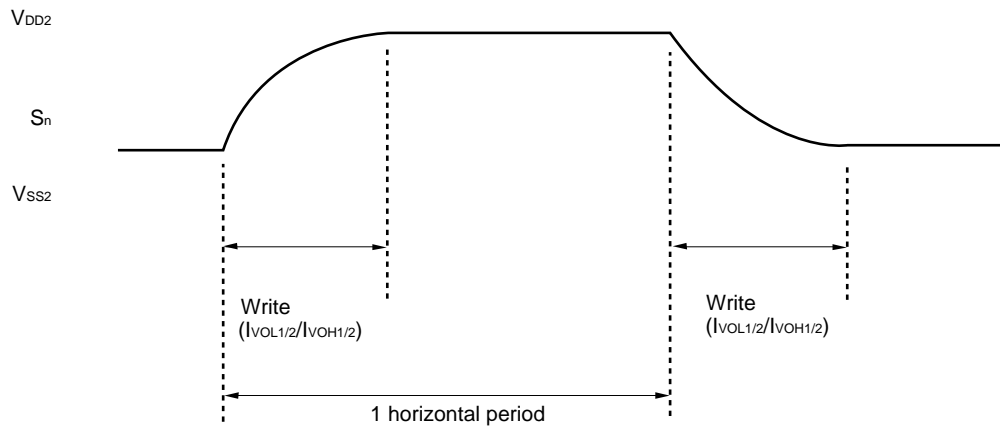
(2) R,/L = L (left shift)

Output	S <sub>1</sub>	S <sub>2</sub>	S <sub>3</sub>	S <sub>4</sub>	...	S <sub>401/383</sub>	S <sub>402/384</sub>
Data	D <sub>00</sub> to D <sub>05</sub>	D <sub>10</sub> to D <sub>15</sub>	D <sub>20</sub> to D <sub>25</sub>	D <sub>00</sub> to D <sub>05</sub>	...	D <sub>10</sub> to D <sub>15</sub>	D <sub>20</sub> to D <sub>25</sub>

### 6. OPERATION OF OUTPUT BUFFER

The output buffer consists of an operational amplifier circuit that does not perform precharge operation. Therefore, driver output current  $I_{VOH1/2}$  is the charging current to the LCD, and  $I_{VOL1/2}$  is the discharging current.

Figure 6-1. LCD panel driving waveform of μPD16647

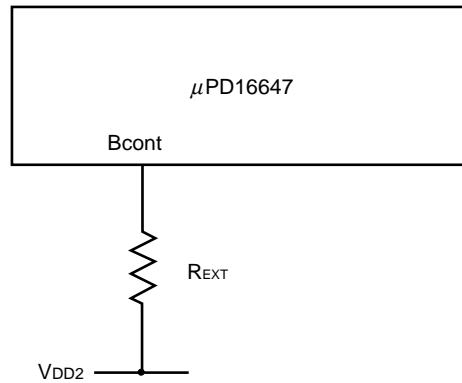




★ 7. CURRENT CONSUMPTION REDUCTION FUNCTION

It is possible to fine-control the bias current of the output amplifier (Static current consumption) by using the bias current control function (Bcont pin). When using this function, connect this pin to the stabilized V<sub>DD2</sub> potential using an external resistor (R<sub>EXT</sub>). When not using this function, however, short-circuit this pin to V<sub>DD2</sub>.

Figure 7-1. Bias Current Control Function/Bcont



Refer to the table below for the percentage of current regulation compare to normal mode, when using the bias current control function.

Table 7-1. Current Consumption Regulation Percentage Compared to Normal Mode (V<sub>DD1</sub> = 3.3 V, V<sub>DD2</sub> = 5 V)

R <sub>EXT</sub> (kΩ)	Current Consumption Regulation Percentage (%)
Short-circuit	100
10	95
20	91
40	85
80	79

**Remark** Be aware that the above current consumption regulation percentages are not product-characteristic guaranteed as they are based on the results of simulation.

**Caution** Because the bias-current control functions control the bias current in the output amplifier and regulate the over-all current consumption of the driver IC, when this occurs, the characteristics of the output amplifier will simultaneously change. Therefore, when using these functions, be sure to sufficiently evaluate the picture quality.

8. ELECTRICAL SPECIFICATIONS

**Absolute Maximum Ratings (V<sub>SS1</sub> = V<sub>SS2</sub> = 0 V)**

Parameter	Symbol	Ratings	Unit
Logic Supply Voltage	V <sub>DD1</sub>	-0.3 to +4.5	V
Driver Supply Voltage	V <sub>DD2</sub>	-0.3 to +6.0	V
Input Voltage	V <sub>I</sub>	-0.3 to V <sub>DD1,2</sub> + 0.3	V
Output Voltage	V <sub>O</sub>	-0.3 to V <sub>DD1,2</sub> + 0.3	V
Operating Ambient Temperature	T <sub>A</sub>	-10 to +75	°C
Storage Temperature	T <sub>stg</sub>	-55 to +125	°C

**Caution** Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

**Recommended Operating Range (T<sub>A</sub> = -10 to +75°C, V<sub>SS1</sub> = V<sub>SS2</sub> = 0 V)**

Parameter	Symbol	MIN.	TYP.	MAX.	Unit
Logic Supply Voltage	V <sub>DD1</sub>	3.0	3.3	3.6	V
Driver Supply Voltage	V <sub>DD2</sub>	4.5	5.0	5.5	V
High-level Input Voltage	V <sub>IH</sub>	0.7 V <sub>DD1</sub>		V <sub>DD1</sub>	V
Low-level Input Voltage	V <sub>IL</sub>	0		0.3 V <sub>DD1</sub>	V
γ-corrected Supply Voltage	V <sub>0</sub> to V <sub>9</sub>	V <sub>SS2</sub> + 0.1		V <sub>DD2</sub> - 0.1	V
★ Clock Frequency	f <sub>CLK</sub>			50	MHz

Electrical Characteristics (T<sub>A</sub> = -10 to +75°C, V<sub>DD1</sub> = 3.3 V ± 0.3 V, V<sub>DD2</sub> = 5.0 V ± 0.5 V, V<sub>SS1</sub> = V<sub>SS2</sub> = 0 V,

Short-circuit Bcont to V<sub>DD2</sub>)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit	
Input Leakage Current	I <sub>IL</sub>	D <sub>00</sub> to D <sub>05</sub> , D <sub>10</sub> to D <sub>15</sub> , D <sub>20</sub> to D <sub>25</sub> , R/L, STB			±1.0	μA	
Pull-up Resistor	R <sub>PU</sub>	V <sub>DD1</sub> = 3.3 V	40	100	250	kΩ	
High-level Output Voltage	V <sub>OH</sub>	STHR (STHL), I <sub>o</sub> = -1.0 mA	V <sub>DD1</sub> - 0.5			V	
Low-level Output Voltage	V <sub>OL</sub>	STHR (STHL), I <sub>o</sub> = +1.0 mA			0.5	V	
Static Current Consumption of γ-corrected Power	I <sub>vn1</sub>	V <sub>DD1</sub> = 3.3 V, V <sub>n</sub> to V <sub>n+1</sub> = 0.5 V, V <sub>DD2</sub> = 5.0 V	V <sub>0</sub> to V <sub>1</sub>	126	253	506	μA
			V <sub>1</sub> to V <sub>2</sub>	145	291	582	μA
			V <sub>2</sub> to V <sub>3</sub>	289	579	1158	μA
			V <sub>3</sub> to V <sub>4</sub>	252	504	1008	μA
			V <sub>4</sub> to V <sub>5</sub>	343	686	1372	μA
			V <sub>5</sub> to V <sub>6</sub>	315	631	1262	μA
			V <sub>6</sub> to V <sub>7</sub>	237	474	948	μA
			V <sub>7</sub> to V <sub>8</sub>	158	316	632	μA
			V <sub>8</sub> to V <sub>9</sub>	40	80	160	μA
Driver Output Current	I <sub>VOH2</sub>	V <sub>OUT</sub> = 4.4 V, V <sub>X</sub> = 4.9 V <sup>Note1</sup> , V <sub>DD1</sub> = 3.3 V, V <sub>DD2</sub> = 5.0 V	-0.12		-0.03	mA	
	I <sub>VOL2</sub>	V <sub>OUT</sub> = 0.6 V, V <sub>X</sub> = 0.1 V <sup>Note1</sup> , V <sub>DD1</sub> = 3.3 V, V <sub>DD2</sub> = 5.0 V	0.04		0.16	mA	
Output Voltage Deviation	ΔV <sub>O</sub>	V <sub>DD1</sub> = 3.3 V, V <sub>DD2</sub> = 5.0 V, V <sub>OUT</sub> = 2.5 V <sup>Note1</sup>		±10	±20	mV	
Output Swing Difference Deviation	ΔV <sub>P-P</sub>	Input data		±5		mV	
Output Voltage Range	V <sub>O</sub>	Input data : 00H to 3FH	V <sub>SS2</sub> + 0.1		V <sub>DD2</sub> - 0.1	V	
Dynamic Logic Current Consumption	I <sub>DD1</sub>	No load, V <sub>DD2</sub> = 3.3 V <sup>Note2</sup>		0.5	2.5	mA	
Dynamic Driver Current Consumption	I <sub>DD2</sub>	No load, V <sub>DD2</sub> = 5.0 V <sup>Note2</sup>		5.0	10.0	mA	

- Notes 1.** V<sub>X</sub> refers to the output voltage of analog output pins S<sub>1</sub> to S<sub>402/384</sub>.  
V<sub>OUT</sub> refers to the voltage applied to analog output pins S<sub>1</sub> to S<sub>402/384</sub>.
- 2.** The STB cycle is specified at 31 μs and f<sub>CLK</sub> = 16 MHz.

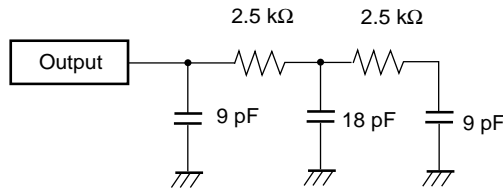
Switching Characteristics (T<sub>A</sub> = -10 to +75°C, V<sub>DD1</sub> = 3.3 V ± 0.3 V, V<sub>DD2</sub> = 5.0 V ± 0.5 V, V<sub>SS1</sub> = V<sub>SS2</sub> = 0 V,

Short-circuit Bcont to V<sub>DD2</sub>)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Start Pulse Delay Time	t <sub>PLH1</sub>	C <sub>L</sub> = 15 pF		7	12	ns
	t <sub>PHL1</sub>			7	12	ns
★ Driver Output Delay Time	t <sub>PLH2</sub>	V <sub>DD2</sub> = 5.0 V, 5 kΩ +36 pF	V <sub>OUT</sub> : 0.1 → 4.9 V <sup>Note</sup>	2.2	10	μs
	t <sub>PLH3</sub>			2.9	12	μs
	t <sub>PHL2</sub>	V <sub>OUT</sub> : 4.9 → 0.1 V <sup>Note</sup>	2.6	10	μs	
	t <sub>PHL3</sub>		3.6	12	μs	
★ Input Capacitance	C <sub>I1</sub>	STHR (STHL), T <sub>A</sub> = 25°C		10	15	pF
	C <sub>I2</sub>	V <sub>0</sub> to V <sub>9</sub> , T <sub>A</sub> = 25°C		100	150	pF
	C <sub>I3</sub>	Input pins are except STHR (STHL), and V <sub>0</sub> to V <sub>9</sub> , T <sub>A</sub> = 25°C		10	15	pF

★ **Note** V<sub>OUT</sub> refers to the voltage applied to analog output pins S<sub>1</sub> to S<sub>402/384</sub>.

<Output Load>

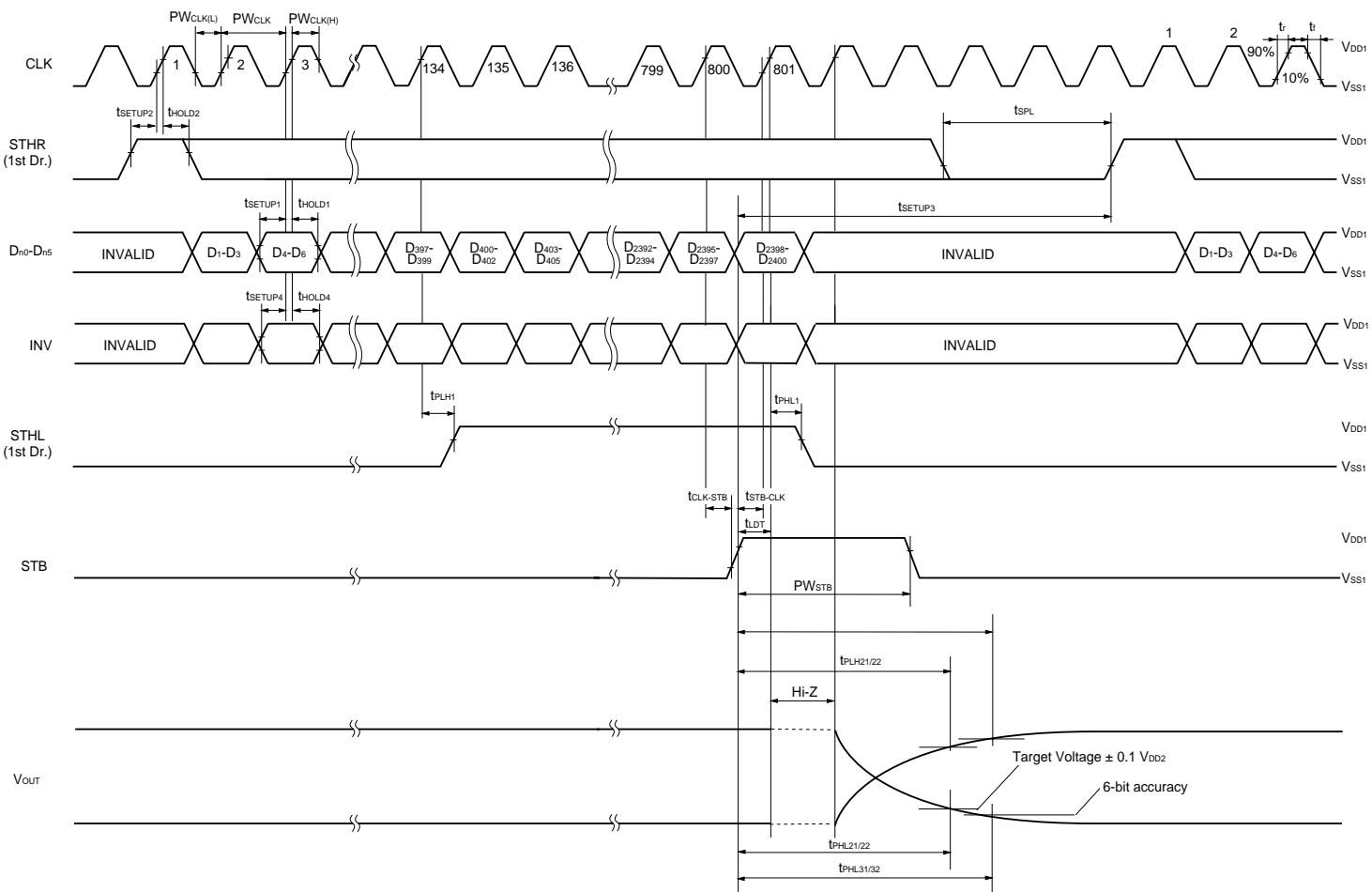


Timing Requirements (T<sub>A</sub> = -10 to +75°C, V<sub>DD1</sub> = 3.3 V ± 0.3 V, V<sub>DD2</sub> = 5.0 V ± 0.5 V, V<sub>SS1</sub> = V<sub>SS2</sub> = 0 V)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Clock Pulse Width	PW <sub>CLK</sub>		20			ns
Clock High Period	PW <sub>CLK (H)</sub>		4			ns
Clock Low Period	PW <sub>CLK (L)</sub>		4			ns
Data Setup Time	t <sub>SETUP1</sub>		4			ns
Data Hold Time	t <sub>HOLD1</sub>		0			ns
Start Pulse Setup Time	t <sub>SETUP2</sub>		4			ns
Start Pulse Hold Time	t <sub>HOLD2</sub>		0			ns
INV Setup Time	t <sub>SETUP4</sub>		4			ns
INV Hold Time	t <sub>HOLD4</sub>		0			ns
Start Pulse Low Period	t <sub>SPL</sub>		2			CLK
STB Setup Time	t <sub>SETUP3</sub>		1			CLK
STB Pulse Width	PW <sub>STB</sub>		2			CLK
Last Data Timing	t <sub>LDT</sub>				1	CLK
CLK to STB Time	t <sub>CLK-STB</sub>	CLK ↑ → STB ↑	7			ns
STB to CLK Time	t <sub>STB-CLK</sub>	STB ↑ → CLK ↑	7			ns

**SWITCHING CHARACTERISTIC WAVEFORM (R./L = H)**

Unless otherwise specified, the input level is defined to be  $V_{IH} = 0.7 V_{DD1}$ ,  $V_{IL} = 0.3 V_{DD1}$ .



**9. RECOMMENDED MOUNTING CONDITIONS**

The following conditions must be met for mounting conditions of the μPD16647.

For more details, refer to the **Semiconductor Device Mounting Technology Manual (C10535E)**.

Please consult with our sales offices in case other mounting process is used, or in case the mounting is done under different conditions.

μPD16647N-xxx: TCP (TAB package)

Mounting Condition	Mounting Method	Condition
Thermocompression	Soldering	Heating tool 300 to 350°C, heating for 2 to 3 sec; pressure 100 g (per solder).
	ACF (Adhesive Conductive Film)	Temporary bonding 70 to 100°C; pressure 3 to 8 kg/cm <sup>2</sup> ; time 3 to 5 sec. Real bonding 165 to 180°C pressure 25 to 45 kg/cm <sup>2</sup> time 30 to 40 secs (When using the anisotropy conductive film SUMIZAC1003 of Sumitomo Bakelite, Ltd).

**Caution** To find out the detailed conditions for mounting the ACF part, please contact the ACF manufacturing company. Be sure to avoid using two or more mounting methods at a time.

**NOTES FOR CMOS DEVICES****① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS**

Note:

Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

**② HANDLING OF UNUSED INPUT PINS FOR CMOS**

Note:

No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to  $V_{DD}$  or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

**③ STATUS BEFORE INITIALIZATION OF MOS DEVICES**

Note:

Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

## Reference Documents

NEC Semiconductor Device Reliability/Quality Control System (C10983E)

Quality Grades On NEC Semiconductor Devices (C11531E)

- **The information in this document is current as of September, 2001. The information is subject to change without notice. For actual design-in, refer to the latest publications of NEC's data sheets or data books, etc., for the most up-to-date specifications of NEC semiconductor products. Not all products and/or types are available in every country. Please check with an NEC sales representative for availability and additional information.**
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