NEC

MOS INTEGRATED CIRCUIT
μPD16364

160-BIT HIGH-VOLTAGE CMOS DRIVER

DESCRIPTION

The μPD16364 is a high-voltage CMOS driver for EL display. It consists of 4 × 40/8 × 20-bit data latch, 160-bits data latch, 160-bit level shifter, and a high-voltage CMOS driver. The logic circuit operates on 5-V power supply (CMOS level input), so that it can be connected to a micro-controller. The driver block is comprised of 60 V, 25 mA MAX. high-voltage output buffer, and both the logic block and driver block employ a CMOS, allowing operation with low power consumption.

FEATURES

- High-voltage Full CMOS process
- High-voltage output (60 V, 25 mA MAX.)
- 4 × 40/8 × 20-bit data latch (4/8-bit data input)
- High-speed data transfer (f_{CLK} = 16 MHz: in cascade connection)
- Wide operating temperature range (T_A = –40 to +85°C)

ORDERING INFORMATION

Part Number	Package
μPD16364N -×××	TCP (TAB package)

Remark The TCP's external shape is customized. To order the required shape, please contact one of our sales representatives.

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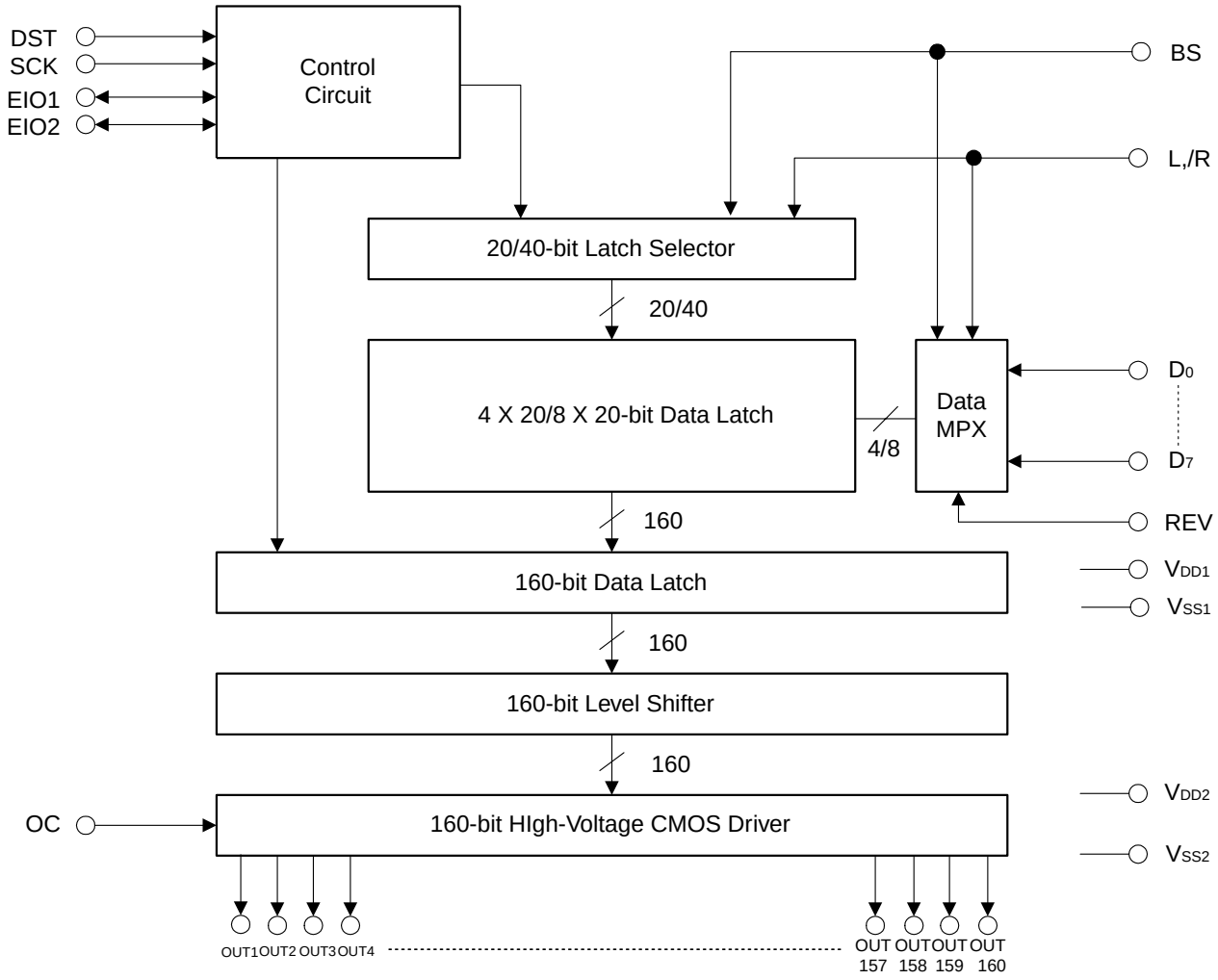
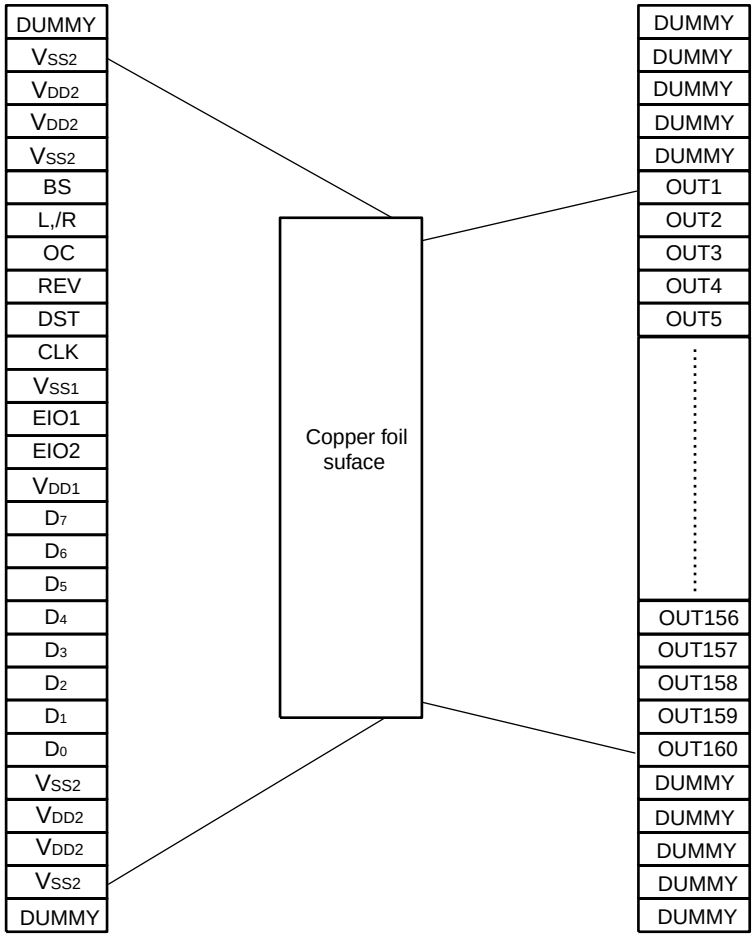
The mark ★ shows major revised points.

1. BLOCK DIAGRAM



Remark /xxx indicates active low signal.

2. PIN CONFIGURATION (μPD16364N-xxx: Copper foil surface, Face-up)



Remark This figure does not specify the TCP package.

Caution Be sure to use all the V_{DD1}, V_{DD2}, V_{SS1}, and V_{SS2} pins. Keep the V_{SS1} and V_{SS2} pins at the same voltage level.

3. PIN FUNCTIONS

Pin Symbol	Pin Name	I/O	Description
★ EIO1	Enable I/O1	I/O	L,/R pin = "L" level: Input L,/R pin = "H" level: Output
★ EIO2	Enable I/O2	I/O	L,/R pin = "H" level: Input L,/R pin = "L" level: Output
SCK	Shift Clock Input	Input	Fall edge operation. Input shift clock for 4 x 40/8 x 20-bit data latch.
DST	Data Strobe Input	Input	Fall edge operation. Data are latched to 160-bits data latch and also set outputs of OUT1 to OUT160.
D_0 to D_7	Data Input	Input	Data input. When BS is low level, D_4 to D_7 pins should be connected to V_{SS1} or V_{DD1}.
L,/R	Select Left or Right Shift	Input	Refer to **4.TRUTH TABLE**
OC	Output Control	Input	When OC pin is low level, output is normal operation. When OC pin is high level, output become low level.
REV	Invert Input Data	Input	When REV pin is low level, input data D_0 to D_7 are latched without inversion. When REV pin is high level, input data D_0 to D_7 are inverted before latching.
BS	Bus Select	Input	When BS pin is low level, data bus is4 bits. When BS pin is high level, data bus is 8 bits.
OUT1 to OUT160	High-voltage output	Output	Output level is V_{SS2} or V_{DD2}. These outputs are changed by falling edge of DST pin.
V_{DD1}	Logic power supply	–	Logic power supply
V_{DD2}	Driver power supply	–	Driver power supply
V_{SS1}	Logic ground	–	Grounding
V_{SS2}	Driver ground	–	Grounding

4. TRUTH TABLE

Shift Register Block (4 x 40 data latch, BS = L)

L,/R	SCK	1	2	3	...	40
L level	D_3	1	5	9	...	157
	D_2	2	6	10	...	158
	D_1	3	7	11	...	159
	D_0	4	8	12	...	160
H level	D_3	160	156	152	...	4
	D_2	159	155	151	...	3
	D_1	158	154	150	...	2
	D_0	157	153	149	...	1

Shift Register Block (8 x 20 data latch, BS = H)

★

L,/R	SCK	1	2	3	...	20
L level	D_7	1	9	17	...	153
	D_6	2	10	18	...	154
	D_5	3	11	19	...	155
	D_4	4	12	20	...	156
	D_3	5	13	21	...	157
	D_2	6	14	22	...	158
	D_1	7	15	23	...	159
	D_0	8	16	24	...	160
H level	D_7	160	152	144	...	8
	D_6	159	151	143	...	7
	D_5	158	150	142	...	6
	D_4	157	149	141	...	5
	D_3	156	148	140	...	4
	D_2	155	147	139	...	3
	D_1	154	146	138	...	2
	D_0	153	145	137	...	1

Control Block

L,/R	EIO1	EIO2
H level	Out	In
L level	In	Out

Driver Block

OC	REV	Dn	Driver Output
L	L	L	L
L	L	H	H
L	H	L	H
L	H	H	L
H	x	x	L (All driver outputs are L.)

5. ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings (T_A = 25°C, V_{SS1} = V_{SS2} = 0 V)

Parameter	Symbol	Rating	Unit
Logic Part Supply Voltage	V_{DD1}	–0.5 to +6.0	V
Driver Part Supply Voltage	V_{DD2}	–0.5 to +60	V
Logic Part Input Voltage	V_{I1}	–0.5 to V_{DD1} + 0.5	V
Logic Part Output Voltage	V_{O1}	–0.5 to V_{DD1} + 0.5	V
Driver Part Output Voltage	V_{O2}	–0.5 to V_{DD2} + 0.5	V
Logic Part Output Current	I_{O1}	±10	mA
Driver Part Output Current	I_{O2}	±25	mA
Operating Ambient Temperature	T_A	–40 to +85	°C
Storage Temperature	T_{stg}	–55 to +125	°C

Cautions 1. $T_A \geq 25°C$, load should be alleviated at a rate of –4.5 mW/°C.

2. Product qualify may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

Recommended Operating Range (T_A = –40 to +85°C, V_{SS1} = V_{SS2} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Logic Part Supply Voltage	V_{DD1}		4.5	5.0	5.5	V
Driver Part Supply Voltage	V_{DD2}		20		55	V
High-Level Input Voltage	V_{IH}		0.8 V_{DD1}		V_{DD1}	V
Low-Level Input Voltage	V_{IL}		0		0.2 V_{DD1}	V
Driver Part Output Current	I_{OL2}				+20	mA
	I_{OH2}				–20	mA

Caution Turn of and off power sequence must be as follows:

Turn-on sequence: V_{DD1} → Input → V_{DD2}

Turn-off sequence: V_{DD2} → Input →V_{DD1}

Electrical Characteristics (T_A = –40 to +85°C, V_{DD1} = 4.5 to 5.5 V, V_{DD2} = 55 V, V_{SS1} = V_{SS2} = 0 V,)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
High-Level Output Voltage	V_{OH1}	Logic, I_{OH1} = –0.4 mA,	V_{DD1} – 0.4			V
	V_{OH2}	OUT1 to OUT160, I_{OH2} = –1.0 mA	V_{DD2} – 0.4			V
Low-Level Output Voltage	V_{OL1}	Logic, I_{OL1} = 0.4 mA			0.4	V
	V_{OL2}	OUT1 to OUT160, I_{OL2} = 1.0 mA			0.4	V
High-Level Input Current	I_{IH}	V_I = V_{DD1}			5.0	μA
Low-Level Input Current	I_{IL}	V_I = 0 V			–5.0	μA
High-Level Input Voltage	V_{IH}	Logic	0.8 V_{DD1}			V
Low-Level Input Voltage	V_{IL}	Logic			0.2 V_{DD1}	V
R_{ON} Variance	R_{VAR}	OUT1 to OUT160 (in one chip under constant T_j [Note1])			±30	%
Logic Part Dynamic Current Consumption	I_{DD1}	**Note2**			10	mA
Driver Part Dynamic Current Consumption	I_{DD2}	**Note2**			10	mA
Standby Current	$I_{standby}$	**Note3**			500	μA

Notes 1. R_{var} = (1 – Xn/X_{avg}) x 100

Xn = Impedance of OUTn, X_{avg} = Impedance of average

I_{OH2} = –1.0 mA, I_{OL2} = 1.0 mA

2. f_{SCK} = 16 MHz, f_{DST} = 36 kHz, V_{IN} = V_{DD1} or V_{SS1}, no load

3. V_{IN} = V_{DD1} or V_{SS1}, no load

Switching Characteristics (T_A = –40 to +85°C, V_{DD1} = 4.5 to 5.5 V, V_{DD2} = 55 V, V_{SS1} = V_{SS2} = 0 V)

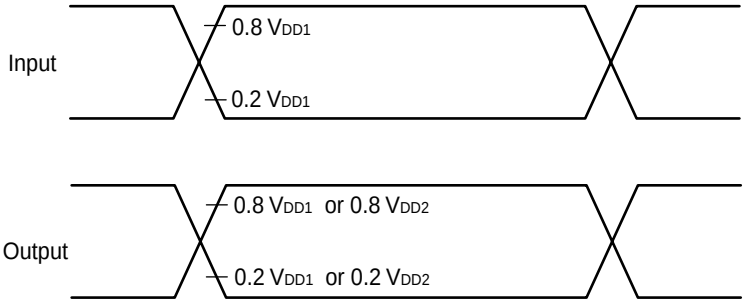
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Enable Pulse Delay Time	t_{PLH1}	DST↓ → EIOn↑, C_L = 30 pF			70	ns
	t_{PHL2}	Last SCK↓ → EIOn↓, C_L = 30 pF			40	ns
Driver Output Delay Time	t_{PHL3}	DST↓ → OUT1 to OUT160,			7	μs
	t_{PLH3}	C_L = 2000 pF			7	μs
Input Capacitance	C_I				20	pF

Timing Requirement (T_A = –40 to +85°C, V_{DD1} = 4.5 to 5.5 V, V_{DD2} = 55 V, V_{SS1} = V_{SS2} = 0 V, t_r = t_f = 13.0 ns)

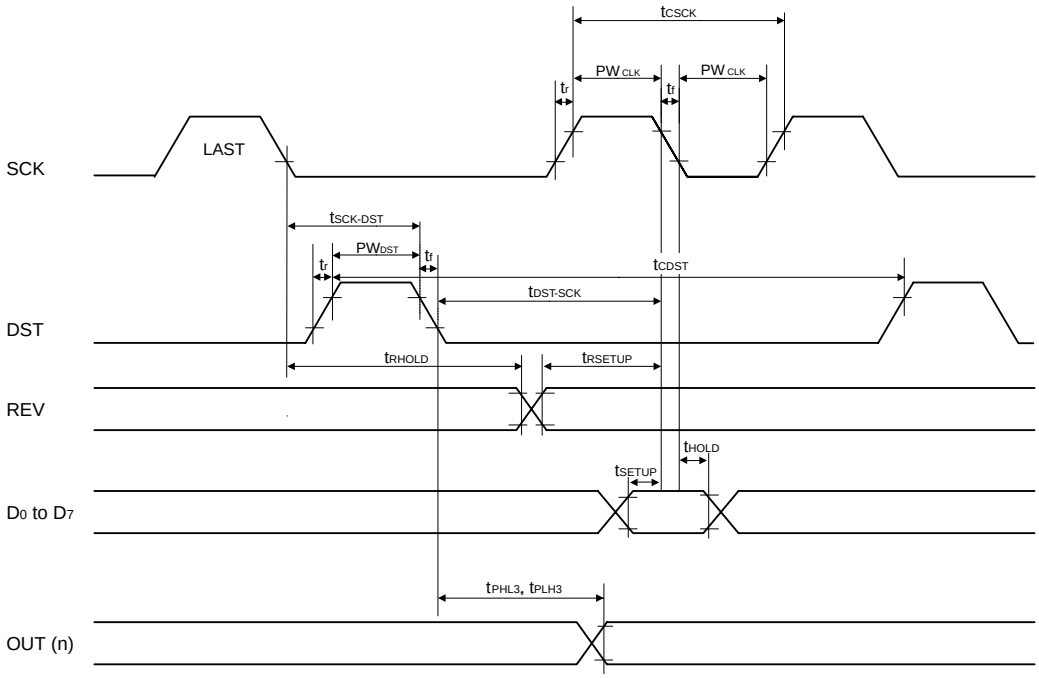
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
SCK Cycle Time	t_{CSCK}		62			ns
SCK Pulse Width	PW_{CLK}		20			ns
DST Cycle Time	t_{CDST}		1000			ns
DST High-Level Pulse Width	PW_{DST}		30			ns
DST-SCK Time	$t_{DST-SCK}$	DST↓ → 1st SCK ↓	100			ns
SCK-DST Time	$t_{SCK-DST}$	Last SCK↓ → DST ↓	30			ns
Data Setup Time	t_{SETUP}		20			ns
Data Hold Time	t_{HOLD}		20			ns
REV Setup Time	t_{RSETUP}		40			ns
REV Hold Time	t_{RHOLD}		30			ns
EIO-SCK Time1	$t_{EIO-SCK1}$	EIOn↓ → 1st SCK ↓	22			ns
EIO-SCK Time2	$t_{EIO-SCK2}$	EIOn↑ → 1st SCK ↑	25			ns

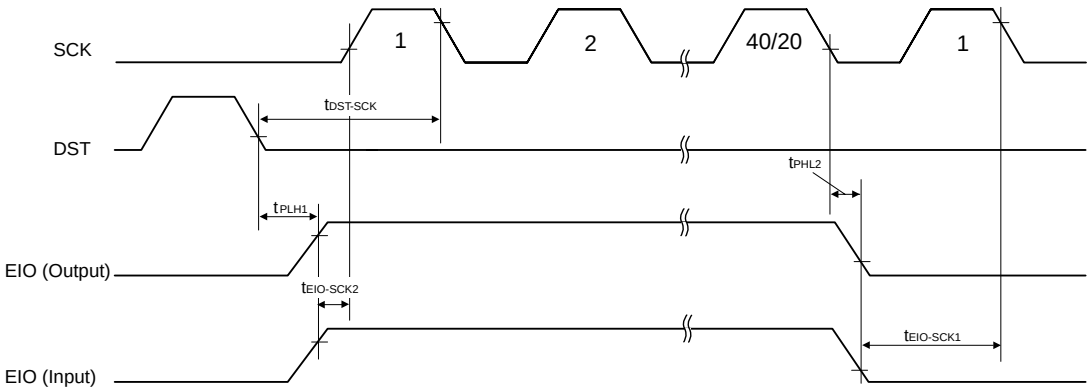
Switching Characteristics and Timing Requirements Waveform

Timing requirement waveform

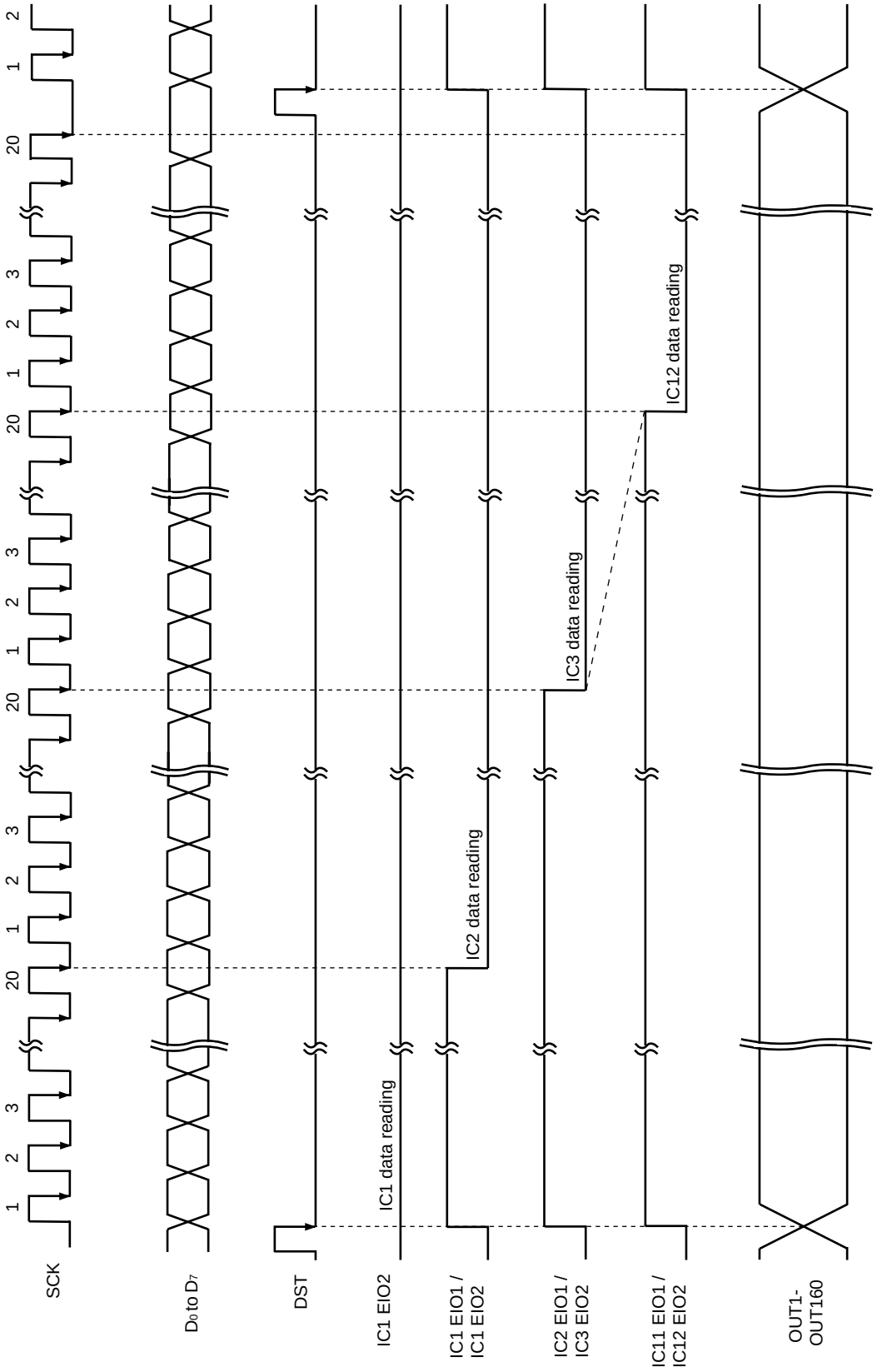


Switching characteristics waveform





Timing Example (640 dots x 3/line, BS = H, L,/R = H)



6. RECOMMENDED SOLDERING CONDITIONS

The following conditions must be met for soldering conditions of the μPD16364.

For more details, refer to the **Semiconductor Device Mounting Technology Manual (C10535E).**

Please consult with our sales offices in case other soldering process is used, or in case the soldering is done under different conditions.

μPD16364N-×××: TCP (TAB package)

Mounting Condition	Mounting Method	Condition
Thermocompression	Soldering	Heating tool 300 to 350°C: heating for 2 to 3 seconds: pressure 100g (per solder)
	ACF (Adhesive Conductive Film)	Temporary bonding 70 to 100°C: pressure 3 to 8 kg/cm^2: time 3 to 5 seconds. Real bonding 165 to 180°C: pressure 25 to 45 kg/cm^2: time 30 to 40 seconds. (When using the anisotropy conductive film SUMIZAC1003 of Sumitomo Bakelite, Ltd.)

Caution To find out the detailed conditions for packaging the ACF part, please contact the ACF manufacturing company. Be sure to avoid using two or more packaging methods at a time.

[MEMO]

[MEMO]

[MEMO]

NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note:

Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note:

No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note:

Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

Reference Documents

NEC Semiconductor Device Reliability/Quality Control System (C10983E)

Semiconductor Device Mounting Technology (C10535E)

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