DATA SHEET

BIPOLAR ANALOG INTEGRATED CIRCUIT

μPC8182TB

3 V, 2.9 GHz SILICON MMIC MEDIUM OUTPUT POWER AMPLIFIER FOR MOBILE COMMUNICATIONS

DESCRIPTION

The μPC8182TB is a silicon monolithic integrated circuit designed as amplifier for mobile communications. This IC operates at 3V. The medium output power is suitable for RF-TX of mobile communications system.

This IC is manufactured using NEC's 30 GHz f_{max} UHS0 (Ultra High Speed Process) silicon bipolar process. This process uses direct silicon nitride passivation film and gold electrodes. These materials can protect the chip surface from pollution and prevent corrosion/migration. Thus, this IC has excellent performance, uniformity and reliability.

FEATURES

- High-density surface mounting : 6-pin super minimold package (2.0 × 1.25 × 0.9 mm)
- Supply voltage : V_{CC} = 2.7 to 3.3 V
- Circuit current : I_{CC} = 30 mA TYP. @ V_{CC} = 3.0 V
- Medium output power : $P_{O(1dB)}$ = +9.5 dBm TYP. @ f = 0.9 GHz
  $P_{O(1dB)}$ = +9.0 dBm TYP. @ f = 1.9 GHz
  $P_{O(1dB)}$ = +8.0 dBm TYP. @ f = 2.4 GHz
- Power gain : G_P = 21.5 dB TYP. @ f = 0.9 GHz
  G_P = 20.5 dB TYP. @ f = 1.9 GHz
  G_P = 20.5 dB TYP. @ f = 2.4 GHz
- Upper limit operating frequency : f_u = 2.9 GHz TYP. @ 3 dB bandwidth

APPLICATION

- Buffer amplifiers on 1.9 to 2.4 GHz mobile communications system.

ORDERING INFORMATION

Part Number	Package	Marking	Supplying Form
μPC8182TB-E3	6-pin super minimold	C3F	Embossed tape 8 mm wide. 1, 2, 3 pins face the perforation side of the tape. Qty 3 kpcs/reel.

Remark To order evaluation samples, please contact your local NEC sales office.
(Part number for sample order: μPC8182TB)

Caution Electro-static sensitive devices

The information in this document is subject to change without notice. Before using this document, please confirm that this is the latest version.
Not all devices/types available in every country. Please check with local NEC representative for availability and additional information.

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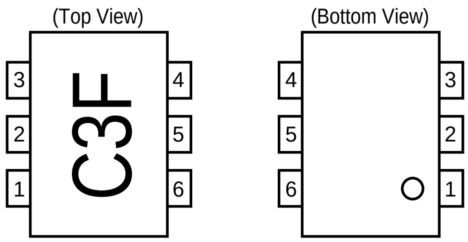
The mark ★ shows major revised points.

PIN CONNECTIONS



Pin No.	Pin Name
1	INPUT
2	GND
3	GND
4	OUTPUT
5	GND
6	V_{CC}

PRODUCT LINE-UP (T_A = +25°C, V_{CC} = V_{out} = 3.0 V, Z_S = Z_L = 50 Ω)

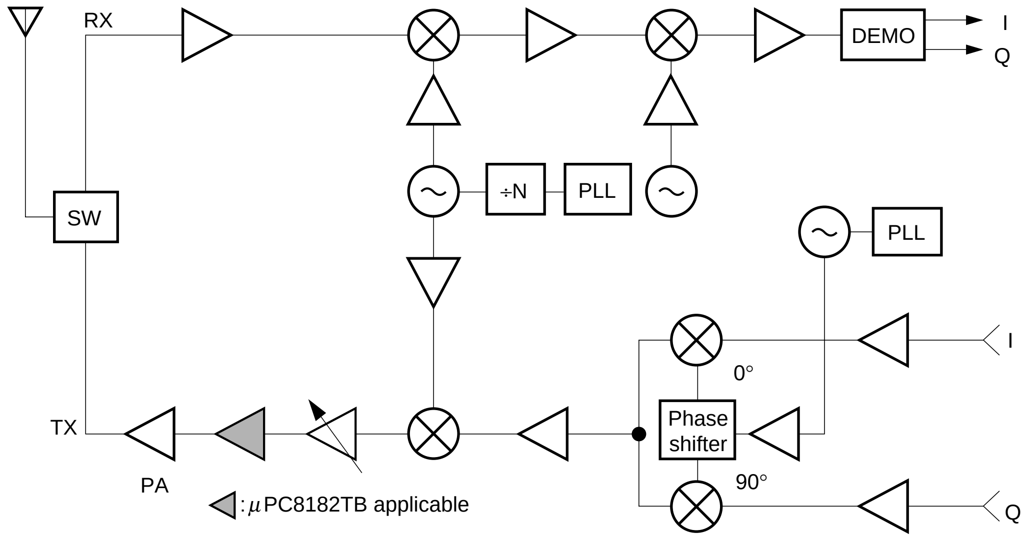
Part No.	f_u (GHz)	$P_{O\ (1\ dB)}$ (dBm)	G_P (dB)	I_{CC} (mA)	Package	Marking
★ μPC8182TB	2.9	+9.5 @ f = 0.9 GHz	21.5 @ f = 0.9 GHz	30.0	6-pin super minimold	C3F
		+9.0 @ f = 1.9 GHz	20.5 @ f = 1.9 GHz			
		+8.0 @ f = 2.4 GHz	20.5 @ f = 2.4 GHz			
μPC2762T	2.9	+8.0 @ f = 0.9 GHz	13.0 @ f = 0.9 GHz	26.5	6-pin minimold	C1Z
μPC2762TB		+7.0 @ f = 1.9 GHz	15.5 @ f = 1.9 GHz		6-pin super minimold	
μPC2763T	2.7	+9.5 @ f = 0.9 GHz	20.0 @ f = 0.9 GHz	27.0	6-pin minimold	C2A
μPC2763TB		+6.5 @ f = 1.9 GHz	21.0 @ f = 1.9 GHz		6-pin super minimold	
μPC2771T	2.2	+11.5 @ f = 0.9 GHz	21.0 @ f = 0.9 GHz	36.0	6-pin minimold	C2H
μPC2771TB		+9.5 @ f = 1.5 GHz	21.0 @ f = 1.5 GHz		6-pin super minimold	

Remark Typical performance. Please refer to ELECTRICAL CHARACTERISTICS in detail.

Caution The package size distinguishes between minimold and super minimold.

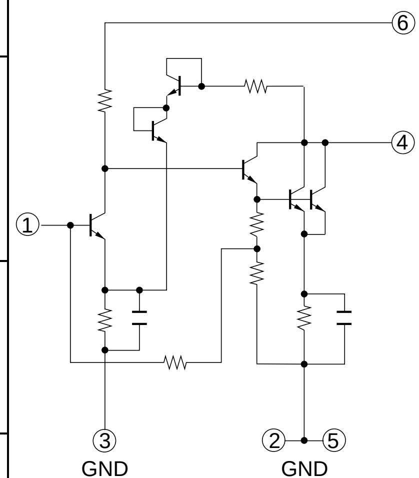
SYSTEM APPLICATION EXAMPLE

Digital cellular telephone



Caution The insertion point is different due to the specifications of conjunct devices.

PIN EXPLANATION

Pin No.	Pin Name	Applied Voltage (V)	Pin Voltage (V)[Note]	Function and Applications	Internal Equivalent Circuit
★ 1	INPUT	–	0.99	Signal input pin. A internal matching circuit, configured with resistors, enables 50 Ω connection over a wide band. A multi-feedback circuit is designed to cancel the deviations of h_{FE} and resistance. This pin must be coupled to signal source with capacitor for DC cut.	
4	OUTPUT	Voltage as same as V_{CC} through external inductor	–	Signal output pin. The inductor must be attached between V_{CC} and output pins to supply current to the internal output transistors.	
6	V_{CC}	2.7 to 3.3	–	Power supply pin, which biases the internal input transistor. This pin should be externally equipped with bypass capacitor to minimize its impedance.	
2 3 5	GND	0	–	Ground pin. This pin should be connected to system ground with minimum inductance. Ground pattern on the board should be formed as wide as possible. All the ground pins must be connected together with wide ground pattern to decrease impedance difference.	

Note Pin voltage is measured at V_{CC} = 3.0 V.

★ ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Conditions	Ratings	Unit
Supply Voltage	V_{CC}	T_A = +25°C, pin 4 and 6	3.6	V
Total Circuit Current	I_{CC}	T_A = +25°C	60	mA
Power Dissipation	P_D	Mounted on double copper clad 50 × 50 × 1.6 mm epoxy glass PWB (T_A = +85°C)	270	mW
Operating Ambient Temperature	T_A		–40 to +85	°C
Storage Temperature	T_{stg}		–55 to +150	°C
Input Power	P_{in}	T_A = +25°C	+10	dBm

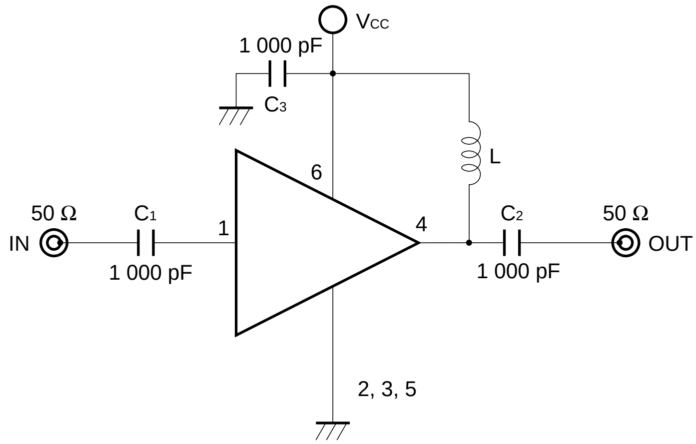
RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	MIN.	TYP.	MAX.	Unit	Remark
Supply Voltage	V_{CC}	2.7	3.0	3.3	V	Same voltage should be applied to pin 4 and 6.
Operating Ambient Temperature	T_A	–40	+25	+85	°C	–

★ ELECTRICAL CHARACTERISTICS (Unless otherwise specified, T_A = +25°C, V_{CC} = V_{out} = 3.0 V, Z_S = Z_L = 50 Ω)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
Circuit Current	I_{CC}	No signal	–	30.0	38.0	mA
Power Gain	G_P	f = 0.9 GHz	19.0	21.5	25.0	dB
		f = 1.9 GHz	18.0	20.5	24.0	
		f = 2.4 GHz	18.0	20.5	24.0	
Noise Figure	NF	f = 0.9 GHz	–	4.5	6.0	dB
		f = 1.9 GHz	–	4.5	6.0	
		f = 2.4 GHz	–	5.0	6.5	
Upper Limit Operating Frequency	f_u	3 dB down below from gain at f = 0.1 GHz	2.6	2.9	–	GHz
Isolation	ISL	f = 0.9 GHz	28	33	–	dB
		f = 1.9 GHz	27	32	–	
		f = 2.4 GHz	26	31	–	
Input Return Loss	RL_{in}	f = 0.9 GHz	5	8	–	dB
		f = 1.9 GHz	7	10	–	
		f = 2.4 GHz	9	12	–	
Output Return Loss	RL_{out}	f = 0.9 GHz	7	10	–	dB
		f = 1.9 GHz	8	11	–	
		f = 2.4 GHz	11	14	–	
Gain 1 dB Compression Output Power	$P_{O\ (1dB)}$	f = 0.9 GHz	+7.0	+9.5	–	dBm
		f = 1.9 GHz	+6.5	+9.0	–	
		f = 2.4 GHz	+5.5	+8.0	–	
Saturated Output Power	$P_{O\ (sat)}$	f = 0.9 GHz, P_{in} = –5 dBm	–	+11.0	–	dBm
		f = 1.9 GHz, P_{in} = –5 dBm	–	+10.5	–	
		f = 2.4 GHz, P_{in} = –5 dBm	–	+10.0	–	

TEST CIRCUIT



COMPONENTS OF TEST CIRCUIT FOR MEASURING ELECTRICAL CHARACTERISTICS

	Type	Value
C_1, C_2	Bias Tee	1 000 pF
C_3	Capacitor	1 000 pF
L	Bias Tee	1 000 nH

EXAMPLE OF ACTUAL APPLICATION COMPONENTS

	Type	Value	Operating Frequency
C_1 to C_3	Chip capacitor	1 000 pF	100 MHz or higher
L	Chip inductor	100 nH	100 MHz or higher
		10 nH	2.0 GHz or higher

INDUCTOR FOR THE OUTPUT PIN

The internal output transistor of this IC consumes 20 mA, to output medium power. To supply current for output transistor, connect an inductor between the Vcc pin (pin 6) and output pin (pin 4). Select large value inductance, as listed above.

The inductor has both DC and AC effects. In terms of DC, the inductor biases the output transistor with minimum voltage drop to output enable high level. In terms of AC, the inductor make output-port-impedance higher to get enough gain. In this case, large inductance and Q is suitable.

For above reason, select an inductance of 100 Ω or over impedance in the operating frequency. The gain is a peak in the operating frequency band, and suppressed at lower frequencies.

The recommendable inductance can be chosen from example of actual application components list as shown above.

CAPACITORS FOR THE V_{CC}, INPUT, AND OUTPUT PINS

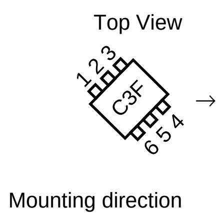
Capacitors of 1 000 pF are recommendable as the bypass capacitor for the Vcc pin and the coupling capacitors for the input and output pins.

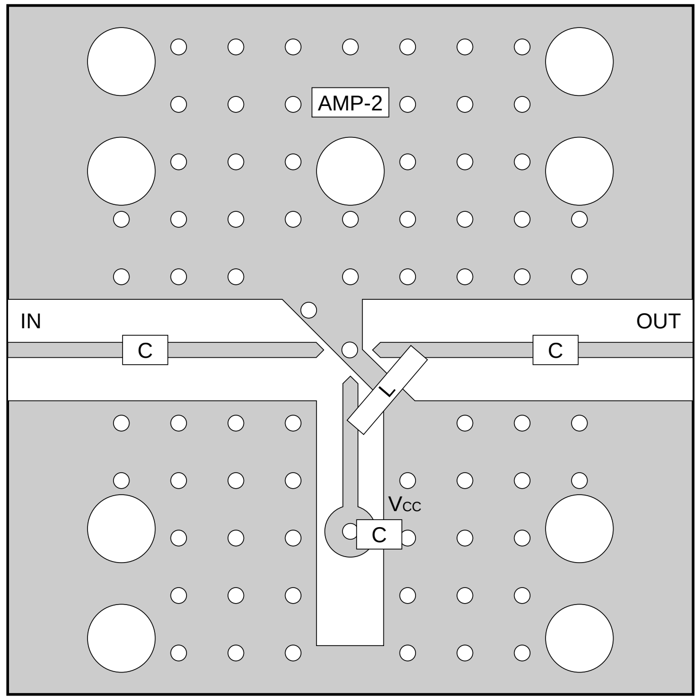
The bypass capacitor connected to the Vcc pin is used to minimize ground impedance of Vcc pin. So, stable bias can be supplied against Vcc fluctuation.

The coupling capacitors, connected to the input and output pins, are used to cut the DC and minimize RF serial impedance. Their capacitance are therefore selected as lower impedance against a 50 Ω load. The capacitors thus perform as high pass filters, suppressing low frequencies to DC.

To obtain a flat gain from 100 MHz upwards, 1 000 pF capacitors are used in the test circuit. In the case of under 10 MHz operation, increase the value of coupling capacitor such as 10 000 pF. Because the coupling capacitors are determined by equation, $C = 1/(2\pi Rfc)$.

ILLUSTRATION OF THE TEST CIRCUIT ASSEMBLED ON EVALUATION BOARD





COMPONENT LIST

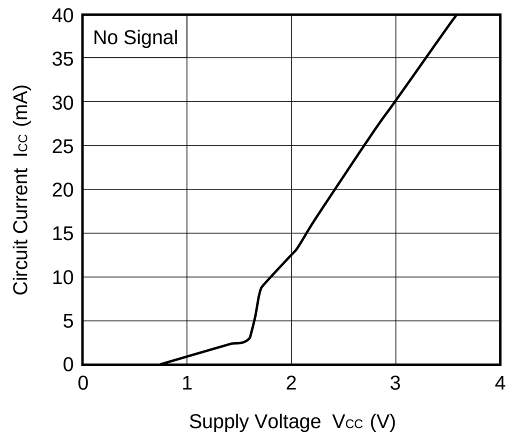
	Value
C	1 000 pF
L	Example: 10 nH

Notes

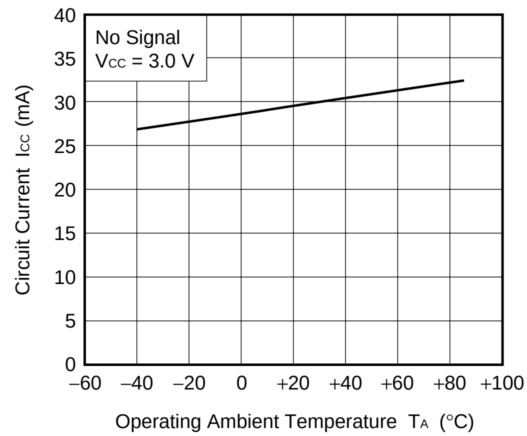
1. 30 × 30 × 0.4 mm double sided copper clad polyimide board.
2. Back side: GND pattern
3. Solder plated on pattern
4. ○ ◯ : Through holes

★ TYPICAL CHARACTERISTICS (Unless otherwise specified, T_A = +25°C)

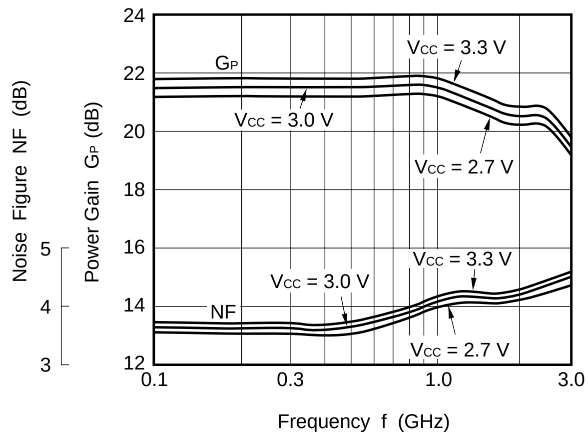
CIRCUIT CURRENT vs. SUPPLY VOLTAGE



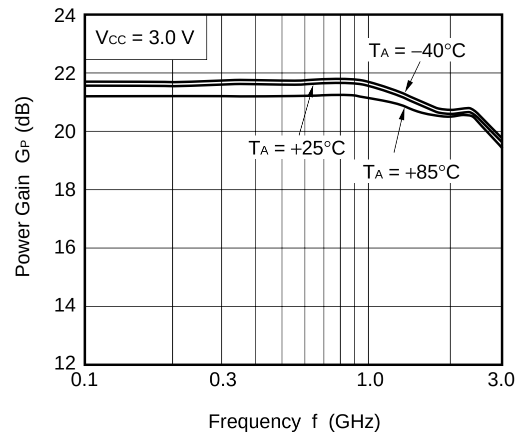
CIRCUIT CURRENT vs. OPERATING AMBIENT TEMPERATURE



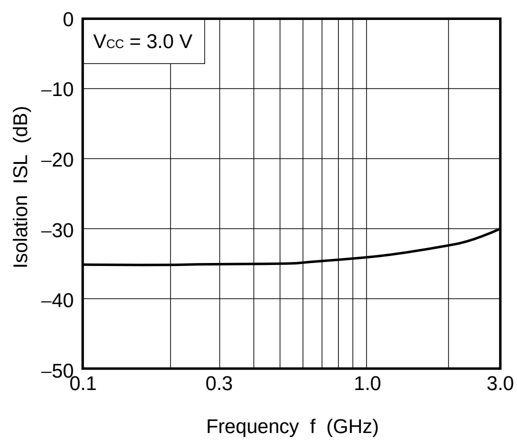
NOISE FIGURE, POWER GAIN vs. FREQUENCY



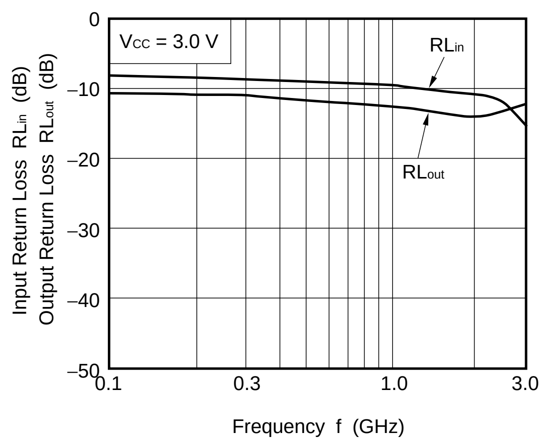
POWER GAIN vs. FREQUENCY



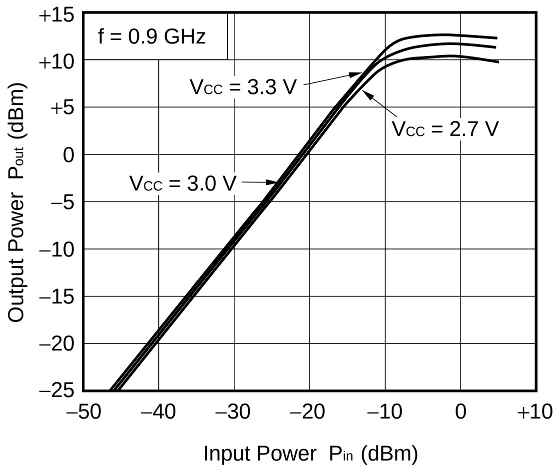
ISOLATION vs. FREQUENCY



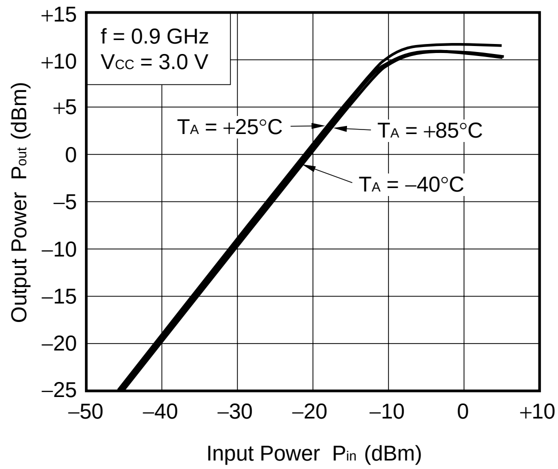
INPUT RETURN LOSS, OUTPUT RETURN LOSS vs. FREQUENCY



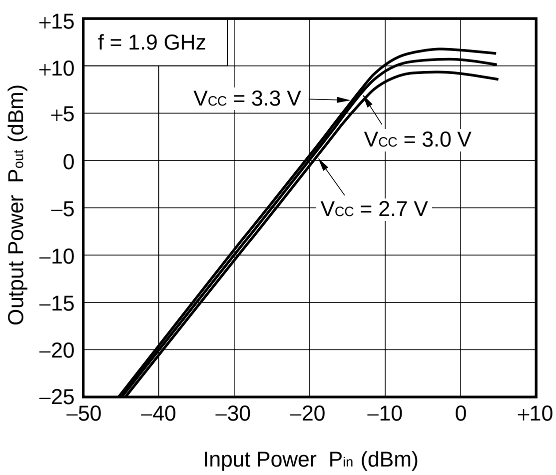
OUTPUT POWER vs. INPUT POWER



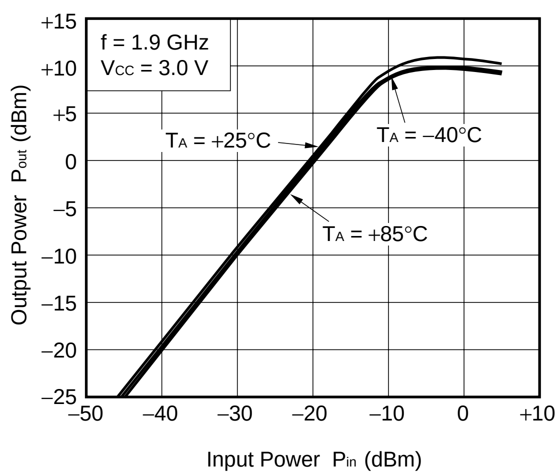
OUTPUT POWER vs. INPUT POWER



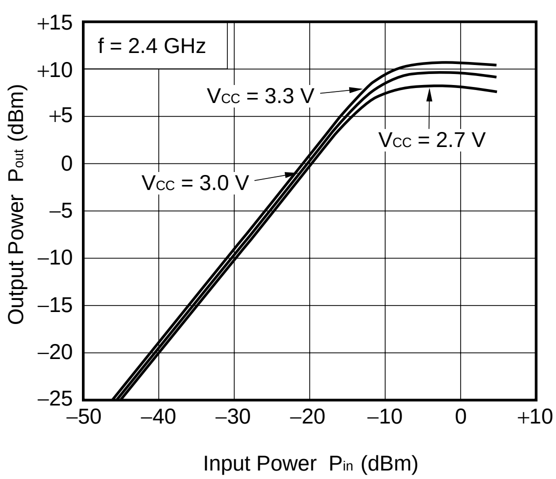
OUTPUT POWER vs. INPUT POWER



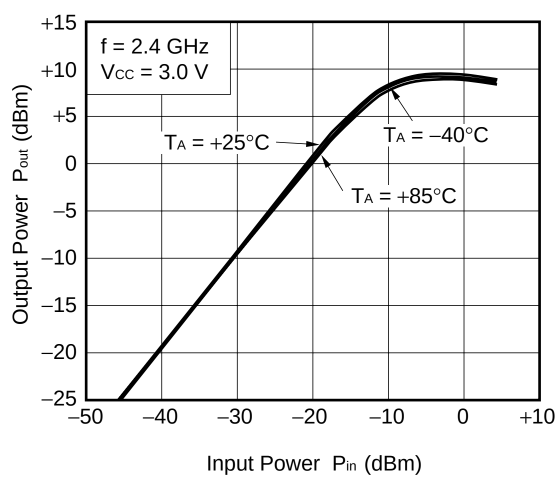
OUTPUT POWER vs. INPUT POWER



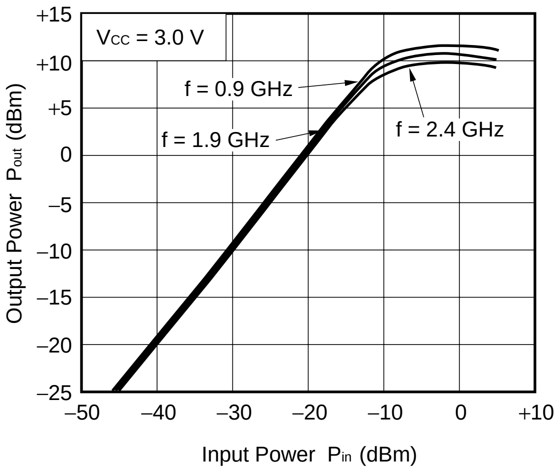
OUTPUT POWER vs. INPUT POWER



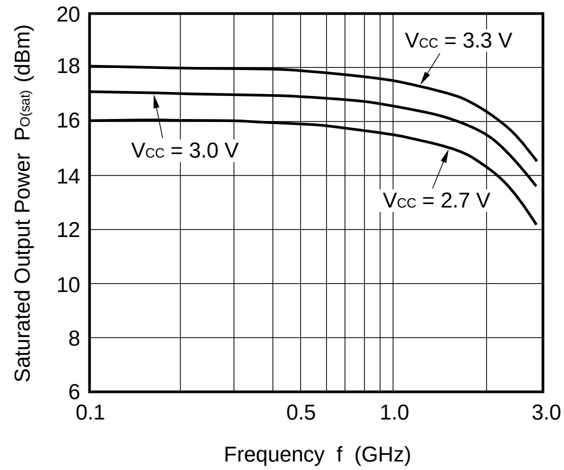
OUTPUT POWER vs. INPUT POWER



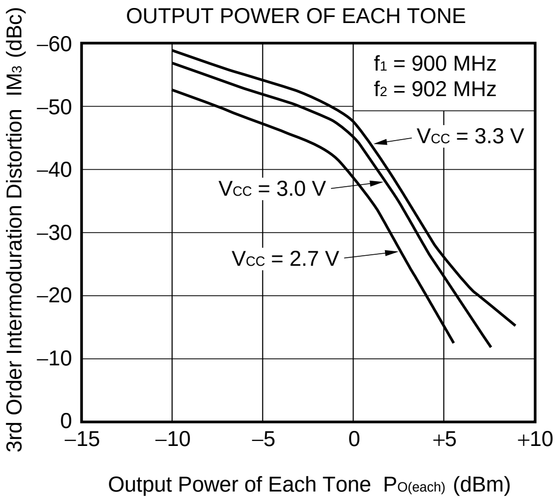
OUTPUT POWER vs. INPUT POWER



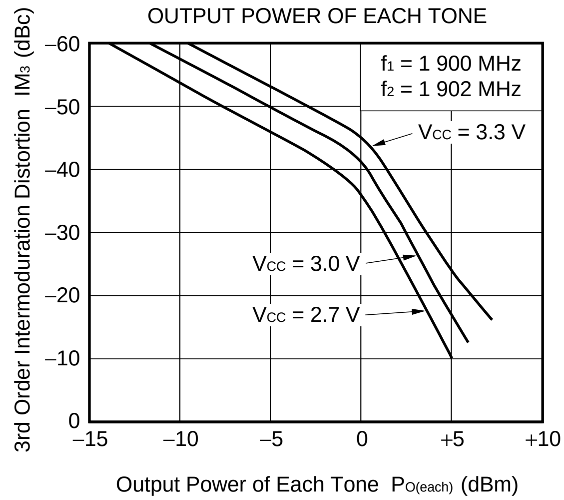
SATURATED OUTPUT POWER vs. FREQUENCY



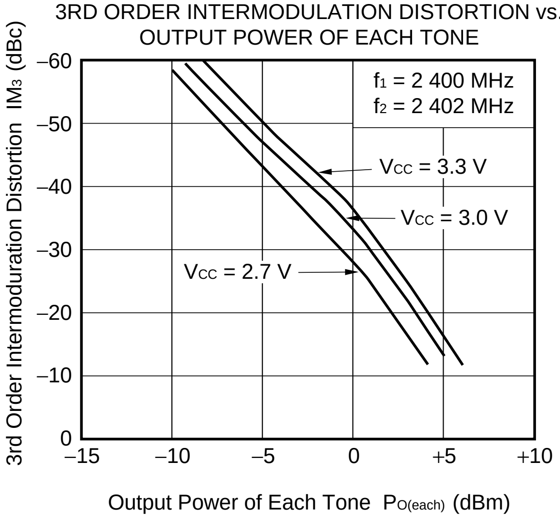
3RD ORDER INTERMODULATION DISTORTION vs. OUTPUT POWER OF EACH TONE



3RD ORDER INTERMODULATION DISTORTION vs. OUTPUT POWER OF EACH TONE



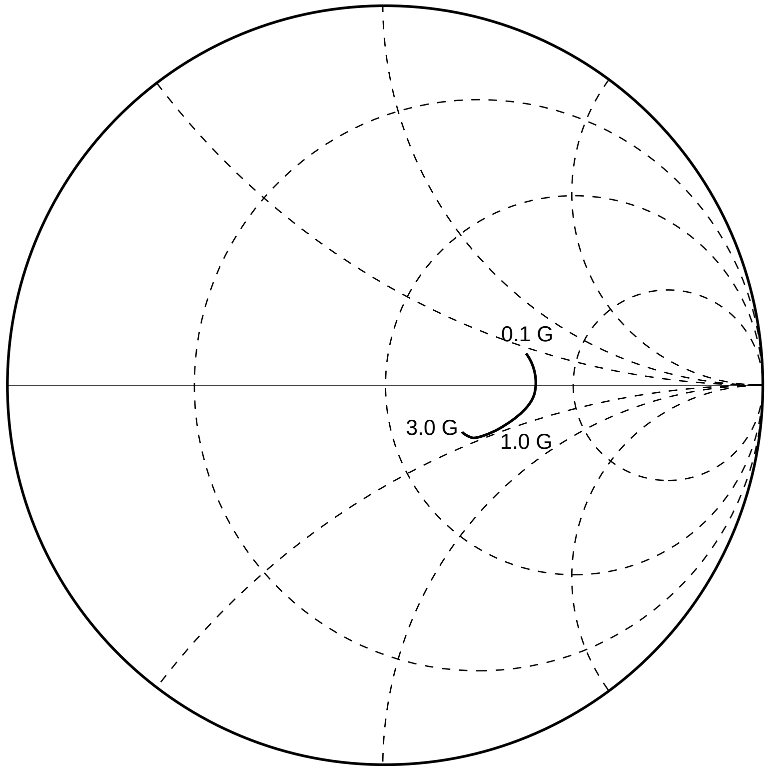
3RD ORDER INTERMODULATION DISTORTION vs. OUTPUT POWER OF EACH TONE



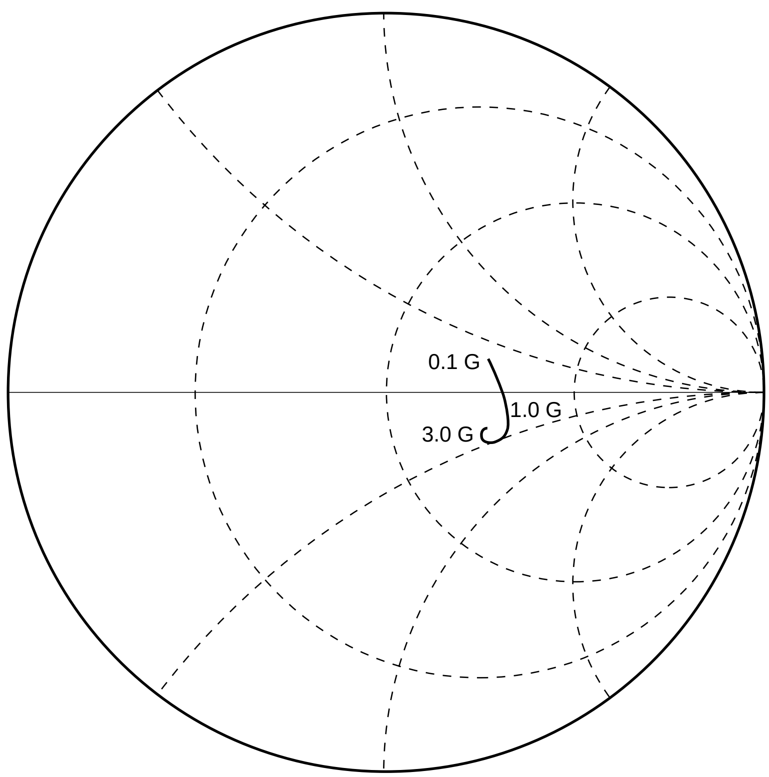
Remark The graphs indicate nominal characteristics.

★ S-PARAMETERS (V_{CC} = V_{out} = 3.0 V)

S_{11}-FREQUENCY



S_{22}-FREQUENCY



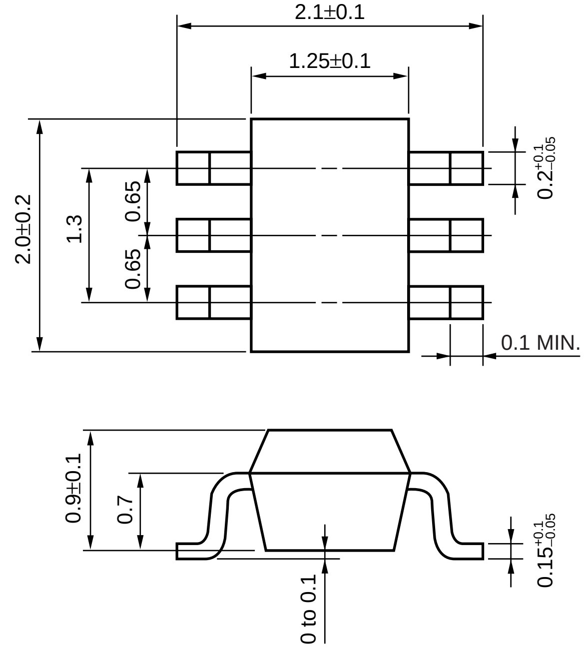
★ TYPICAL S-PARAMETER VALUES (T_A = +25°C)

V_{CC} = V_{out} = 3.0 V, I_{CC} = 30 mA

FREQUENCY	S11		S21		S12		S22		K
MHz	MAG.	ANG.	MAG.	ANG.	MAG.	ANG.	MAG.	ANG.	
100.0000	0.391	–2.6	12.933	–4.4	0.016	1.8	0.293	–2.7	1.84
200.0000	0.391	–6.2	12.999	–8.0	0.017	3.5	0.287	–5.1	1.80
300.0000	0.387	–10.2	13.174	–11.8	0.016	7.6	0.282	–6.8	1.86
400.0000	0.382	–13.8	13.322	–16.4	0.016	9.2	0.279	–8.4	1.82
500.0000	0.371	–16.7	13.391	–20.7	0.017	13.2	0.276	–9.1	1.79
600.0000	0.365	–19.5	13.407	–25.7	0.017	15.9	0.279	–10.0	1.78
700.0000	0.354	–21.6	13.549	–30.4	0.018	21.0	0.278	–11.0	1.73
800.0000	0.347	–23.7	13.475	–35.3	0.020	22.3	0.285	–11.7	1.57
900.0000	0.343	–25.8	13.426	–40.1	0.020	21.2	0.290	–13.5	1.52
1000.0000	0.334	–28.1	13.474	–44.9	0.019	27.0	0.293	–15.1	1.62
1100.0000	0.330	–30.8	13.386	–50.0	0.018	28.1	0.296	–17.6	1.69
1200.0000	0.324	–32.1	13.185	–54.6	0.020	27.6	0.302	–20.3	1.61
1300.0000	0.317	–34.2	13.121	–59.4	0.020	31.7	0.303	–21.9	1.62
1400.0000	0.318	–35.7	13.151	–64.2	0.021	32.1	0.309	–24.6	1.51
1500.0000	0.313	–38.0	12.866	–69.4	0.022	34.0	0.315	–27.1	1.47
1600.0000	0.309	–39.8	12.814	–73.9	0.023	34.6	0.318	–29.5	1.43
1700.0000	0.303	–42.5	12.508	–78.2	0.022	34.3	0.314	–33.1	1.52
1800.0000	0.302	–44.3	12.357	–83.2	0.024	35.9	0.319	–35.6	1.44
1900.0000	0.298	–45.5	12.090	–86.7	0.026	36.9	0.322	–37.6	1.39
2000.0000	0.290	–47.5	12.035	–90.9	0.025	40.0	0.313	–40.5	1.43
2100.0000	0.291	–50.1	11.984	–95.4	0.027	36.5	0.321	–43.5	1.36
2200.0000	0.283	–52.6	11.662	–99.9	0.026	38.2	0.314	–46.0	1.43
2300.0000	0.277	–54.1	11.711	–104.0	0.027	40.0	0.310	–48.6	1.41
2400.0000	0.274	–56.7	11.629	–108.6	0.028	38.4	0.309	–51.6	1.37
2500.0000	0.270	–58.0	11.475	–113.7	0.029	39.1	0.304	–54.1	1.35
2600.0000	0.261	–59.8	11.308	–118.5	0.029	39.9	0.297	–55.3	1.39
2700.0000	0.264	–61.4	11.198	–123.5	0.032	38.6	0.303	–56.5	1.29
2800.0000	0.253	–62.0	10.803	–129.4	0.031	42.8	0.295	–57.3	1.39
2900.0000	0.258	–63.9	10.670	–134.8	0.032	41.3	0.307	–57.9	1.33
3000.0000	0.255	–65.7	10.086	–139.5	0.033	40.9	0.316	–60.0	1.35
3100.0000	0.250	–67.9	9.683	–145.4	0.032	39.8	0.321	–63.1	1.44

★ PACKAGE DIMENSIONS

6-PIN SUPER MINIMOLD (UNIT: mm)



NOTES ON CORRECT USE

(1) Observe precautions for handling because of electro-static sensitive devices.

(2) Form a ground pattern as widely as possible to minimize ground impedance (to prevent undesired oscillation). All the ground pins must be connected together with wide ground pattern to decrease impedance difference.

(3) The bypass capacitor should be attached to the V_{CC} pin.

(4) The inductor must be attached between V_{CC} and output pins. The inductance value should be determined in accordance with desired frequency.

(5) The DC cut capacitor must be attached to input and output pin.

RECOMMENDED SOLDERING CONDITIONS

This product should be soldered under the following recommended conditions. For soldering methods and conditions other than those recommended below, contact your NEC sales representative.

Soldering Method	Soldering Conditions	Recommended Condition Symbol
Infrared Reflow	Package peak temperature: 235°C or below Time: 30 seconds or less (at 210°C) Count: 3, Exposure limit: None[Note]	IR35-00-3
VPS	Package peak temperature: 215°C or below Time: 40 seconds or less (at 200°C) Count: 3, Exposure limit: None[Note]	VP15-00-3
Wave Soldering	Soldering bath temperature: 260°C or below Time: 10 seconds or less Count: 1, Exposure limit: None[Note]	WS60-00-1
Partial Heating	Pin temperature: 300°C Time: 3 seconds or less (per side of device) Exposure limit: None[Note]	–

Note After opening the dry pack, keep it in a place below 25°C and 65% RH for the allowable storage period.

Caution Do not use different soldering methods together (except for partial heating).

For details of recommended soldering conditions for surface mounting, refer to information document **SEMICONDUCTOR DEVICE MOUNTING TECHNOLOGY MANUAL (C10535E)**.

ATTENTION

OBSERVE PRECAUTIONS
FOR HANDLING
ELECTROSTATIC
SENSITIVE
DEVICES