

# BIPOLAR ANALOG INTEGRATED CIRCUIT $\mu PC2749TB$

# **3 V, SUPER MINIMOLD SILICON MMIC AMPLIFIER FOR MOBILE COMMUNICATIONS**

## DESCRIPTION

NEC

The  $\mu$ PC2749TB is a silicon monolithic integrated circuit designed as amplifier for mobile communications. Due to wideband response at 2.9 GHz, this IC is recommendable for GPS receiver, wireless communication systems.

This IC is manufactured using NEC's 20 GHz f⊤ NESAT<sup>™</sup> III silicon bipolar process. This process uses silicon nitride passivation film and gold electrodes. These materials can protect chip surface from external pollution and prevent corrosion/migration. Thus, this IC has excellent performance, uniformity and reliability.

## ★ FEATURES

- Supply voltage
- Circuit current
- Noise figure
- Power gain
- Saturated output power

Upper limit operating frequency High-density surface mounting : lcc = 6.0 mA TYP. @Vcc = 3.0 V : NF = 4.0 dB TYP. @f = 1.9 GHz

: Vcc = 2.7 to 3.3 V

- : G<sub>P</sub> = 16.0 dB TYP. @f = 1.9 GHz
- :  $P_{O(sat)} = -6.0 \text{ dBm TYP}$ . @f = 1.9 GHz
- : fu = 2.9 GHz TYP. @3 dB down below from gain at f = 0.9 GHz
- : 6-pin super minimold package  $(2.0 \times 1.25 \times 0.9 \text{ mm})$

## **APPLICATIONS**

- GPS receiver
- Wireless LAN

#### **ORDERING INFORMATION**

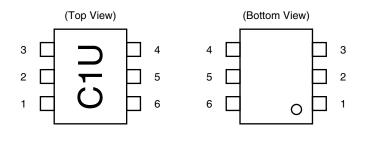
Part Number	Package	Marking	Supplying Form
μPC2749TB-E3	6-pin super minimold	C1U	<ul> <li>Embossed tape 8 mm wide</li> <li>1, 2, 3 pins face the perforation side of the tape</li> <li>Qty 3 kpcs/reel</li> </ul>

**Remark**To order evaluation samples, please contact your local NEC sales office.Part number for sample order:  $\mu$ PC2749TB

#### Caution Electro-static sensitive devices

The information in this document is subject to change without notice. Before using this document, please confirm that this is the latest version. Not all devices/types available in every country. Please check with local NEC representative for availability and additional information.

## **PIN CONNECTIONS**



Pin No.	Pin Name
1	INPUT
2	GND
3	GND
4	OUTPUT
5	GND
6	Vcc

## \* PRODUCT LINE-UP (TA = $+25^{\circ}$ C, V cc = 3.0 V, Zs = ZL = 50 $\Omega$ )

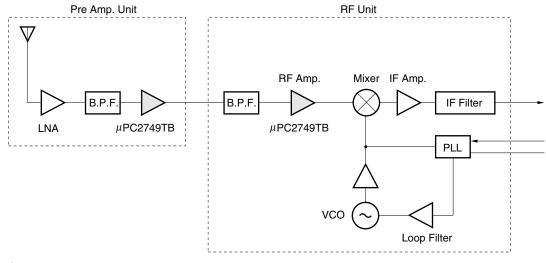
Part No.	f <sub>u</sub> (GHz)	P <sub>O(sat)</sub> (dBm)	G₽ (dB)	NF (dB)	lcc (mA)	Package	Marking
μPC2749T	2.9	-6.0	16	4.0	6.0	6-pin minimold	C1U
μPC2749TB						6-pin super minimold	
μPC2745T	2.7	-1.0	12	6.0	7.5	6-pin minimold	C1Q
μPC2745TB						6-pin super minimold	
μPC2746T	1.5	0	19	4.0	7.5	6-pin minimold	C1R
μPC2746TB						6-pin super minimold	
μPC2747T	1.8	-7.0	12	3.3	5.0	6-pin minimold	C1S
μPC2747TB						6-pin super minimold	
μPC2748T	0.2 to 1.5	-3.5	19	2.8	6.0	6-pin minimold	C1T
μPC2748TB						6-pin super minimold	

Remark Typical performance. Please refer to ELECTRICAL CHARACTERISTICS in detail.

Caution The package size distinguishes between minimold and super minimold.

#### SYSTEM APPLICATION EXAMPLE

#### **EXAMPLE OF GPS RECEIVER**



 $\triangleright$  :  $\mu$ PC2749TB applicable

## PIN EXPLANATION

Pin No.	Pin Name	Applied Voltage (V)	Pin Voltage (V) <sup>Note</sup>	Function and Applications	Internal Equivalent Circuit
1	INPUT	_	0.82	Signal input pin. A internal matching circuit, configured with resistors, enables 50 $\Omega$ connection over a wide band. This pin must be coupled to signal source with capacitor for DC cut.	
2 3 5	GND	0	-	Ground pin. This pin should be connected to system ground with minimum inductance. Ground pattern on the board should be formed as wide as possible. All the ground pins must be connected together with wide ground pattern to decrease impedance difference.	
4	OUTPUT	-	2.87	Signal output pin. A internal matching circuit, configured with resistors, enables 50 $\Omega$ connection over a wide band. This pin must be coupled to next stage with capacitor for DC cut.	3 2-5
6	Vcc	2.7 to 3.3	-	Power supply pin. This pin should be externally equipped with bypass capacity to minimize ground impedance.	

**Note** Pin voltage is measured at Vcc = 3.0 V.

 $\star$ 

### ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Conditions	Ratings	Unit
Supply Voltage	Vcc	$T_A = +25^{\circ}C$	4.0	V
Circuit Current	lcc	$T_A = +25^{\circ}C$	15	mA
Power Dissipation	PD	Mounted on double-sided copper clad $50 \times 50 \times 1.6$ mm epoxy glass PWB, $T_A = +85^{\circ}C$	270	mW
Operating Ambient Temperature	TA		–40 to +85	°C
Storage Temperature	Tstg		–55 to +150	°C
Input Power	Pin	$T_A = +25^{\circ}C$	0	dBm

#### **RECOMMENDED OPERATING RANGE**

Parameter	Symbol	MIN.	TYP.	MAX.	Unit
Supply Voltage	Vcc	2.7	3.0	3.3	V

#### **ELECTRICAL CHARACTERISTICS**

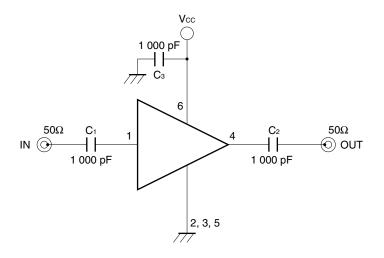
# (Unless otherwise specified, TA = +25 °C, V cc = 3.0 V, Zs = ZL = 50 $\Omega$ )

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
Circuit Current	Icc	No Signal	4.0	6.0	8.0	mA
Power Gain	G₽	f = 1.9 GHz	13.0	16.0	18.5	dB
Saturated Output Power	Po(sat)	f = 1.9 GHz, P <sub>in</sub> = -6 dBm	-9.0	-6.0	_	dBm
Noise Figure	NF	f = 1.9 GHz	-	4.0	5.5	dB
Upper Limit Operating Frequency	fu	3 dB down below flat gain at f = 0.9 GHz	2.5	2.9	-	GHz
Isolation	ISL	f = 1.9 GHz	25	30	_	dB
Input Return Loss	RLin	f = 1.9 GHz	7	10	-	dB
Output Return Loss	RLout	f = 1.9 GHz	9.5	12.5	-	dB

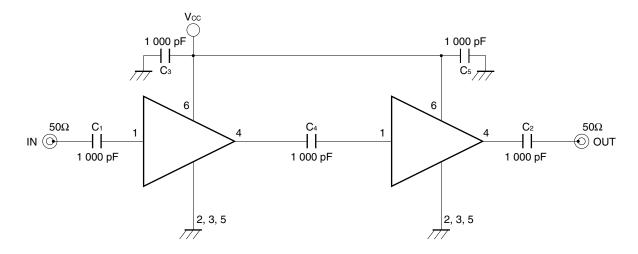
## STANDARD CHARACTERISTICS FOR REFERENCE (TA = +25 °C, V cc = 3.0 V, Zs = ZL = 50 $\Omega$ )

Parameter	Symbol	Test Conditions	Reference Value	Unit
Power Gain	G₽	f = 0.9 GHz	14.5	dB
Noise Figure	NF	f = 0.9 GHz	3.2	dB
3rd Order Intermodulation Distortion	IМз	$P_{O(each)} = -20 \text{ dBm}$ f <sub>1</sub> = 1.900 GHz, f <sub>2</sub> = 1.902 GHz	-33	dBc
Gain 1 dB Compression Output Power	Po(1 dB)	f = 1.9 GHz	-12.5	dBm

#### **TEST CIRCUIT**



#### EXAMPLE OF APPLICATION CIRCUIT



The application circuits and their parameters are for reference only and are not intended for use in actual design-ins.

## CAPACITORS FOR THE Vcc, INPUT AND OUTPUT PINS

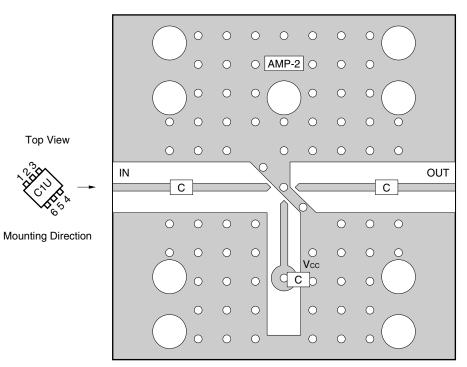
1 000 pF capacitors are recommendable as bypass capacitor for  $V_{CC}$  pin and coupling capacitors for input/output pins.

Bypass capacitor for Vcc pin is intended to minimize Vcc pin's ground impedance. Therefore, stable bias can be supplied against Vcc fluctuation.

Coupling capacitors for input/output pins are intended to minimize RF serial impedance and cut DC.

To get a flat gain from 100 MHz up, 1 000 pF capacitors are assembled on the test circuit. [Actually, 1 000 pF capacitors give flat gain at least 10 MHz. In the case of under 10 MHz operation, increase the value of coupling capacitor such as 2 200 pF. Because the coupling capacitors are determined by the equation of  $C = 1/(2 \pi fZs)$ .]

## ILLUSTRATION OF THE TEST CIRCUIT ASSEMBLED ON EVALUATION BOARD



#### **COMPONENT LIST**

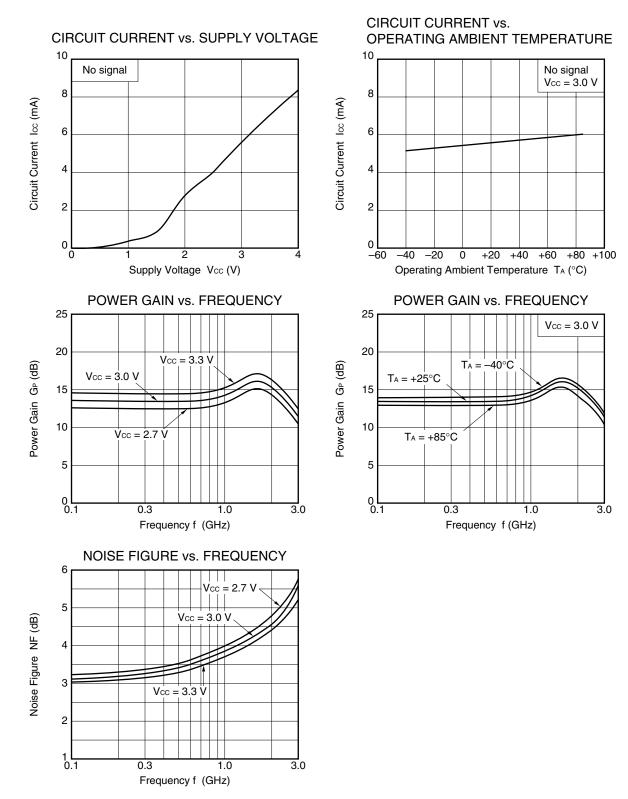
	Value
С	1 000 pF

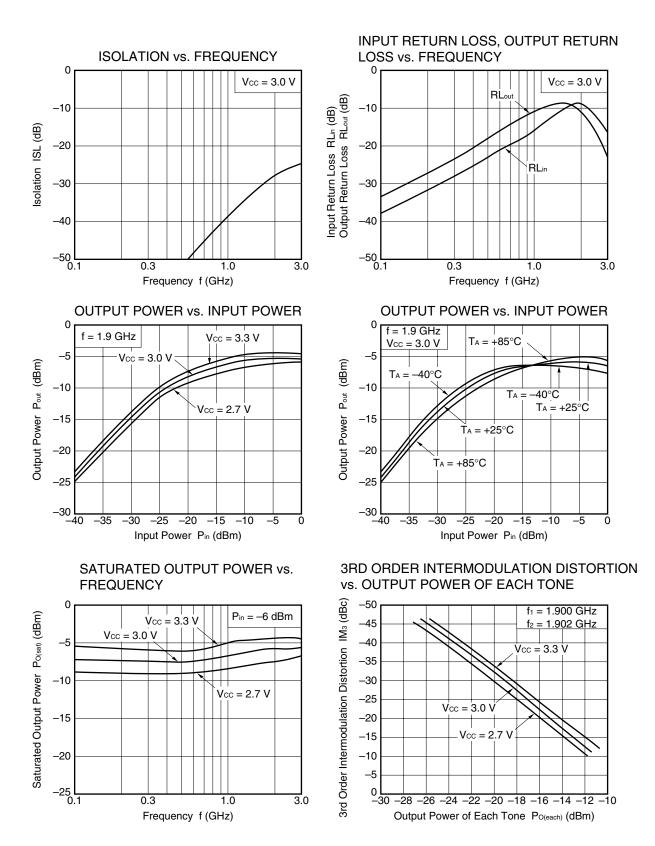
#### Notes

- 1.  $30 \times 30 \times 0.4$  mm double-sided copper clad polyimide board.
- 2. Back side: GND pattern
- 3. Solder plated on pattern
- **4.**  $\circ$   $\bigcirc$  : Through holes

For more information on the use of this IC, refer to the following application note: USAGE AND APPLICATIONS OF 6-PIN MINI-MOLD, 6-PIN SUPER MINI-MOLD SILICON HIGH-FREQUENCY WIDEBAND AMPLIFIER MMIC (P11976E).

## TYPICAL CHARACTERISTICS (Unless otherwise specified, $T_A = +25^{\circ}C$ )

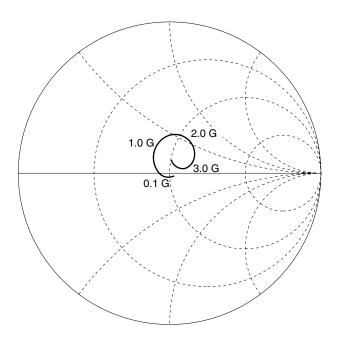




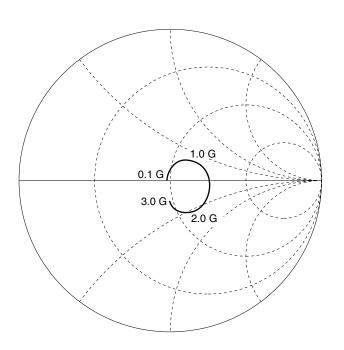
**Remark** The graphs indicate nominal characteristics.

S-PARAMETERS (T<sub>A</sub> =  $+25^{\circ}$ C, Vcc = 3.0 V)

#### S11-FREQUENCY



S22-FREQUENCY



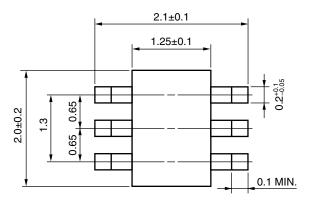
## TYPICAL S-PARAMETER VALUES (T<sub>A</sub> = $+25^{\circ}$ C)

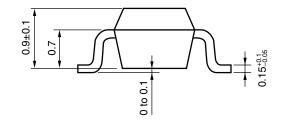
Vcc = 3.0 V, Icc = 6.5 mA

FREQUENCY	5	S11	5	<b>S</b> 21	S	12	S	22	к
MHz	MAG.	ANG.	MAG.	ANG.	MAG.	ANG.	MAG.	ANG.	
100 0000	0.001	12.0	4.000	1.0	0.000		0.004	165.0	66.90
100.0000	0.021	13.0	4.096	-1.9	0.002	-1.1	0.024	165.8	66.82
200.0000	0.038	-30.5	4.216	-7.8	0.001	75.4	0.033	113.6	129.26
300.0000	0.034	-71.8	4.282	-15.5	0.001	141.5	0.064	96.1	90.16
400.0000	0.052	-120.5	4.403	-21.0	0.002	129.9	0.080	87.9	45.30
500.0000	0.062	-149.9	4.390	-26.6	0.002	134.1	0.103	76.9	57.58
600.0000	0.079	-169.7	4.399	-31.6	0.003	128.3	0.127	68.6	34.08
700.0000	0.097	173.6	4.566	-36.7	0.005	132.9	0.151	60.6	22.08
800.0000	0.116	160.5	4.667	-41.3	0.007	131.5	0.174	53.7	14.70
900.0000	0.134	149.3	4.843	-46.8	0.008	129.3	0.197	44.9	12.29
1000.0000	0.156	138.8	5.016	-52.6	0.009	124.6	0.220	36.1	10.00
1100.0000	0.178	128.5	5.305	-60.3	0.014	131.4	0.240	28.0	6.15
1200.0000	0.195	118.7	5.660	-67.1	0.016	122.5	0.262	17.3	5.13
1300.0000	0.214	108.7	5.835	-76.2	0.020	118.6	0.279	8.6	3.80
1400.0000	0.229	99.5	6.148	-84.5	0.022	114.4	0.287	-2.0	3.23
1500.0000	0.249	89.4	6.364	-93.8	0.025	107.7	0.294	-13.5	2.72
1600.0000	0.259	79.9	6.611	-103.6	0.028	104.3	0.294	-23.6	2.35
1700.0000	0.264	69.8	6.577	-113.5	0.032	96.8	0.283	-33.8	2.09
1800.0000	0.259	60.3	6.549	-123.4	0.034	91.8	0.272	-44.1	1.99
1900.0000	0.248	50.9	6.407	-132.9	0.036	83.3	0.256	-53.8	1.97
2000.0000	0.238	43.6	6.321	-140.8	0.037	78.5	0.234	-61.4	1.99
2100.0000	0.218	35.9	6.046	-148.8	0.038	75.1	0.213	-69.5	2.04
2200.0000	0.204	30.1	5.862	-156.5	0.039	70.4	0.193	-73.8	2.08
2300.0000	0.183	25.3	5.696	-163.2	0.040	68.3	0.174	-79.5	2.15
2400.0000	0.156	21.2	5.430	-170.5	0.041	60.7	0.164	-84.1	2.25
2500.0000	0.140	18.8	5.282	-176.3	0.042	61.6	0.152	-82.1	2.25
2600.0000	0.119	18.7	5.013	177.2	0.040	58.1	0.142	-84.5	2.53
2700.0000	0.095	21.2	4.849	170.9	0.042	55.1	0.146	-85.5	2.46
2800.0000	0.078	30.0	4.596	164.9	0.042	51.9	0.149	-83.9	2.62
2900.0000	0.066	44.5	4.446	158.1	0.042	44.7	0.154	-91.8	2.70
3000.0000	0.070	66.0	4.163	152.3	0.044	41.9	0.171	-92.8	2.73
3100.0000	0.082	78.1	3.966	145.3	0.042	37.1	0.181	-99.6	2.97
	0.00-		0.000			••••			

#### **\*** PACKAGE DIMENSIONS

## 6-PIN SUPER MINIMOLD (UNIT: mm)





#### NOTES ON CORRECT USE

- (1) Observe precautions for handling because of electro-static sensitive devices.
- (2) Form a ground pattern as widely as possible to minimize ground impedance (to prevent undesired oscillation).All the ground pins must be connected together with wide ground pattern to decrease impedance difference.
- (3) The bypass capacitor should be attached to Vcc line.
- (4) The DC cut capacitor must be attached to input and output pin.

#### **RECOMMENDED SOLDERING CONDITIONS**

This product should be soldered under the following recommended conditions. For soldering methods and conditions other than those recommended below, contact your NEC sales representative.

Soldering Method	Soldering Conditions	Recommended Condition Symbol
Infrared Reflow	Package peak temperature: 235℃ or below Time: 30 seconds or less (at 210℃) Count: 3, Exposure limit: None <sup>Note</sup>	IR35-00-3
VPS	Package peak temperature: 215°C or below Time: 40 seconds or less (at 200°C) Count: 3, Exposure limit: None <sup>Note</sup>	VP15-00-3
Wave Soldering	Soldering bath temperature: 260°C or below Time: 10 seconds or less Count: 1, Exposure limit: None <sup>Note</sup>	WS60-00-1
Partial Heating	Pin temperature: 300°C or below Time: 3 seconds or less (per side of device) Exposure limit: None <sup>Note</sup>	_

Note After opening the dry pack, keep it in a place below 25°C and 65% RH for the allowable storage period.

#### Caution Do not use different soldering methods together (except for partial heating).

For details of recommended soldering conditions for surface mounting, refer to information document **SEMICONDUCTOR DEVICE MOUNTING TECHNOLOGY MANUAL (C10535E)**.

[MEMO]

[MEMO]



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