



BIPOLAR ANALOG INTEGRATED CIRCUIT $\mu PC1678GV$

5 V-BIAS, +17.5 dBm OUTPUT, 2.0 GHz WIDEBAND Si MMIC AMPLIFIER

★ DESCRIPTION

The μ PC1678GV is a silicon monolithic integrated circuit designed as medium output power amplifier for high frequency system applications. Due to +17.5 dBm TYP. output at 2 GHz, this IC is recommendable for transmitter stage amplifier of L BAND wireless communication systems.

The μ PC1678GV has shrink package and compatible pin connections and supply voltage to μ PC1678G. So, in the case of decreasing your system size, μ PC1678GV is suitable to replace from μ PC1678G.

This IC is manufactured using NEC's 20 GHz f⊤ NESAT[™]IV silicon bipolar process. This process uses silicon nitride passivation film and gold electrodes. These materials can protect chip surface from external pollution and prevent corrosion/migration. Thus, this IC has excellent performance, uniformity and reliability.

FEATURES

•	Supply voltage	:	Vcc = 4.5 to 5.5 V
•	Saturated output power	:	$P_{O(sat)}$ = +17.5 dBm TYP. @ f = 500 MHz with external inductor
•	Wideband response	:	f_{u} = 2.0 GHz TYP. @ 3 dB down below the gain at 0.1 GHz
•	Power gain	:	G _P = 23 dB TYP. @ f = 500 MHz
•	Isolation	:	ISL = 35 dB TYP. @ f = 500 MHz
•	High-density surface mounting	g :	8-pin plastic SSOP package ($3.0 \times 3.2 \times 1.8$ mm)

APPLICATIONS

· PA driver for high frequency system.

ORDERING INFORMATION

Part Number	Package	Marking	Supplying Form
μPC1678GV-E1	8 pin plastic SSOP	1678	Embossed tape 8 mm wide. Pin 1 is in tape pull-out direction. Qty 1 kp/reel.

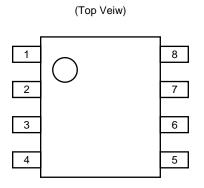
 $\label{eq:result} \textbf{Remark} \quad \mbox{To order evaluation samples, please contact your local NEC sales office.}$

(Part number for sample order: μ PC1678GV)

Caution Electro-static sensitive devices

The information in this document is subject to change without notice. Before using this document, please confirm that this is the latest version. Not all devices/types available in every country. Please check with local NEC representative for availability and additional information.

PIN CONNECTIONS



Pin No.	Pin Name		
1	INPUT		
2	GND		
3	GND		
4	GND		
5	OUTPUT		
6	GND		
7	GND		
8	Vcc		

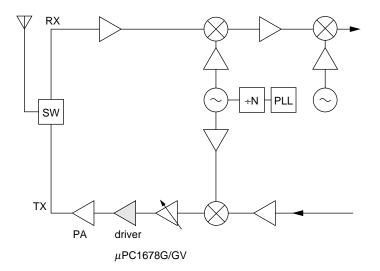
PRODUCT LINE-UP (TA = +25 °C, Vcc = Vout = 5.0 V, Zs = ZL = 50 Ω)

Part Number	fu (GHz)	Po(sat) (dBm)	G _P (dB)	NF (dB)	Icc (mA)	Package
μPC1678G	2.0	+17.5	23	6.0	49	8-pin plastic SOP
μPC1678GV	2.0	+17.5	23	6.0	49	8-pin plastic SSOP

Remark Typical performance. Please refer to ELECTRICAL CHARACTERISTICS in detail.

SYSTEM APPLICATION EXAMPLE

EXAMPLE OF PA driver in RF transmitter block



PIN EXPLANATION

Pin NO.	Pin Name	Applied Voltage (V)	Pin Voltage (V) ^{Note}	Functions and application	Internal equivalent circuit
1	INPUT	_	1.17	Signal input pin. A internal matching circuit, configured with resistors, enables 50Ω connection over a wide band. A multi-feedback circuit is designed to cancel the deviations of hFE and resistance. This pin must be coupled to signal sause with capacitor for DC cut.	
5	OUTPUT	Voltage as same as Vcc through external inductor		Signal output pin. This output is designed as open collector of derlington transistors. Connect an inductor between this pin and Vcc pin to supply current to the internal output transistors. The inductor should be selected as high frequency use and small DC resistance.	
8	Vcc	4.5 to 5.5		Power supply pin. This pin should be externally equipped with bypass capacitor to minimize ground impedance.	
6 7	GND	0		Ground pins of internal input stage. Form a ground pattern as wide as possible to minimize ground impedance.	2, 3, 4, 6 and 7 are shorted by a lead frame.
2 3 4	GND	0		Ground pins of internal output stage. All the ground pins including pin 6 and pin 7 must be connected together with wide ground pattern to decrease impedance difference.	

Note Pin voltage is measured at $Vcc = V_{out} = 5.0 V$.

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Conditions	Rating	Unit
Supply Voltage	Vcc	T _A = +25 °C, Pin 5 and 8	6	V
Input Power	Pin	T _A = +25 °C	+10	dBm
Power Dissipation	P⊳	Mounted on double sided copper clad $50 \times 50 \times 1.6$ mm epoxy glass PWB (T _A = +85 °C)	330	mW
Operating Ambient Temperature	Та		-45 to +85	°C
Storage Temperature	Tstg		–55 to +150	°C

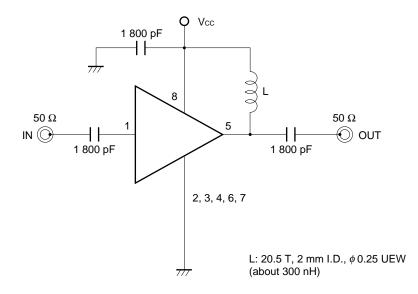
RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	MIN.	TYP.	MAX.	Unit	Notice
Supply Voltage	Vcc	4.5	5.0	5.5	V	The same voltage should be applied to pin 5 and 8.
Operating Ambient Temperature	TA	-45	+25	+85	°C	

ELECTRICAL CHARACTERISTICS (TA = + 25 °C, Vcc = Vout = 5.0 V, $Z_L = Z_S = 50 \Omega$)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Circuit Current	Icc	No signal	40	49	60	mA
Power Gain	GP	f = 500 MHz	21	23	25	dB
Noise Figure	NF	f = 500 MHz	_	6.0	8.0	dB
Upper Limit Operating Frequency	fu	3 dB down below from gain at f = 100 MHz	1.7	2.0	—	GHz
Isolation	ISL	f = 500 MHz	30	35	_	dB
Input Return Loss	RLin	f = 500 MHz	11	14	_	dB
Output Return Loss	RLout	f = 500 MHz	1	4	_	dB
Saturated Output Power Level	P _{O(sat)}	f = 500 MHz	+15.5	+17.5	—	dBm

TEST CIRCUIT



INDUCTOR FOR THE OUTPUT PIN

The internal output transistor of this IC consumes 30 mA, to output medium power. To supply current for output transistor, connect an inductor between the Vcc pin (pin 8) and output pin (pin 5).

The inductor has both DC and AC effects. In terms of DC, the inductor biases the output transistor with minimum voltage drop to output enable high level. In terms of AC, the inductor make output-port impedance higher to get enough gain. In this case, large inductance and Q is suitable.

CAPACITORS FOR THE Vcc, INPUT AND OUTPUT PINS

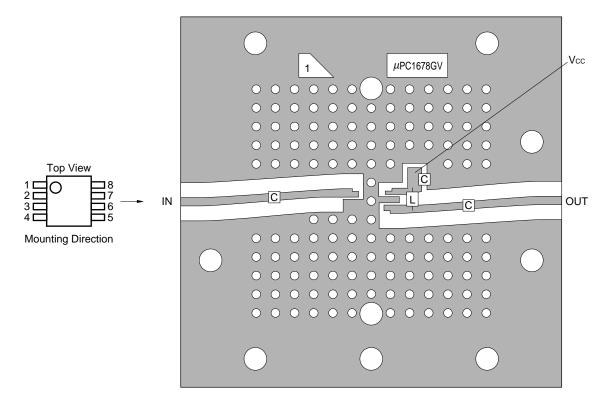
Capacitors of 1 800 pF are recommendable as the bypass capacitor for the Vcc pin and the coupling capacitors for the input and output pins.

The bypass capacitor connected to the Vcc pin is used to minimize ground impedance of Vcc pin. So, stable bias can be supplied against Vcc fluctuation.

The coupling capacitors, connected to the input and output pins, are used to cut the DC and minimize RF serial impedance. Their capacitance are therefore selected as lower impedance against a 50 Ω load. The capacitors thus perform as high pass filters, suppressing low frequencies to DC.

To obtain a flat gain from 100 MHz upwards, 1 800 pF capacitors are used in the test circuit. In the case of under 100 MHz operation, increase the value of coupling capacitor such as 10 000 pF. Because the coupling capacitors are determined by equation, $C = 1/(2 \pi R f c)$.

ILLUSTRATION OF THE TEST CIRCUIT ASSEMBLED ON EVALUATION BOARD



COMPONENT LIST

NEC

	Value
С	1 800 pF
L	300 nH

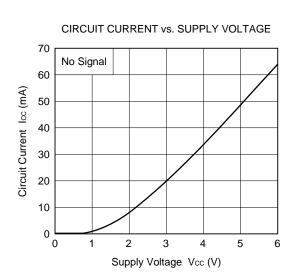
Notes

- 1. $50 \times 50 \times 0.4$ mm double sided copper clad polyimide board.
- 2. Back side: GND pattern
- 3. Solder plated on pattern
- 4. o O : Through holes

For more information on the use of this IC, refer to the following application note: USAGE AND APPLICATION OF SILICON MEDIUM-POWER HIGH-FREQUENCY AMPLIFIER MMIC (P12152E).

NEC

TYPICAL CHARACTERISTICS (Unless otherwise specified, $T_A = +25$ °C)



NOISE FIGURE, INSERTION POWER GAIN

Vcc = 5.0 V

√cc = 5.0 V

Vcc = 4.5 V

0.3

Vcc = 5.5 V

′4.5 V

Vcc = 5.5 V

1.0

3.0

Vcc

vs. FREQUENCY

G

NF

0.03

35

30

25

20

15

10

5

0 └ 0.01

(dB)

ġ

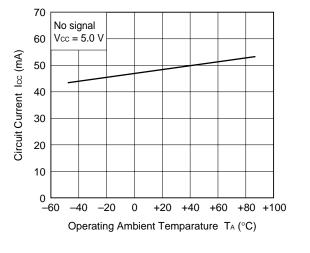
Gain

Insertion Power

9

Noise Figure NF (dB) c 9 2 8

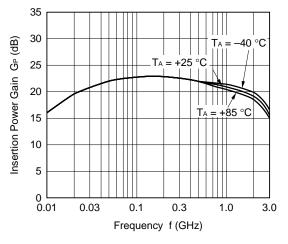
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OPERATING AMBIENT TEMPERATURE

CIRCUIT CURRENT vs.

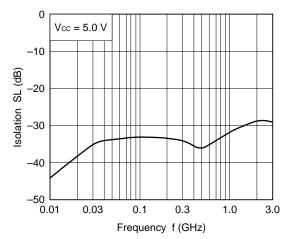
INSERTION POWER GAIN vs. FREQUENCY



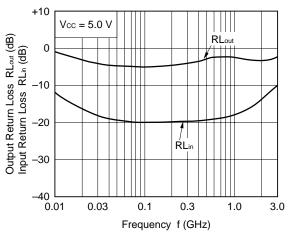
ISOLATION vs. FREQUENCY

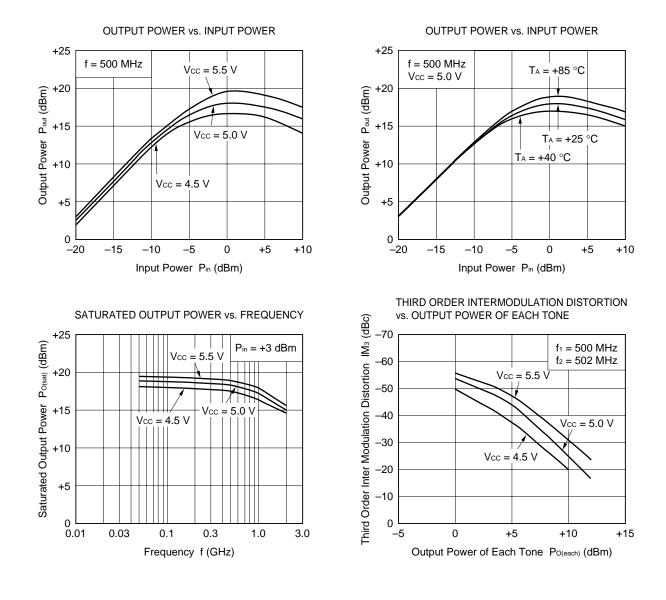
Frequency f (GHz)

0.1



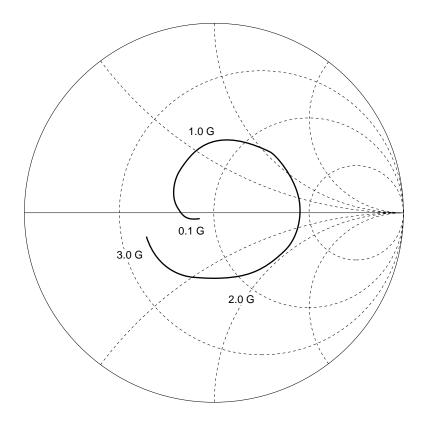
INPUT RETURN LOSS, OUTPUT RETURN LOSS vs. FREQUENCY



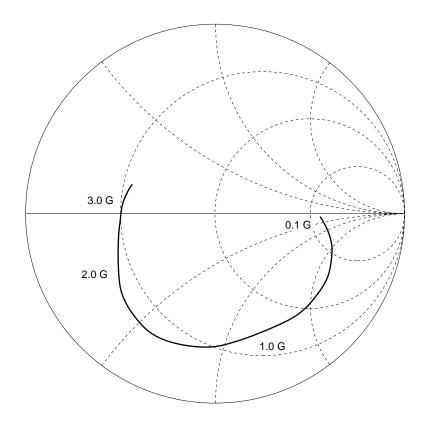


★ S-PARAMETER (T_A = +25 °C, V_CC = V_{out} = 5.0 V)

S11-FREQUENCY



S22-FREQUENCY



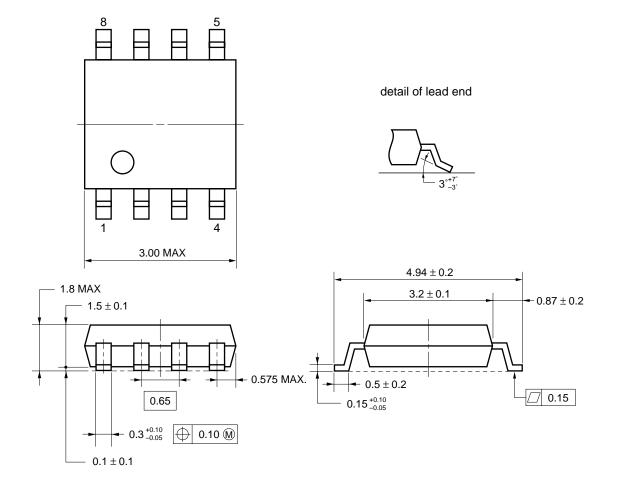
★ TYPICAL S-PARAMETER VALUES (T_A = +25 °C)

 $Vcc = V_{out} = 5.0 V Icc = 44 mA$

FREQUENCY	S	511	S	21	S	12	S	22	к
MHz	MAG.	ANG.	MAG.	ANG.	MAG.	ANG.	MAG.	ANG.	
100.0000	0.085	-163.8	12.206	-2.6	0.024	-5.0	0.558	-2.3	1.36
200.0000	0.118	-163.3	12.842	-6.0	0.020	-8.1	0.594	-6.6	1.43
300.0000	0.158	-170.9	13.766	-10.9	0.015	-2.4	0.637	-13.6	1.61
400.0000	0.184	176.0	14.731	-17.7	0.016	11.1	0.667	-21.3	1.39
500.0000	0.214	164.8	15.815	-25.1	0.014	26.3	0.692	-30.8	1.34
600.0000	0.243	152.4	16.598	-33.9	0.015	44.5	0.703	-40.2	1.13
700.0000	0.266	138.9	17.541	-43.2	0.019	51.4	0.701	-49.0	0.85
800.0000	0.293	125.2	18.057	-52.3	0.024	56.5	0.689	-57.0	0.69
900.0000	0.312	113.7	18.475	-62.2	0.027	58.1	0.670	-65.7	0.62
1000.0000	0.379	95.6	20.083	-71.9	0.031	61.7	0.686	-68.6	0.47
1100.0000	0.381	82.2	20.090	-82.8	0.035	58.6	0.685	-77.5	0.45
1200.0000	0.401	66.5	20.620	-94.0	0.038	56.0	0.688	-84.9	0.42
1300.0000	0.422	51.1	20.669	-106.8	0.042	55.1	0.702	-92.8	0.38
1400.0000	0.446	34.0	20.473	-119.6	0.046	52.6	0.713	-100.5	0.36
1500.0000	0.455	16.6	19.765	-132.5	0.048	48.4	0.717	-110.4	0.35
1600.0000	0.465	-0.5	18.759	-145.7	0.050	47.0	0.711	-119.0	0.36
1700.0000	0.444	-16.7	17.137	-157.7	0.049	44.9	0.684	-128.7	0.42
1800.0000	0.431	-33.5	15.512	-168.9	0.050	42.9	0.659	-137.4	0.48
1900.0000	0.397	-47.2	13.846	-178.7	0.048	43.5	0.616	-145.1	0.59
2000.0000	0.378	-59.2	12.398	172.4	0.048	45.8	0.574	-151.4	0.70
2100.0000	0.357	-70.5	11.060	164.9	0.048	45.3	0.540	-157.0	0.81
2200.0000	0.343	-80.7	9.918	157.8	0.048	47.4	0.510	-161.5	0.91
2300.0000	0.339	-89.4	8.927	151.7	0.049	47.4	0.489	-164.8	1.00
2400.0000	0.335	-98.9	8.107	146.2	0.051	46.1	0.483	-167.6	1.06
2500.0000	0.338	-107.2	7.388	140.6	0.050	46.2	0.475	-171.7	1.15
2600.0000	0.358	-115.5	6.772	135.4	0.055	46.8	0.475	-173.8	1.16
2700.0000	0.359	-125.3	6.267	131.0	0.051	48.1	0.463	-178.1	1.32
2800.0000	0.368	-133.9	5.807	125.4	0.054	49.4	0.482	179.5	1.33
2900.0000	0.372	-143.4	5.450	121.3	0.051	49.6	0.489	173.4	1.45
3000.0000	0.375	-152.7	5.018	116.0	0.050	53.6	0.475	166.3	1.62
3100.0000	0.372	-161.4	4.684	110.5	0.053	57.5	0.453	161.4	1.66

★ PACKAGE DIMENSIONS

8 PIN PLASTIC SSOP (UNIT : mm)



NOTE Each lead centerline is located within 0.10 mm of its true position (T.P.) at maximum material condition.

NOTE ON CORRECT USE

- (1) Observe precautions for handling because of electro-static sensitive devices.
- (2) Form a ground pattern as widely as possible to minimize ground impedance (to prevent undesired oscillation). All the ground pins must be connected together with wide ground pattern to decrease impedance difference.
- (3) The bypass capacitor should be attached to Vcc line.
- (4) The inductor must be attached between Vcc and output pins. The inductance value should be determined in accordance with desired frequency.
- (5) The DC cut capacitor must be each attached to the input and output pins.

RECOMMENDED SOLDERING CONDITIONS

This product should be soldered under the following recommended conditions. For soldering methods and conditions other than those recommended below, contact your NEC sales representative.

Soldering Method	Soldering Conditions	Recommended Condition Symbol
Infrared Reflow	Package peak temperature: 235 °C or below Time: 30 seconds or less (at 210 °C) Count: 3, Exposure limit ^{Nore} : None	IR35-00-3
VPS	Package peak temperature: 215 °C or below Time: 40 seconds or less (at 200 °C) Count: 3, Exposure limit ^{Nee} : None	VP15-00-3
Wave Soldering	Soldering bath temperature: 260 °C or below Time: 10 seconds or less Count: 1, Exposure limit ^{Note} : None	WS60-00-1
Partial Heating	Pin temperature: 300 °C Time: 3 seconds or less (per side of device) Exposure limit ^{Note} : None	_

Note After opening the dry pack, keep it in a place below 25 °C and 65 % RH for the allowable storage period.

Caution Do not use different soldering methods together (except for partial heating).

For details of recommended soldering conditions for surface mounting, refer to information document **SEMICONDUCTOR DEVICE MOUNTING TECHNOLOGY MANUAL (C10535E)**.

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