

N-CHANNEL MOS FIELD EFFECT TRANSISTOR  
FOR SWITCHING

## DESCRIPTION

The  $\mu$ PA1840 is N-channel MOS FET device that features a low on-state resistance and excellent switching characteristics, and designed for high voltage applications such as DC/DC converter.

## ORDERING INFORMATION

PART NUMBER	PACKAGE
$\mu$ PA1840GR-9JG	Power TSSOP8

## FEATURES

- High voltage rating  $V_{DSS} = 200$  V
- Power TSSOP8 package (Single circuit)
- Gate voltage rating  $\pm 30$  V
- Low on-state resistance  
 $R_{DS(on)} = 0.5 \Omega$  MAX. ( $V_{GS} = 10$  V,  $I_D = 1.5$  A)
- Low input capacitance  
 $C_{iss} = 320$  pF TYP. ( $V_{DS} = 10$  V,  $V_{GS} = 0$  V)
- Built-in gate protection diode

ABSOLUTE MAXIMUM RATINGS ( $T_A = 25^\circ\text{C}$ )

Drain to Source Voltage ( $V_{GS} = 0$ V)	$V_{DSS}$	200	V
Gate to Source Voltage ( $V_{DS} = 0$ V)	$V_{GSS}$	$\pm 30$	V
Drain Current (DC) ( $T_C = 25^\circ\text{C}$ )	$I_{D(DC)}$	$\pm 2.2$	A
Drain Current (pulse) <sup>Note1</sup>	$I_{D(pulse)}$	$\pm 8.8$	A
Total Power Dissipation <sup>Note2</sup>	$P_T$	2.0	W
Channel Temperature	$T_{ch}$	150	$^\circ\text{C}$
Storage Temperature	$T_{stg}$	-55 to +150	$^\circ\text{C}$

**Notes 1.**  $PW \leq 10 \mu\text{s}$ , Duty Cycle  $\leq 1\%$

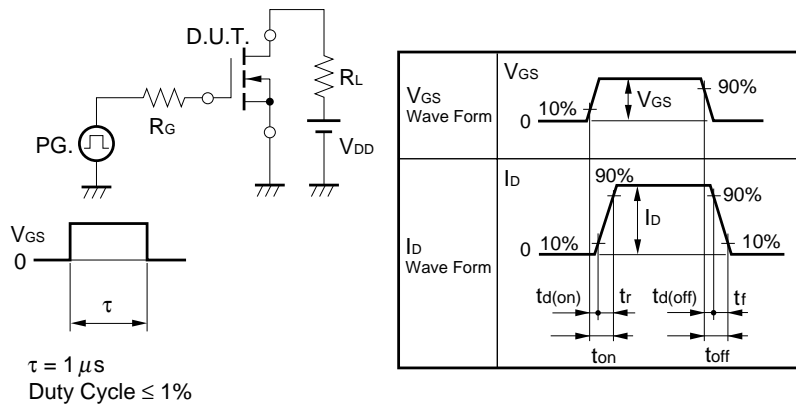
**2.** Mounted on ceramic substrate of  $5000\text{mm}^2 \times 1.1$

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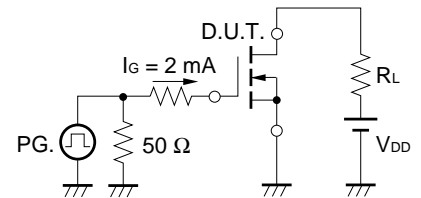
**ELECTRICAL CHARACTERISTICS (T<sub>A</sub> = 25°C)**

CHARACTERISTICS	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> = 200 V, V <sub>GS</sub> = 0 V			100	μA
Gate Leakage Current	I <sub>GSS</sub>	V <sub>GS</sub> = ±30 V, V <sub>DS</sub> = 0 V			±10	μA
Gate Cut-off Voltage	V <sub>GS(off)</sub>	V <sub>DS</sub> = 10 V, I <sub>D</sub> = 1 mA	2.5		4.5	V
Forward Transfer Admittance	y <sub>fs</sub>	V <sub>DS</sub> = 10 V, I <sub>D</sub> = 1.5 A	1.0	2.0		S
Drain to Source On-state Resistance	R <sub>DS(on)</sub>	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 1.5 A		0.37	0.5	Ω
Input Capacitance	C <sub>iss</sub>	V <sub>DS</sub> = 10 V		320		pF
Output Capacitance	C <sub>oss</sub>	V <sub>GS</sub> = 0 V		96		pF
Reverse Transfer Capacitance	C <sub>rss</sub>	f = 1 MHz		55		pF
Turn-on Delay Time	t <sub>d(on)</sub>	V <sub>DD</sub> = 100 V, I <sub>D</sub> = 1.5 A		14		ns
Rise Time	t <sub>r</sub>	V <sub>GS</sub> = 10 V		13		ns
Turn-off Delay Time	t <sub>d(off)</sub>	R <sub>G</sub> = 10 Ω		30		ns
Fall Time	t <sub>f</sub>			13		ns
Total Gate Charge	Q <sub>G</sub>	V <sub>DD</sub> = 160 V		16		nC
Gate to Source Charge	Q <sub>GS</sub>	V <sub>GS</sub> = 10 V		2.3		nC
Gate to Drain Charge	Q <sub>GD</sub>	I <sub>D</sub> = 2.2 A		9.0		nC
Body Diode Forward Voltage	V <sub>F(S-D)</sub>	I <sub>F</sub> = 2.2 A, V <sub>GS</sub> = 0 V		1.0		V
Reverse Recovery Time	t <sub>rr</sub>	I <sub>F</sub> = 2.2 A, V <sub>GS</sub> = 0 V		150		ns
Reverse Recovery Charge	Q <sub>rr</sub>	di/dt = 50 A/μs		0.4		μC

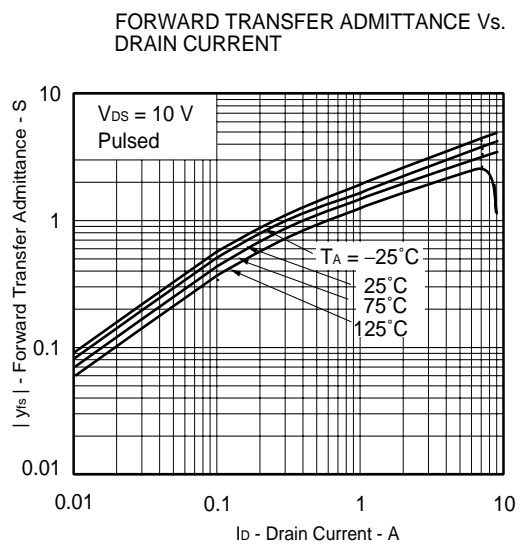
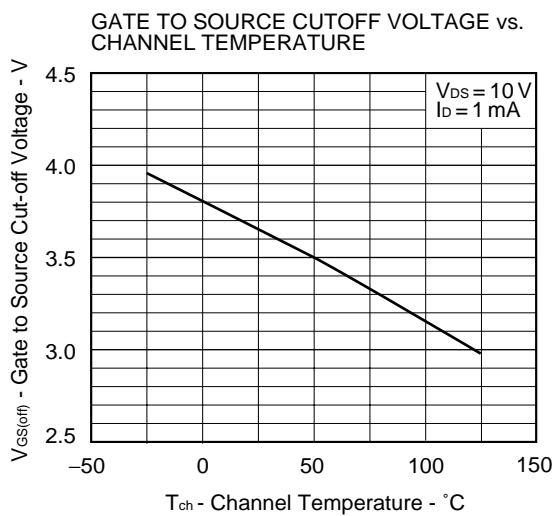
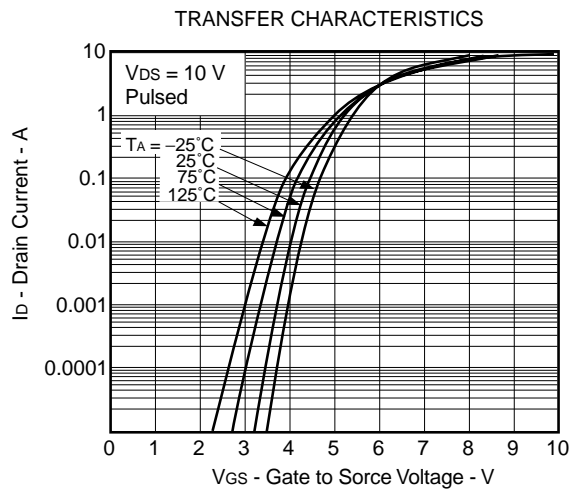
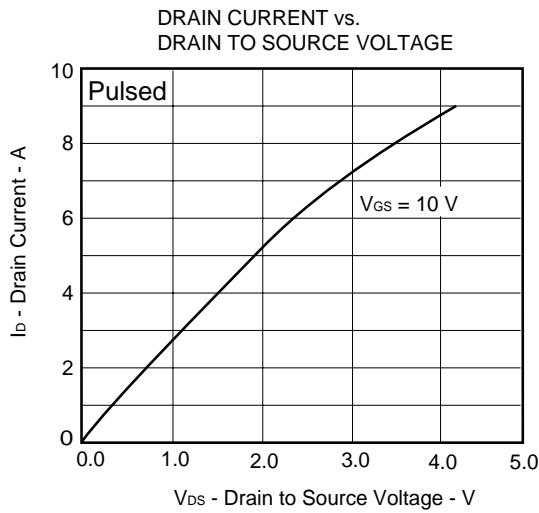
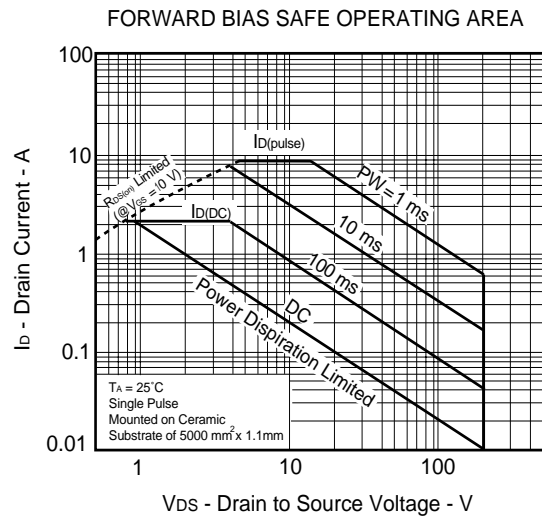
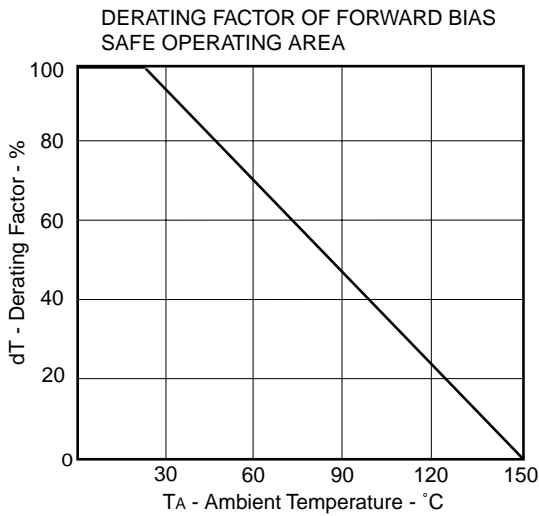
**TEST CIRCUIT 1 SWITCHING TIME**

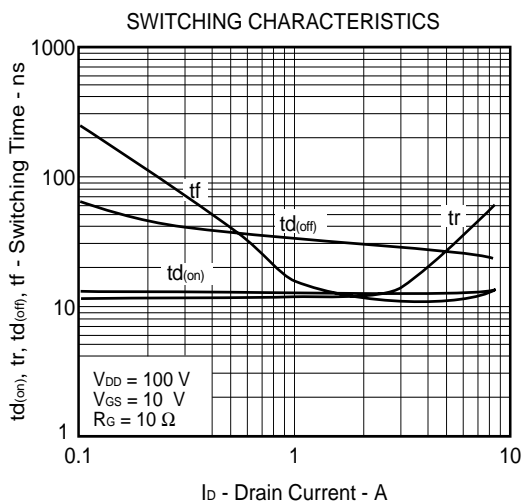
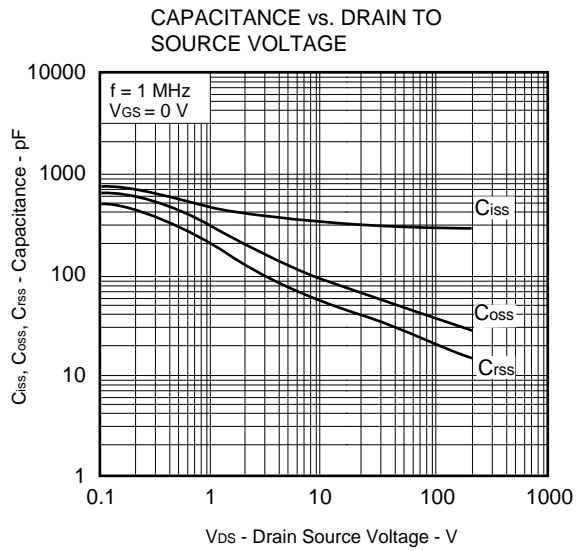
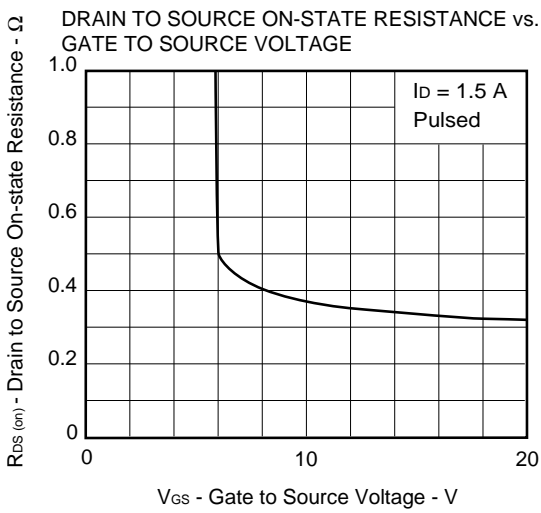
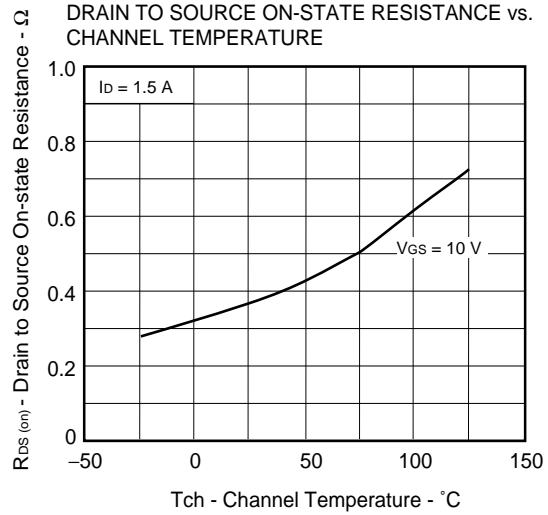
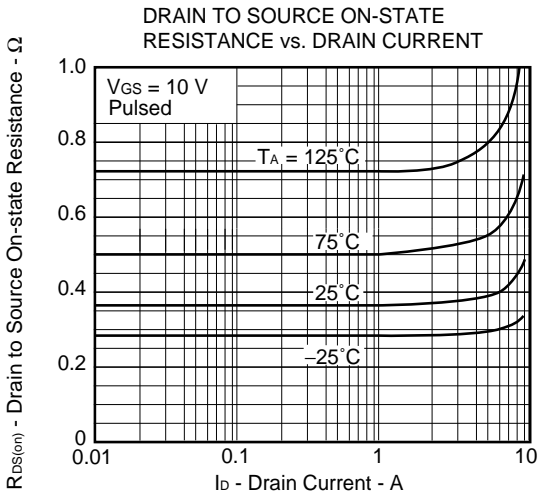


**TEST CIRCUIT 2 GATE CHARGE**

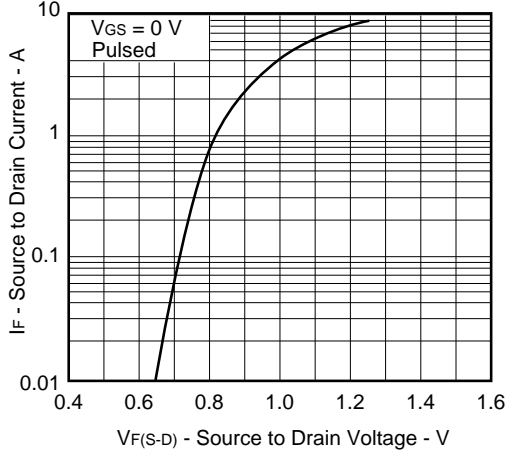


TYPICAL CHARACTERISTICS ( $T_A = 25^\circ\text{C}$ )

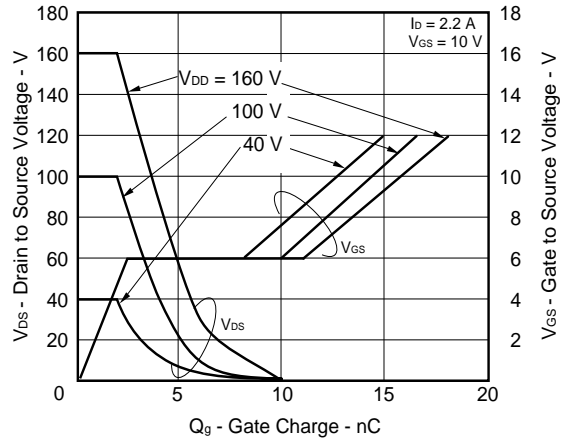




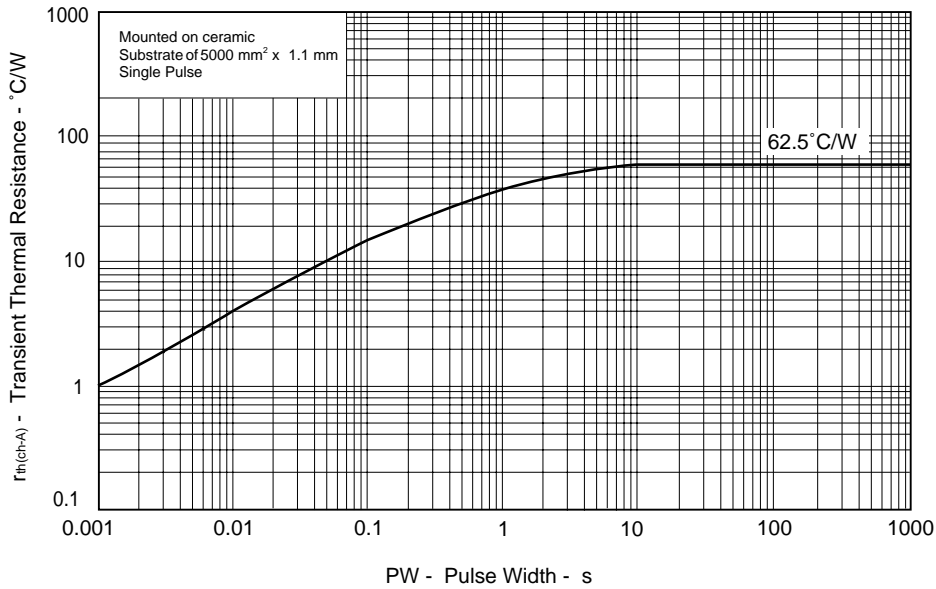
SOURCE TO DRAIN DIODE FORWARD VOLTAGE



DYNAMIC INPUT CHARACTERISTICS

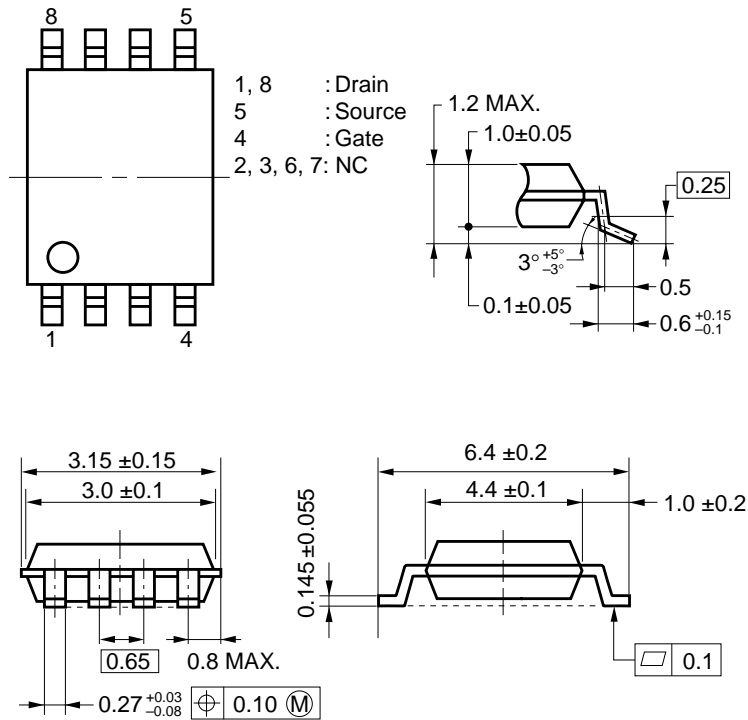


TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH



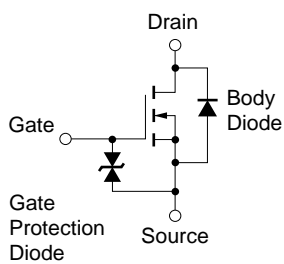
PACKAGE DRAWING (Unit: mm)

Power TSSOP8



**Caution** The terminal assignment is different from that of the NEC standard Power TSSOP8 package.

EQUIVALENT CIRCUIT



**Remark** The diode connected between the gate and source of the transistor serves as a protector against ESD. When this device actually used, an additional protection circuit is externally required if a voltage exceeding the rated voltage may be applied to this device.

[MEMO]

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