

SWITCHING

N-CHANNEL POWER MOS FET

INDUSTRIAL USE

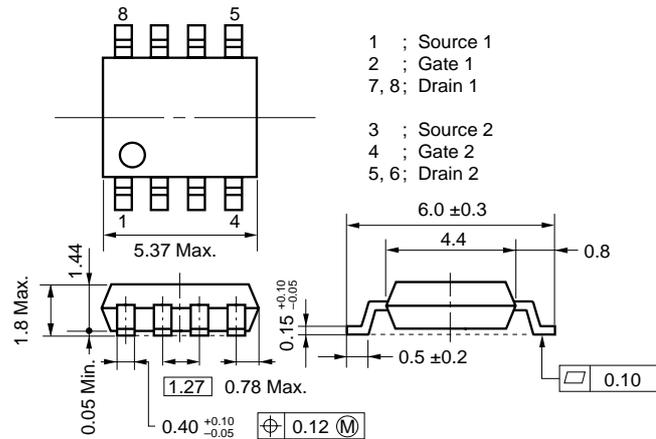
Description

This product is Dual N-Channel MOS Field Effect Transistor designed for power management application of notebook computers, and Li-ion battery application.

Features

- Dual MOS FET chips in small package
- 2.5 V gate drive type and low on-resistance
 $R_{DS(on)1} = 23 \text{ m}\Omega$ (MAX.) ($V_{GS} = 4.5 \text{ V}$, $I_D = 3.5 \text{ A}$)
 $R_{DS(on)2} = 32 \text{ m}\Omega$ (MAX.) ($V_{GS} = 2.5 \text{ V}$, $I_D = 3.5 \text{ A}$)
- Low C_{iss} $C_{iss} = 750 \text{ pF}$ Typ.
- Built-in G-S protection diode
- Small and surface mount package
 (Power SOP8)

Package Drawing (Unit : mm)



Ordering information

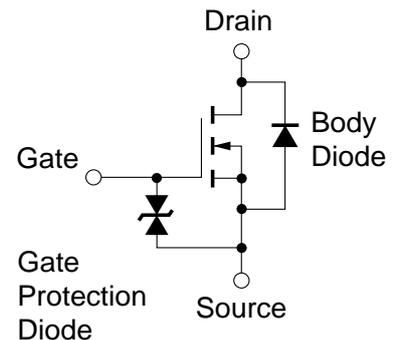
Part Number	Package
μ PA1757G	Power SOP8

Absolute Maximum Ratings ($T_A = 25 \text{ }^\circ\text{C}$)

Drain to source voltage	V_{DSS}	20	V
Gate to source voltage	V_{GSS}	± 12.0	V
Drain current (DC)	$I_{D(DC)}$	± 7.0	A
Drain current (pulse) ^{Note1}	$I_{D(pulse)}$	± 28	A
Total power dissipation (1 unit) ^{Note2}	P_T	1.7	W
Total power dissipation (2 unit) ^{Note2}	P_T	2.0	W
Channel temperature	T_{ch}	150	$^\circ\text{C}$
Storage temperature	T_{stg}	-55 to +150	$^\circ\text{C}$

Notes 1. $PW \leq 10 \mu\text{s}$, Duty Cycle $\leq 1\%$

2. $T_A = 25 \text{ }^\circ\text{C}$, Mounted on ceramic substrate of $2000 \text{ mm}^2 \times 1.1 \text{ mm}$



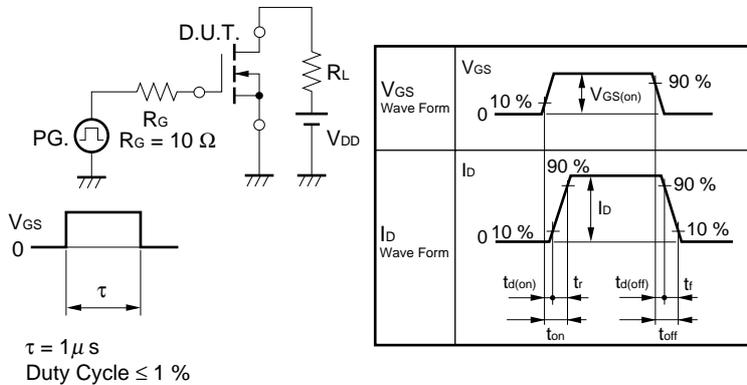
The diode connected between the gate and source of the transistor serves as a protector against ESD. When this device actually used, an additional protection circuit is externally required if a voltage exceeding the rated voltage may be applied to this device.

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 Not all devices/types available in every country. Please check with local NEC representative for availability and additional information.

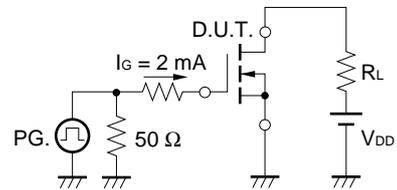
Electrical Characteristics (T_A = 25 °C)

Characteristics	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
Drain to source on-state resistance	R _{DS(on)1}	V _{GS} = 4.5 V, I _D = 3.5 A		16.2	23	mΩ
	R _{DS(on)2}	V _{GS} = 2.5 V, I _D = 3.5 A		22	32	mΩ
Gate to source cutoff voltage	V _{GS(off)}	V _{DS} = 10 V, I _D = 1.0 mA	0.5	0.8	1.5	V
Forward transfer admittance	y _{fs}	V _{DS} = 10 V, I _D = 3.5 A	5.0	13		S
Drain leakage current	I _{DSS}	V _{DS} = 20 V, V _{GS} = 0 V			10	μA
Gate to source leakage current	I _{GSS}	V _{GS} = ±12.0 V, V _{DS} = 0 V			±10	μA
Input capacitance	C _{iss}	V _{DS} = 10 V		750		pF
Output capacitance	C _{oss}	V _{GS} = 0 V		420		pF
Reverse transfer capacitance	C _{rss}	f = 1 MHz		140		pF
Turn-on delay time	t _{d(on)}	I _D = 3.5 A		57		ns
Rise time	t _r	V _{GS(on)} = 4.0 V		206		ns
Turn-off delay time	t _{d(off)}	V _{DD} = 10 V		593		ns
Fall time	t _f	R _G = 10 Ω		815		ns
Total gate charge	Q _G	I _D = 7.0 A		13.0		nC
Gate to source charge	Q _{GS}	V _{DD} = 16 V		2.6		nC
Gate to drain charge	Q _{GD}	V _{GS} = 4.0 V		5.3		nC
Body diode forward voltage	V _{F(S-D)}	I _F = 7.0 A, V _{GS} = 0 V		0.75		V

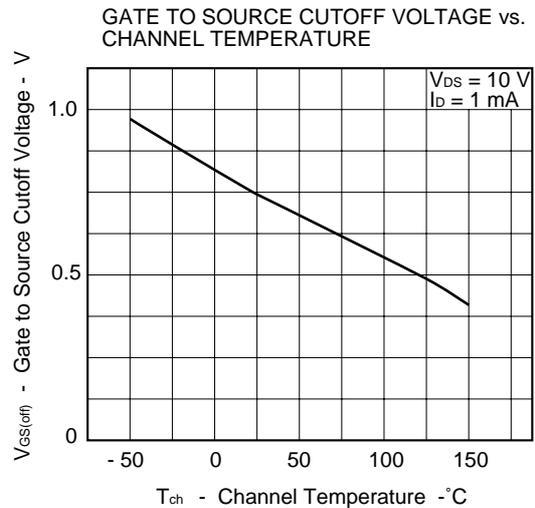
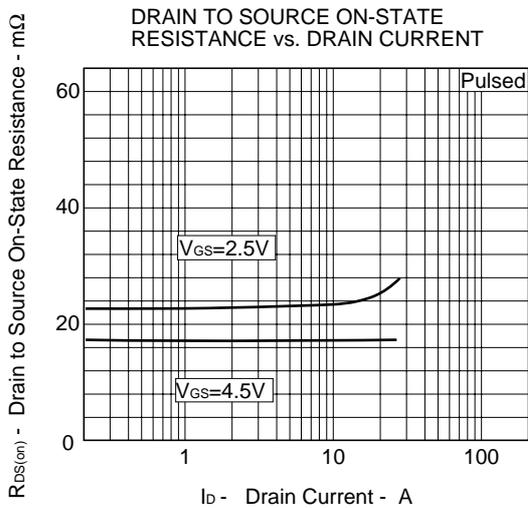
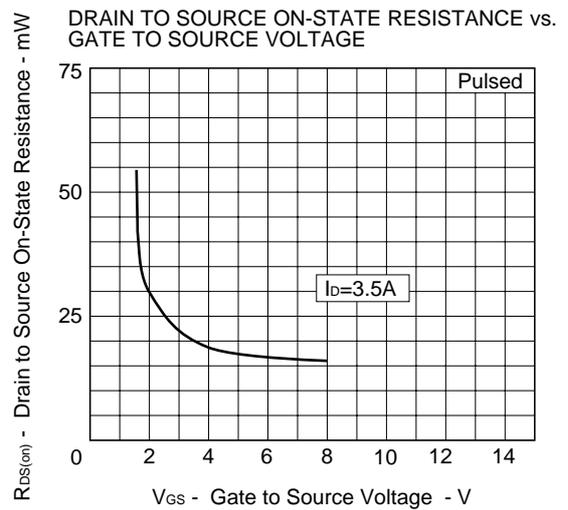
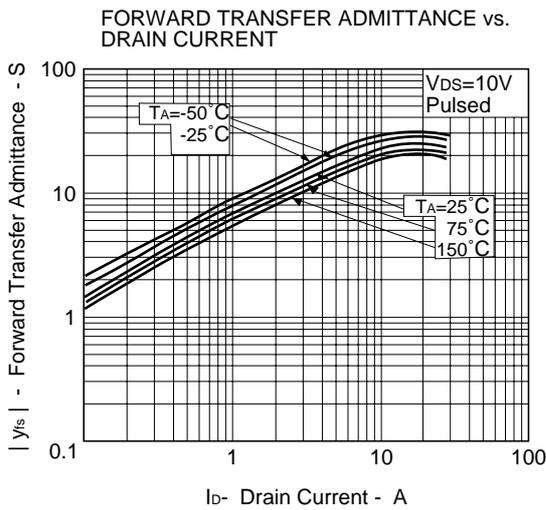
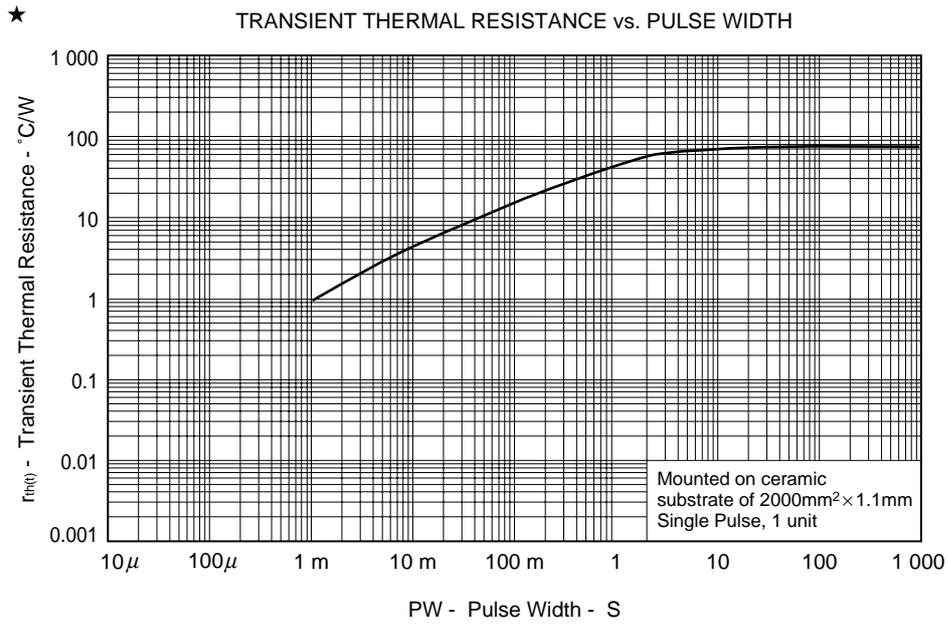
Test circuit 1 Switching time

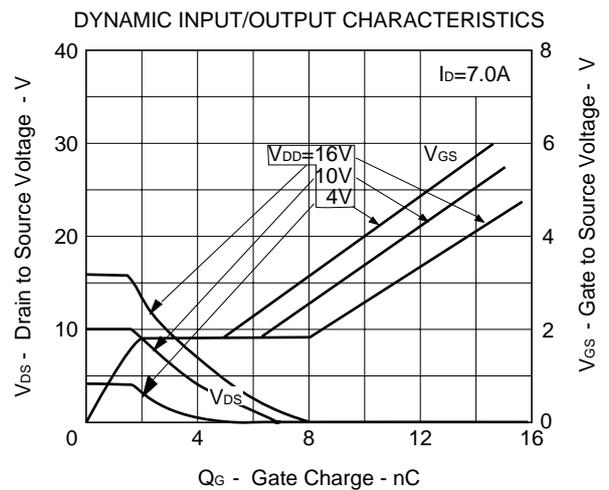
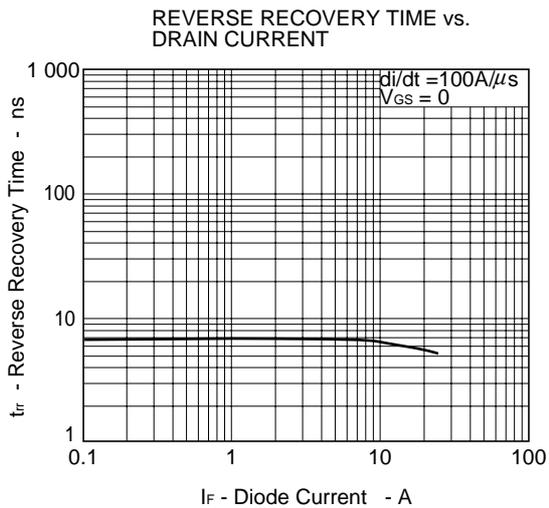
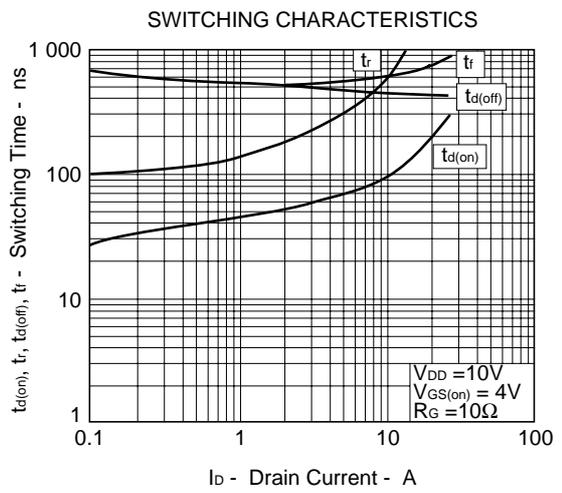
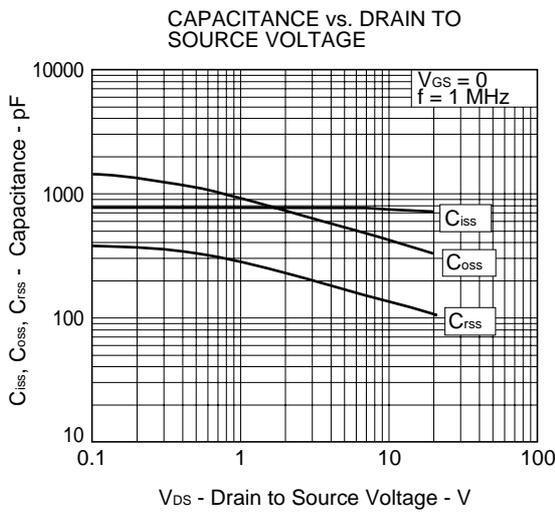
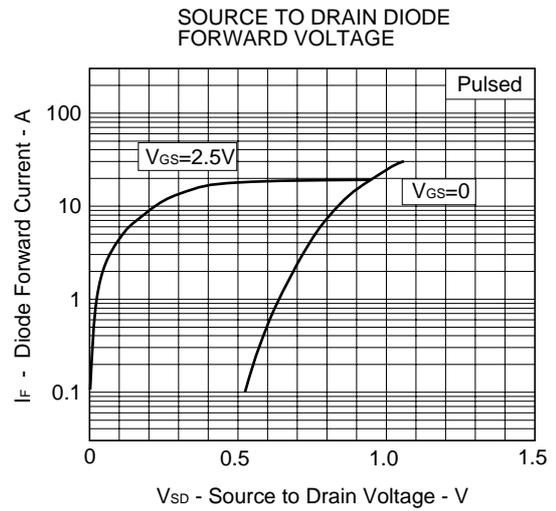
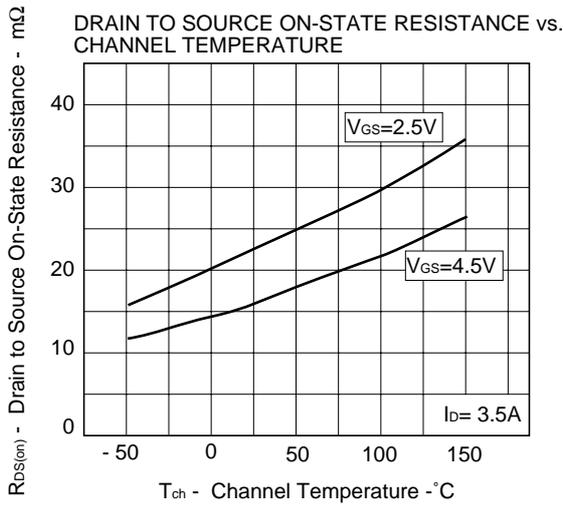


Test circuit 2 Gate charge

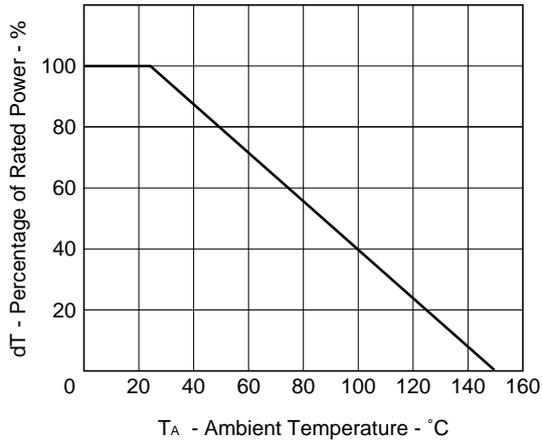


Typical Characteristics ($T_A = 25^\circ\text{C}$)

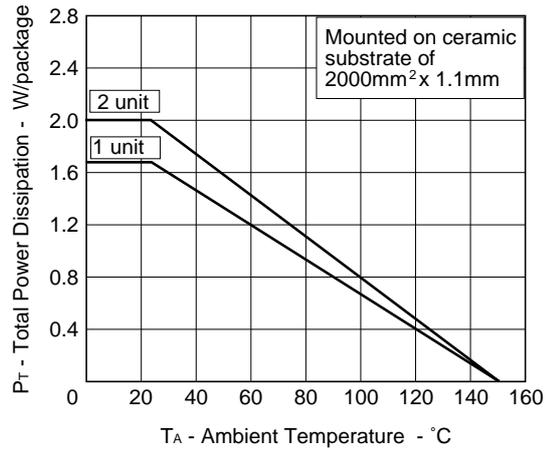




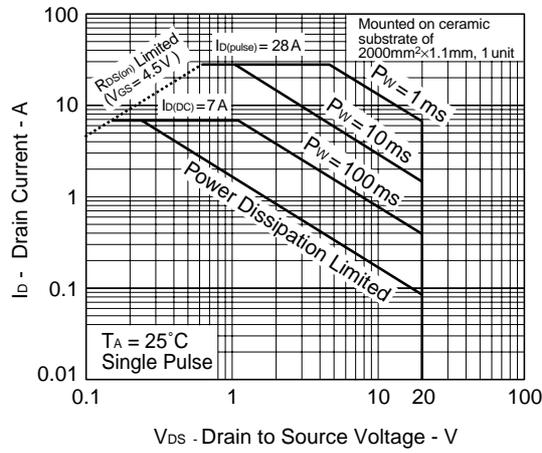
DERATING FACTOR OF FORWARD BIAS SAFE OPERATING AREA



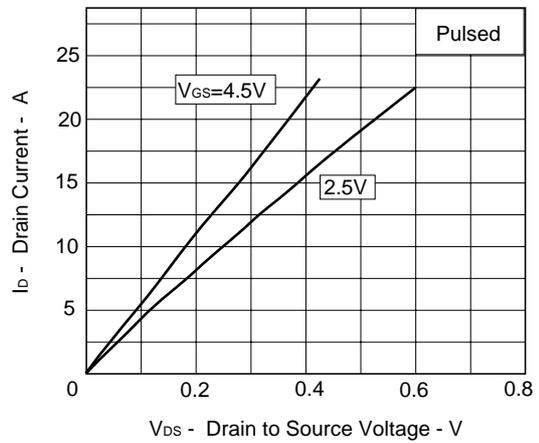
TOTAL POWER DISSIPATION vs. AMBIENT TEMPERATURE



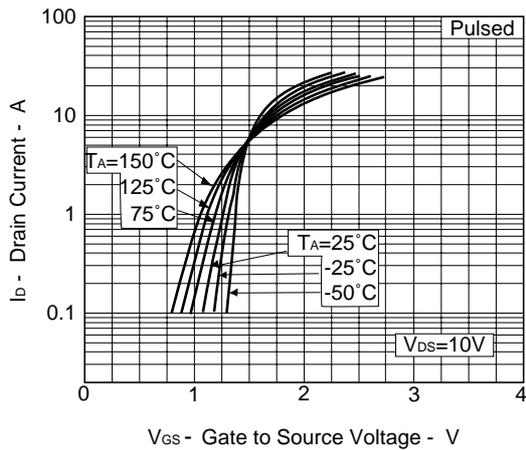
★ FORWARD BIAS SAFE OPERATING AREA



DRAIN CURRENT vs. DRAIN TO SOURCE VOLTAGE



FORWARD TRANSFER CHARACTERISTICS



[MEMO]

[MEMO]

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