

MOS FIELD EFFECT TRANSISTOR μ PA1741TP

SWITCHING N-CHANNEL POWER MOS FET

DESCRIPTION

The μ PA1741TP is N-channel MOS FET device that features a low on-state resistance and excellent switching characteristics, and designed for high voltage applications such as DC/DC converter.

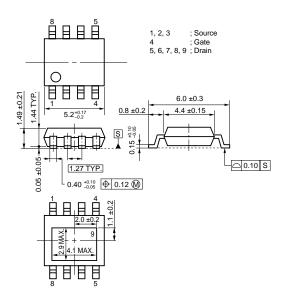
FEATURES

- High voltage: VDSS = 250 V
- Gate voltage rating: ±30 V
- Low on-state resistance
 - RDS(on) = 0.79Ω MAX. (Vgs = 10 V, ID = 2.5 A)
- Low input capacitance
 - Ciss = 340 pF TYP. (VDS = 10 V, VGS = 0 V)
- Built-in gate protection diode
- Small and surface mount package (Power HSOP8)

ORDERING INFORMATION

PART NUMBER	PACKAGE
μPA1741TP	Power HSOP8

PACKAGE DRAWING (Unit: mm)



ABSOLUTE MAXIMUM RATINGS (TA = 25°C, unless otherwise noted. All terminals are connected.)

Drain to Source Voltage (Vgs = 0 V)	VDSS	250	V	
Gate to Source Voltage (Vps = 0 V)	Vgss	±30	V	EQUIVALENT CIRCUIT
Drain Current (DC) (Tc = 25°C)	ID(DC)	±5.0	Α	
Drain Current (pulse) Note1	ID(pulse)	±15	Α	Drain
Total Power Dissipation (Tc = 25°C)	P _{T1}	21	W	
Total Power Dissipation (T _A = 25°C) ^{Note2}	P _{T2}	1	W	→ Body
Channel Temperature	Tch	150	°C	Gate Diode
Storage Temperature	Tstg	-55 to +150	°C	* +
Single Avalanche Current Note3	las	5.0	Α	Gate
Single Avalanche Energy Note3	Eas	2.5	mJ	Protection Source Diode
Repetitive Avalanche Current Note4	I AR	5.0	Α	
Repetitive Pulse Avalanche Energy Note4	Ear	2.5	mJ	

Notes 1. PW \leq 10 μ s, Duty Cycle \leq 1%

- 2. Mounted on glass epoxy board of 1 inch x 1 inch x 0.8 mm
- 3. Starting Tch = 25°C, VdD = 125 V, Rg = 25 Ω , L = 100 μ H, Vgs = 20 \rightarrow 0 V
- **4.** $T_{ch(peak)} \le 150^{\circ}C$, L = 100 μ H

Remark The diode connected between the gate and source of the transistor serves as a protector against ESD. When this device actually used, an additional protection circuit is externally required if a voltage exceeding the rated voltage may be applied to this device.

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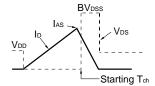
ELECTRICAL CHARACTERISTICS (TA = 25°C, unless otherwise noted. All terminals are connected.)

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CHARACTERISTICS	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Zero Gate Voltage Drain Current	IDSS	V _{DS} = 250 V, V _{GS} = 0 V			10	μΑ
Gate Leakage Current	Igss	$V_{GS} = \pm 30 \text{ V}, V_{DS} = 0 \text{ V}$			±10	μΑ
Gate Cut-off Voltage	V _{GS(off)}	V _{DS} = 10 V, I _D = 1 mA	2.5	3.5	4.5	V
Forward Transfer Admittance Note	yfs	V _{DS} = 10 V, I _D = 2.5 A	2	3.5		S
Drain to Source On-state Resistance Note	R _{DS(on)}	V _G S = 10 V, I _D = 2.5 A		0.63	0.79	Ω
Input Capacitance	Ciss	V _{DS} = 10 V		340		pF
Output Capacitance	Coss	Vgs = 0 V		70		pF
Reverse Transfer Capacitance	Crss	f = 1 MHz		30		pF
Turn-on Delay Time	td(on)	V _{DD} = 125 V, I _D = 2.5 A		11		ns
Rise Time	tr	Vgs = 10 V		8		ns
Turn-off Delay Time	td(off)	R _G = 10 Ω		20		ns
Fall Time	tf			6		ns
Total Gate Charge	QG	VDD = 200 V		11		nC
Gate to Source Charge	Qgs	Vgs = 10 V		2		nC
Gate to Drain Charge	Q _{GD}	ID = 5.0 A		5.5		nC
Body Diode Forward Voltage Note	V _{F(S-D)}	I _F = 5.0 A, V _{GS} = 0 V		0.9	1.5	V
Reverse Recovery Time	trr	I _F = 5.0 A, V _{GS} = 0 V		120		ns
Reverse Recovery Charge	Qrr	di/dt = 100 A/μs		400		nC

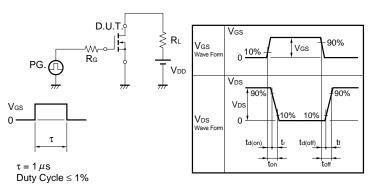
Note Pulsed: PW \leq 800 μ s, Duty Cycle \leq 2%

TEST CIRCUIT 1 AVALANCHE CAPABILITY

$V_{GS} = 20 \rightarrow 0 \text{ V}$ $PG. \bigcirc PG. \bigcirc PG.$



TEST CIRCUIT 2 SWITCHING TIME



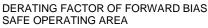
TEST CIRCUIT 3 GATE CHARGE

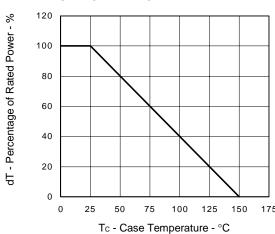
$$\begin{array}{c|c} D.U.T. \\ \hline I_G = 2 \text{ mA} \\ \hline \end{array}$$

$$\begin{array}{c|c} PG. & \\ \hline \end{array} \begin{array}{c} S & \\ \hline \end{array} \begin{array}{c} D.U.T. \\ \hline \end{array}$$

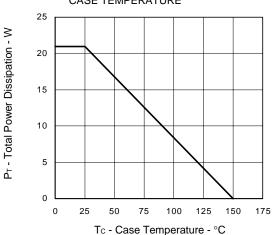
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TYPICAL CHARACTERISTICS (TA = 25°C)

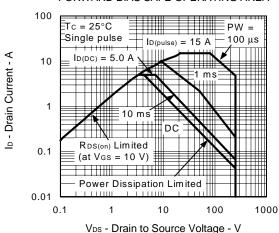




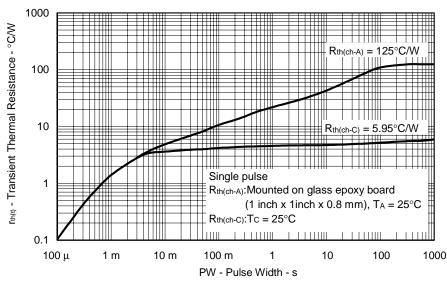
TOTAL POWER DISSIPATION vs. CASE TEMPERATURE



FORWARD BIAS SAFE OPERATING AREA

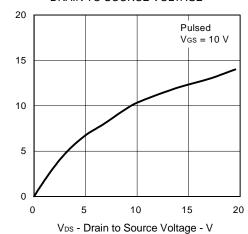


TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH

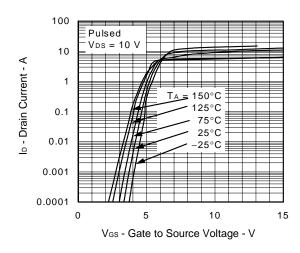


lo - Drain Current - A

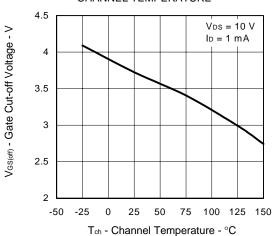
DRAIN CURRENT vs. DRAIN TO SOURCE VOLTAGE



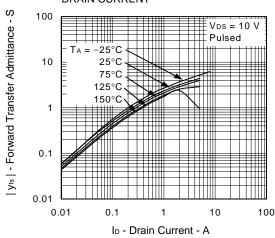
FORWARD TRANSFER CHARACTERISTICS



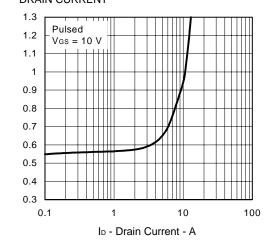
GATE CUT-OFF VOLTAGE vs. CHANNEL TEMPERATURE



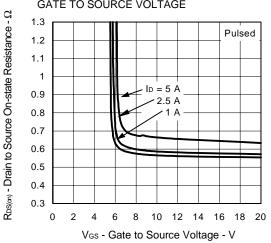
FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT



DRAIN TO SOURCE ON-STATE RESISTANCE vs. DRAIN CURRENT

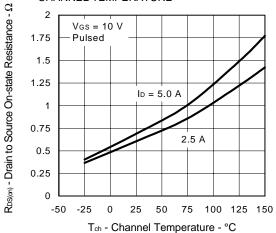


DRAIN TO SOURCE ON-STATE RESISTANCE vs. GATE TO SOURCE VOLTAGE

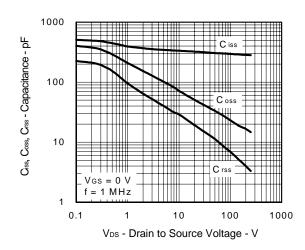


 $\mathsf{R}_{\mathsf{DS}(\varpi)}$ - Drain to Source On-state Resistance - Ω

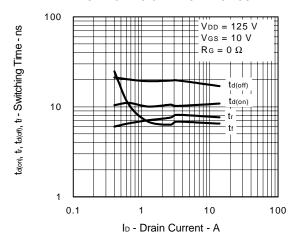
DRAIN TO SOURCE ON-STATE RESISTANCE vs. CHANNEL TEMPERATURE



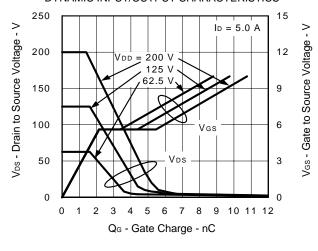
CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE



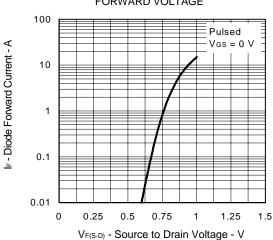
SWITCHING CHARACTERISTICS



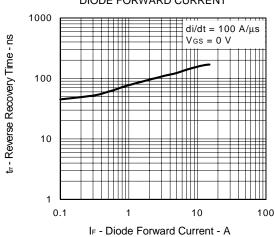
DYNAMIC INPUT/OUTPUT CHARACTERISTICS



SOURCE TO DRAIN DIODE FORWARD VOLTAGE

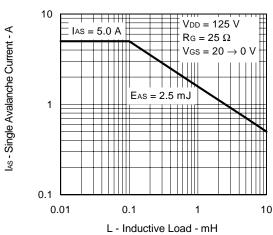


REVERSE RECOVERY TIME vs. DIODE FORWARD CURRENT

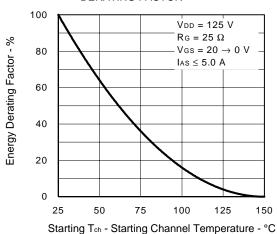


μ PA1741TP

SINGLE AVALANCHE CURRENT vs. INDUCTIVE LOAD



SINGLE AVALANCHE ENERGY DERATING FACTOR



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