NEC

MOS FIELD EFFECT TRANSISTOR

μPA1723

SWITCHING
N-CHANNEL POWER MOS FET
INDUSTRIAL USE

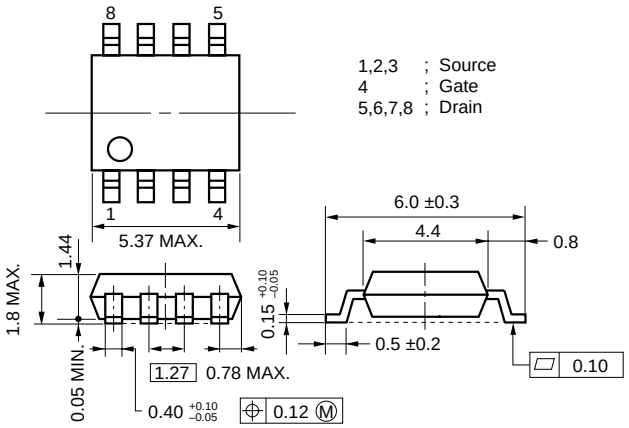
DESCRIPTION

The μPA1723 is N-Channel MOS Field Effect Transistor designed for power management switch.

FEATURES

- Low on-state resistance
  $R_{DS(on)1}$ = 6.7 mΩ MAX. (V_{GS} = 4.5 V, I_D = 7.0 A)
  $R_{DS(on)2}$ = 7.4 mΩ MAX. (V_{GS} = 4.0 V, I_D = 7.0 A)
  $R_{DS(on)3}$ = 8.7 mΩ MAX. (V_{GS} = 2.5 V, I_D = 7.0 A)
- Low C_{iss} : C_{iss} = 3800 pF TYP.
- Built-in G-S protection diode
- Small and surface mount package (Power SOP8)

PACKAGE DRAWING (Unit : mm)



ORDERING INFORMATION

PART NUMBER	PACKAGE
μPA1723G	Power SOP8

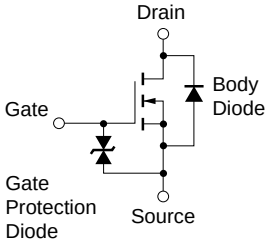
ABSOLUTE MAXIMUM RATINGS (T_A = 25°C, All terminals are connected.)

Drain to Source Voltage (V_{GS} = 0 V)	V_{DSS}	20	V
Gate to Source Voltage (V_{DS} = 0 V)	V_{GSS}	±12	V
Drain Current (DC)	$I_{D(DC)}$	±13	A
Drain Current (pulse) **Note1**	$I_{D(pulse)}$	±52	A
Total Power Dissipation (T_A = 25°C) **Note2**	P_T	2.0	W
Channel Temperature	T_{ch}	150	°C
Storage Temperature	T_{stg}	–55 to + 150	°C

Notes 1. PW ≤ 10 μs, Duty Cycle ≤ 1 %

2. Mounted on ceramic substrate of 1200 mm^2 x 2.2mm

EQUIVALENT CIRCUIT



Remark The diode connected between the gate and source of the transistor serves as a protector against ESD. When this device actually used, an additional protection circuit is externally required if a voltage exceeding the rated voltage may be applied to this device.

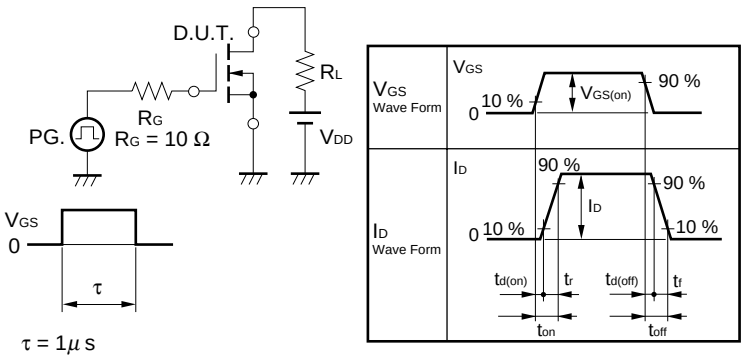
Document No. G14026EJ2V0DS00 (2nd edition)
Date Published April 2001 NS CP(K)
Printed in Japan

The mark ★ shows major revised points.

ELECTRICAL CHARACTERISTICS (T_A = 25 °C, All terminals are connected.)

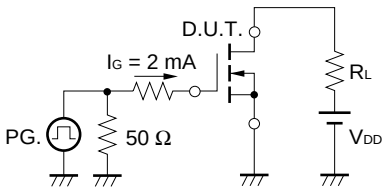
CHARACTERISTICS	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Drain to Source On-state Resistance	$R_{DS(on)1}$	V_{GS} = 4.5 V, I_D = 7.0 A		5.4	6.7	mΩ
	$R_{DS(on)2}$	V_{GS} = 4.0 V, I_D = 7.0 A		5.5	7.4	mΩ
	$R_{DS(on)3}$	V_{GS} = 2.5 V, I_D = 7.0 A		6.5	8.7	mΩ
Gate to Source Cut-off Voltage	$V_{GS(off)}$	V_{DS} = 10 V, I_D = 1 mA	0.5	0.9	1.5	V
Forward Transfer Admittance	$\|y_{fs}\|$	V_{DS} = 10 V, I_D = 7.0 A	15.0	32		S
Drain Leakage Current	I_{DSS}	V_{DS} = 20 V, V_{GS} = 0 V			10	μA
Gate to Source Leakage Current	I_{GSS}	V_{GS} = ±12 V, V_{DS} = 0 V			±10	μA
Input Capacitance	C_{iss}	V_{DS} = 10 V		3800		pF
Output Capacitance	C_{oss}	V_{GS} = 0 V		1200		pF
Reverse Transfer Capacitance	C_{rss}	f = 1 MHz		700		pF
Turn-on Delay Time	$t_{d(on)}$	I_D = 7.0 A		70		ns
Rise Time	t_r	$V_{GS(on)}$ = 4.5 V		440		ns
Turn-off Delay Time	$t_{d(off)}$	V_{DD} = 10 V		230		ns
Fall Time	t_f	R_G = 10 Ω		300		ns
Total Gate Charge	Q_G	I_D = 13 A		47.0		nC
Gate to Source Charge	Q_{GS}	V_{DD} = 16 V		11.0		nC
Gate to Drain Charge	Q_{GD}	V_{GS} = 4.5 V		12.0		nC
Body Diode Forward Voltage	$V_{F(S-D)}$	I_F = 13.0 A, V_{GS} = 0 V		0.75		V
Reverse Recovery Time	t_{rr}	I_F = 13.0 A, V_{GS} = 0 V		68		ns
Reverse Recovery Charge	Q_{rr}	di/dt = 100 A/ μs		70		nC

TEST CIRCUIT 1 SWITCHING TIME



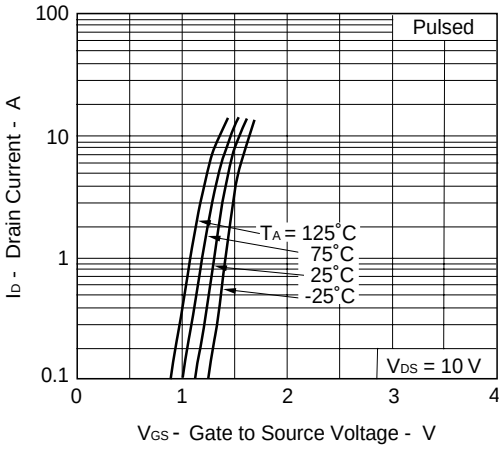
τ = 1μ s
Duty Cycle ≤ 1 %

TEST CIRCUIT 2 GATE CHARGE

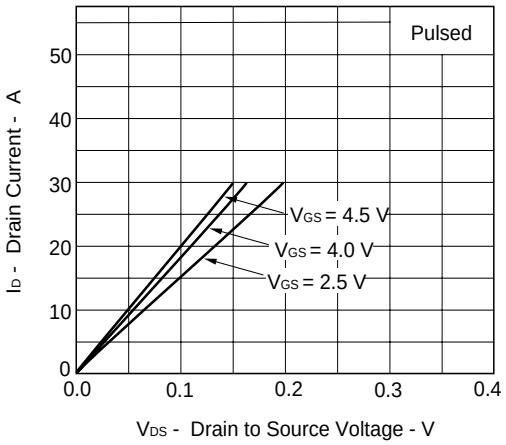


TYPICAL CHARACTERISTICS (T_A = 25°C)

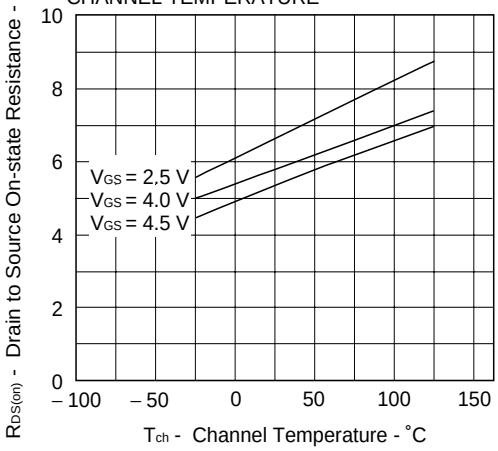
FORWARD TRANSFER CHARACTERISTICS



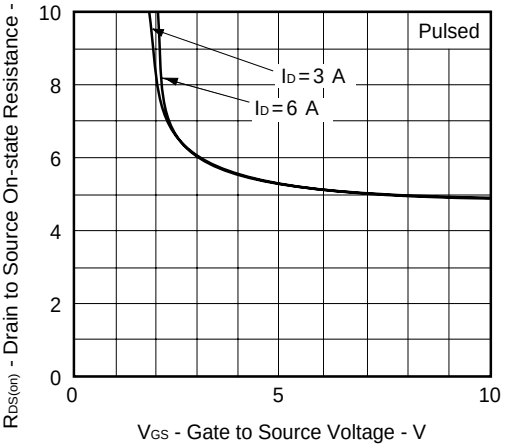
DRAIN CURRENT vs.
DRAIN TO SOURCE VOLTAGE



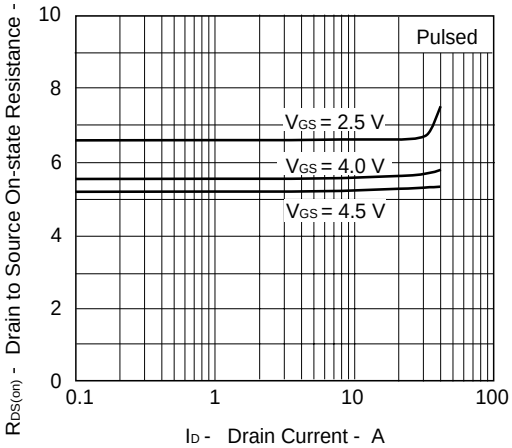
DRAIN TO SOURCE ON-STATE RESISTANCE vs.
CHANNEL TEMPERATURE



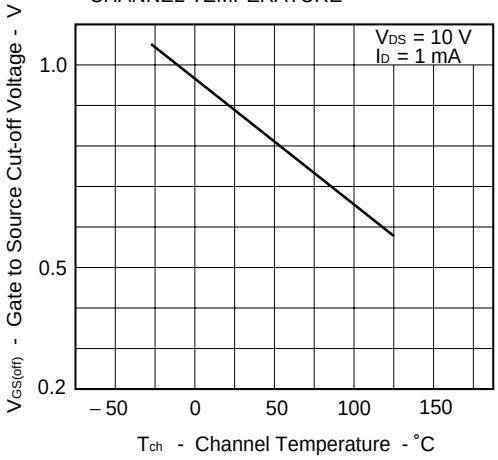
DRAIN TO SOURCE ON-STATE RESISTANCE vs.
GATE TO SOURCE VOLTAGE



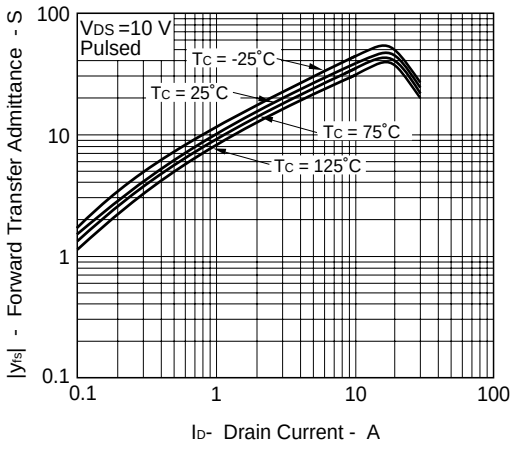
DRAIN TO SOURCE ON-STATE
RESISTANCE vs. DRAIN CURRENT



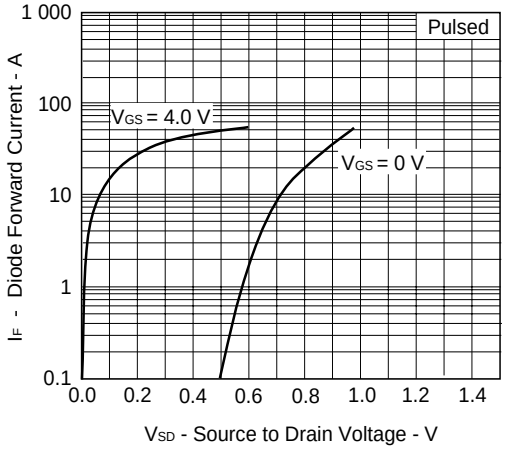
GATE TO SOURCE CUT-OFF VOLTAGE vs.
CHANNEL TEMPERATURE



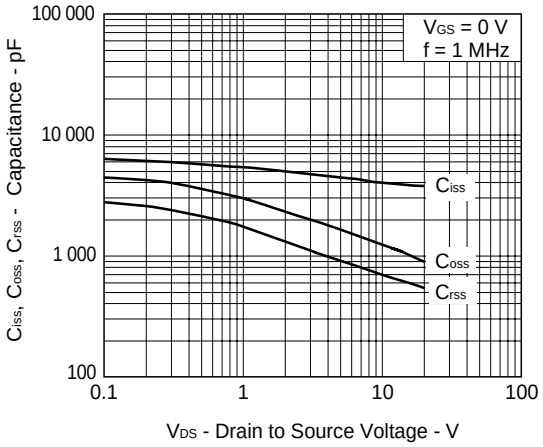
FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT



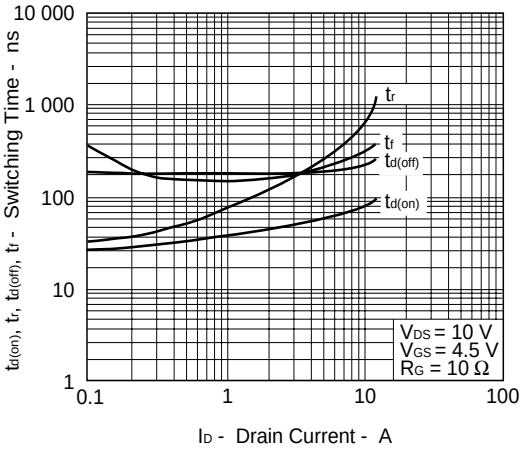
SOURCE TO DRAIN DIODE FORWARD VOLTAGE



CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE

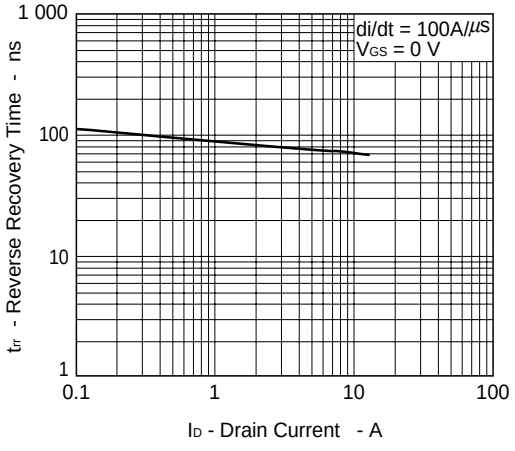


SWITCHING CHARACTERISTICS

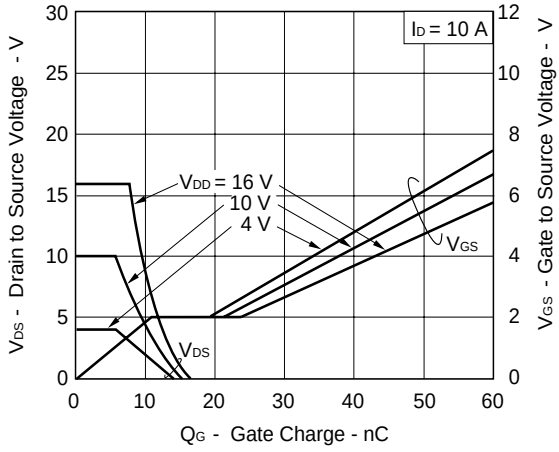


Remark
Mounted on ceramic substrate of 1200 mm^2 x 2.2 mm

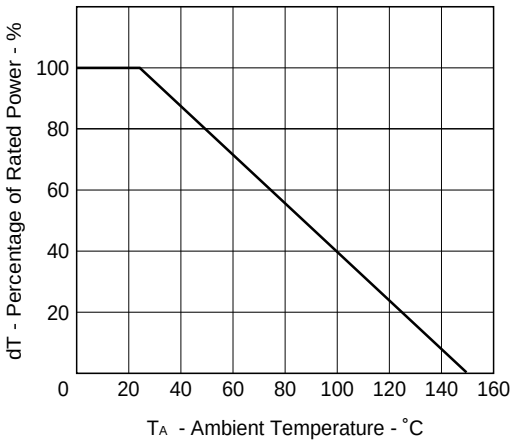
REVERSE RECOVERY TIME vs. DRAIN CURRENT



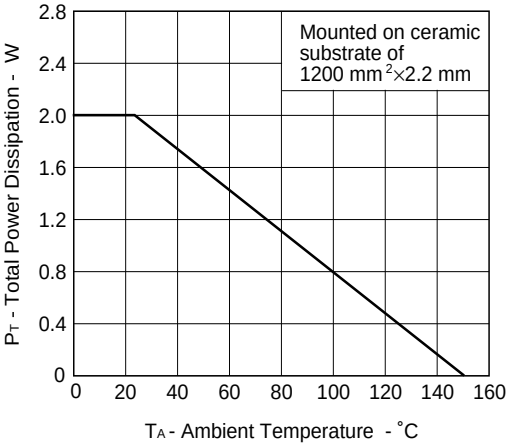
DYNAMIC INPUT/OUTPUT CHARACTERISTICS



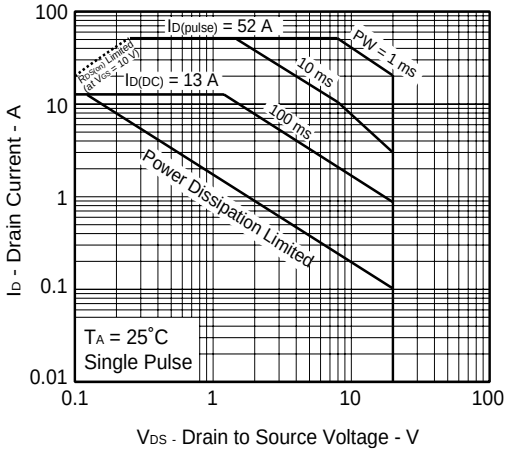
DERATING FACTOR OF FORWARD BIAS SAFE OPERATING AREA



TOTAL POWER DISSIPATION vs. AMBIENT TEMPERATURE

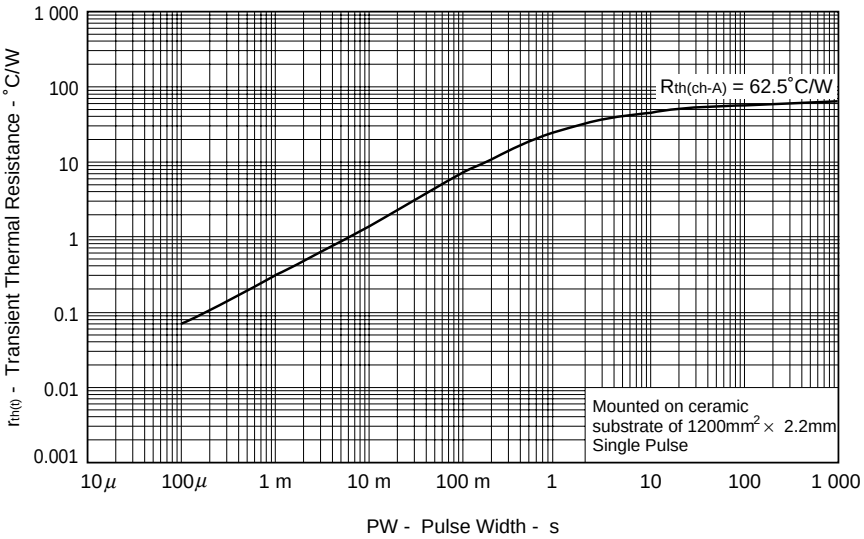


★ FORWARD BIAS SAFE OPERATING AREA



Remark
Mounted on ceramic substrate of 1200 mm^2 x 2.2 mm

TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH



[MEMO]

[MEMO]

- **The information in this document is current as of April, 2001. The information is subject to change without notice. For actual design-in, refer to the latest publications of NEC's data sheets or data books, etc., for the most up-to-date specifications of NEC semiconductor products. Not all products and/or types are available in every country. Please check with an NEC sales representative for availability and additional information.**
- No part of this document may be copied or reproduced in any form or by any means without prior written consent of NEC. NEC assumes no responsibility for any errors that may appear in this document.
- NEC does not assume any liability for infringement of patents, copyrights or other intellectual property rights of third parties by or arising from the use of NEC semiconductor products listed in this document or any other liability arising from the use of such products. No license, express, implied or otherwise, is granted under any patents, copyrights or other intellectual property rights of NEC or others.
- Descriptions of circuits, software and other related information in this document are provided for illustrative purposes in semiconductor product operation and application examples. The incorporation of these circuits, software and information in the design of customer's equipment shall be done under the full responsibility of customer. NEC assumes no responsibility for any losses incurred by customers or third parties arising from the use of these circuits, software and information.
- While NEC endeavours to enhance the quality, reliability and safety of NEC semiconductor products, customers agree and acknowledge that the possibility of defects thereof cannot be eliminated entirely. To minimize risks of damage to property or injury (including death) to persons arising from defects in NEC semiconductor products, customers must incorporate sufficient safety measures in their design, such as redundancy, fire-containment, and anti-failure features.
- NEC semiconductor products are classified into the following three quality grades:
  "Standard", "Special" and "Specific". The "Specific" quality grade applies only to semiconductor products developed based on a customer-designated "quality assurance program" for a specific application. The recommended applications of a semiconductor product depend on its quality grade, as indicated below. Customers must check the quality grade of each semiconductor product before using it in a particular application.

  "Standard": Computers, office equipment, communications equipment, test and measurement equipment, audio and visual equipment, home electronic appliances, machine tools, personal electronic equipment and industrial robots

  "Special": Transportation equipment (automobiles, trains, ships, etc.), traffic control systems, anti-disaster systems, anti-crime systems, safety equipment and medical equipment (not specifically designed for life support)

  "Specific": Aircraft, aerospace equipment, submersible repeaters, nuclear reactor control systems, life support systems and medical equipment for life support, etc.

  The quality grade of NEC semiconductor products is "Standard" unless otherwise expressly specified in NEC's data sheets or data books, etc. If customers wish to use NEC semiconductor products in applications not intended by NEC, they must contact an NEC sales representative in advance to determine NEC's willingness to support a given application.

  (Note)

  (1) "NEC" as used in this statement means NEC Corporation and also includes its majority-owned subsidiaries.

  (2) "NEC semiconductor products" means any semiconductor product developed or manufactured by or for NEC (as defined above).

M8E 00.4