

MOS FIELD EFFECT TRANSISTOR μ PA1701A

SWITCHING N-CHANNEL POWER MOS FET INDUSTRIAL USE

DESCRIPTION

This product is N-Channel MOS Field Effect Transistor designed for power management applications and Li-ion battery application.

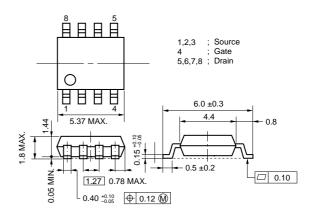
FEATURES

- 2.5 V gate drive and low on-resistance
 R_{DS(on)1} = 27 mΩ (MAX.) (V_{GS} = 4.0 V, I_D = 3.5 A)
 R_{DS(on)2} = 40 mΩ (MAX.) (V_{GS} = 2.5 V, I_D = 3.5 A)
- Low Ciss : Ciss = 1040 pF (TYP.)
- Built-in G-S protection diode
- Small and surface mount package (Power SOP8)

ORDERING INFORMATION

PART NUMBER	PACKAGE
μPA1701AG	Power SOP8

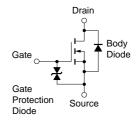
PACKAGE DRAWING (Unit: mm)



EQUIVARENT CIRCUIT

ABSOLUTE MAXIMUM RATINGS (TA = 25°C, All terminals are connected.)

Drain to Source Voltage (Vgs = 0 V)	VDSS	30	V
Gate to Source Voltage (VDS = 0 V)	Vgss	±12	V
Drain Current (DC)	ID(DC)	±7.0	Α
Drain Current (pulse) Note1	D(pulse)	±28	Α
Total Power Dissipation (T _A = 25°C) Note2	Рт	2.0	W
Channel Temperature	Tch	150	°C
Storage Temperature	Tstg	-55 to + 150	°C



- **Notes 1.** PW \leq 10 μ s, Duty Cycle \leq 1 %
 - 2. Mounted on ceramic substrate of 1200 mm² x 1.7mm

Remark The diode connected between the gate and source of the transistor serves as a protector against ESD. When this device actually used, an additional protection circuit is externally required if a voltage exceeding the rated voltage may be applied to this device.

The information in this document is subject to change without notice.



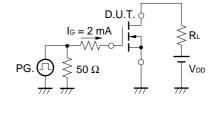
ELECTRICAL CHARACTERISTICS (T_A = 25 °C)

CHARACTERISTICS	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Drain to Source On-state Resistance	RDS(on)1	Vgs = 4.0 V, ID = 3.5 A		19	27	mΩ
	R _{DS(on)2}	Vgs = 2.5 V, ID = 3.5 A		25	40	mΩ
Gate to Source Cut-off Voltage	V _{GS(off)}	V _{DS} = 10 V, I _D = 1 mA	0.5	0.9	1.5	V
Forward Transfer Admittance	yfs	V _{DS} = 10 V, I _D = 3.5 A	6.0	13		S
Drain Leakage Current	Ipss	V _{DS} = 30 V, V _{GS} = 0 V			10	μΑ
Gate to Source Leakage Current	Igss	Vgs = ±12 V, Vps = 0 V			±10	μΑ
Input Capacitance	Ciss	V _{DS} = 10 V		1040		pF
Output Capacitance	Coss	Vgs = 0 V		340		pF
Reverse Transfer Capacitance	Crss	f = 1 MHz		150		pF
Turn-on Delay Time	t _{d(on)}	ID = 3.5 A		25		ns
Rise Time	tr	VGS(on) = 4.0 V		120		ns
Turn-off Delay Time	td(off)	V _{DD} = 15 V		73		ns
Fall Time	tf	R _G = 10 Ω		77		ns
Total Gate Charge	QG	ID = 7.0 A		13.2		nC
Gate to Source Charge	Qgs	VDD = 24 V		1.8		nC
Gate to Drain Charge	Q _{GD}	Vgs = 4.0 V		5.8		nC
Body Diode Forward Voltage	V _{F(S-D)}	IF = 7.0 A, VGS = 0 V		0.77		V
Reverse Recovery Time	trr	IF = 7.0 A, VGS = 0 V		31		ns
Reverse Recovery Charge	Qrr	$di/dt = 100 \text{ A/ } \mu\text{s}$		58		nC

TEST CIRCUIT 1 SWITCHING TIME

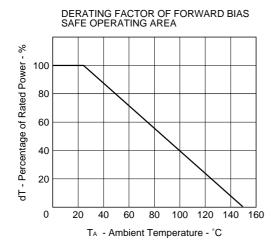
PG. $\bigcap_{RG} R_G = 10 \Omega$ $V_{GS} \bigvee_{Wave Form} V_{DD} \bigvee_{Wave Form} V_{GS} \bigvee_{Wave Form} V_{GS} \bigvee_{UD} V_{UD} \bigvee_{UD} V_{GS} \bigvee_{UD} V_{GS} \bigvee_{UD} V_{GS} \bigvee_{UD} V_{GS} \bigvee_{U$

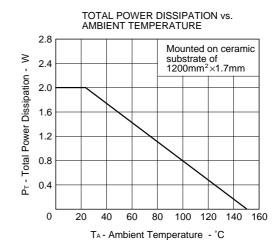
TEST CIRCUIT 2 GATE CHARGE

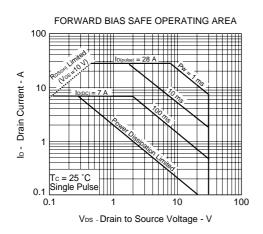


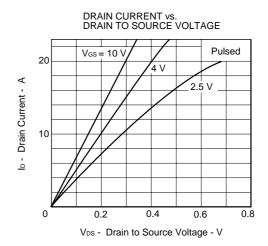


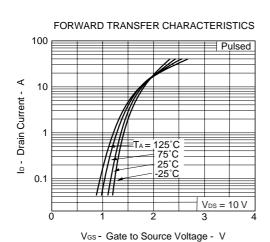
TYPICAL CHARACTERISTICS (TA = 25 °C)



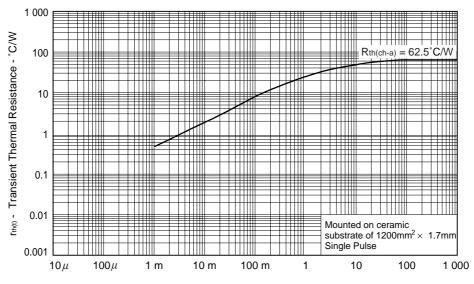






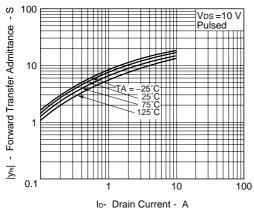


TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH

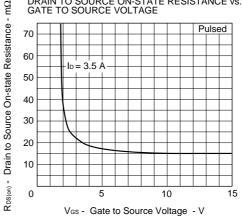


PW - Pulse Width - s

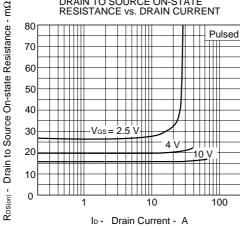


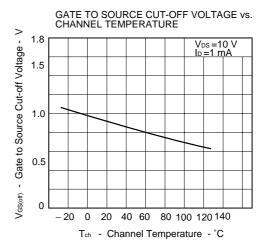


DRAIN TO SOURCE ON-STATE RESISTANCE vs. GATE TO SOURCE VOLTAGE

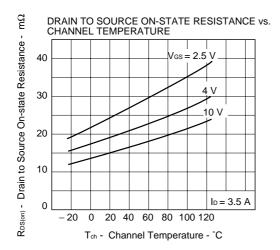


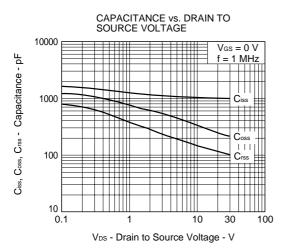
DRAIN TO SOURCE ON-STATE RESISTANCE vs. DRAIN CURRENT

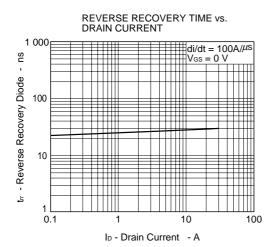


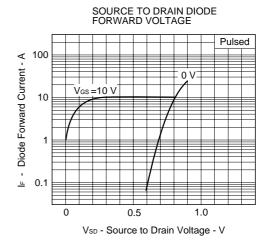


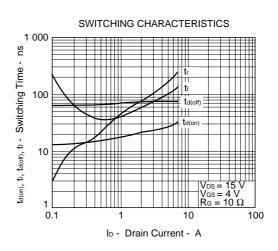


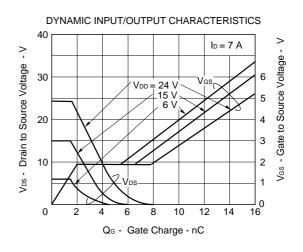












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Anti-radioactive design is not implemented in this product.

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