1. General Description

The UMC's MORTAR (286AT) Chip Set UM82C230 series provides an economic alternative for building a reliable IBM PC/AT compatible system.

A commercial 12MHZ/O wait state, 4MByte main memory system and math-coprocessor can be easily built by using 3 VLSIs, 8 logic components plus memory and processor.

2. Features

- Fully PC/AT-Compatible for 10MHz and 12MHz systems.
- Guaranteed zero wait state for 80ns DRAMs at 12MHz and one wait state for 120ns DRAMs at 12.5MHz.
- Supports up to 4MB local memory on board.
- Remaps 384KB of top of system local memory space.
- Supports 1M/256K SIM module.
- Supports 12MHz operation with one wait state for 200ns EPROM.
- Commercially available BIOS (Phoenix/Award/AMI) applicable.
- Easy design system board, three VLSI chips and eight TTLs configure all the logic.
- Landmark speed=15.9MHz operating at 12MHz, 16.5MHz operating at 12.5MHz.

The UM82C230 MORTAR chipset consists of the UM82C231 System/Memory Controller, the UM82C232 Data/Address Buffer and the UM82C206 Integrated Peripherals Controller (IPC).

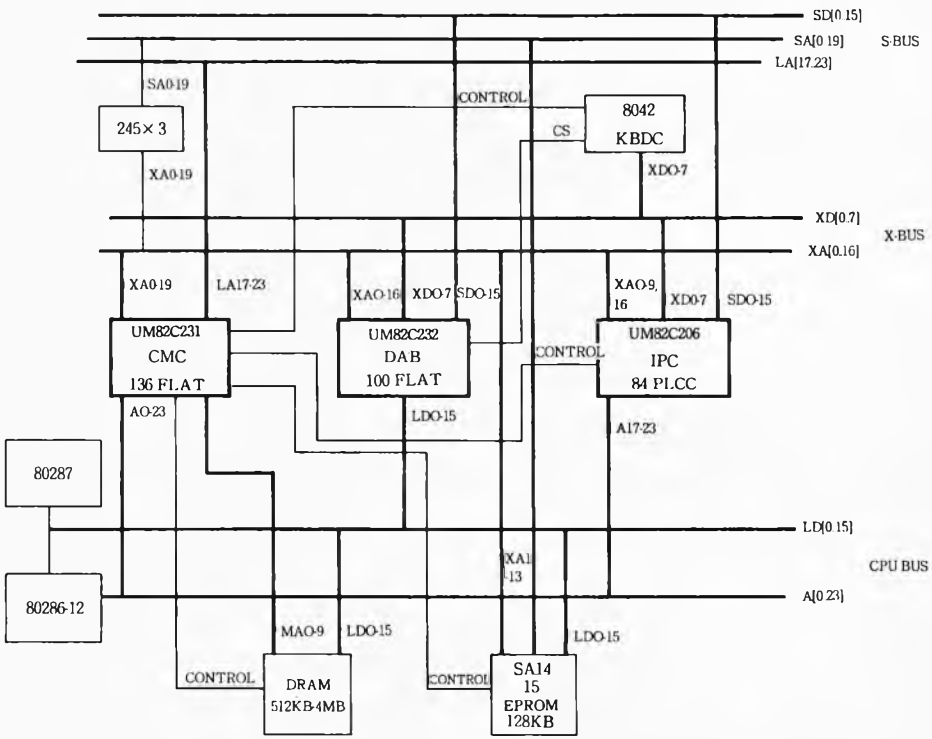
As shown in the System Block Diagram, there are three data buses: local data bus, AT data bus and peripheral data (XD) bus. The local DRAM, EPROM and Numerical Processor are located on the local data bus. The UM82C206 and 8042 Keyboard Controller sit on the XD bus. The AT data bus was driven by the UM82C232 directly which conveys the data to/from the AT Channel Adaptors.

The address bus architecture is also very simple; local CPU address bus, local DRAM address bus (MA), peripheral address bus (XA) and AT address bus. The local address bus is shared between CPU, UM82C231 and UM82C206. The MA bus is used by the local DRAM only. Most of the system board devices are attached to the XA bus, like UM82C232, UM82C206, ROMs and 8042. Some AT address lines are driven by the UM82C231 or UM82C232 directly; the others are buffered.

The UM82C231 provides synchronization and control signals for all buses. The UM82C231 also distinguishes if the current cycle is local memory cycle. Upon detecting that it is a local DRAM cycle, no AT control signals are sent out to the AT channel. The UM82C231 is based on the memory configurations to complete the current cycle with fastest response. If the cycle is AT cycle, the UM82C231 sends out the control signals sequentially which are then used by the adaptors or system board devices to receive the write data or to send the fetched data. Then, depending on the status signals sent back by the adaptors or system board devices, the UM82C231 determines which kind of AT cycles to perform: 8-bit, 16-bit, bus conversion, wait state insert, or 0 wait state cycle.

The UM82C232 Data/Address buffer provides the buffering and latching between the CPU local data bus, AT bus and XD bus. The parity bit generation and parity bit checking logic resides in the UM82C232 also. During DMA cycles, the UM82C232 latches the address from XD, which is sent by the UM82C206, and transfers to XA bus.

MORTAR Chip Set System Diagram



Required IC List :

80286	× 1	74E74	× 1
UM82C231	× 1	74LS08	× 1
UM82C232	× 1	7407	× 1
UM82C206	× 1	14069	× 1
27256	× 2	74ALS04	× 1
8042	× 1	74ALS245	× 3