CURRENT MODE PWM CONTROLLER (KNOWN GOOD DIE)

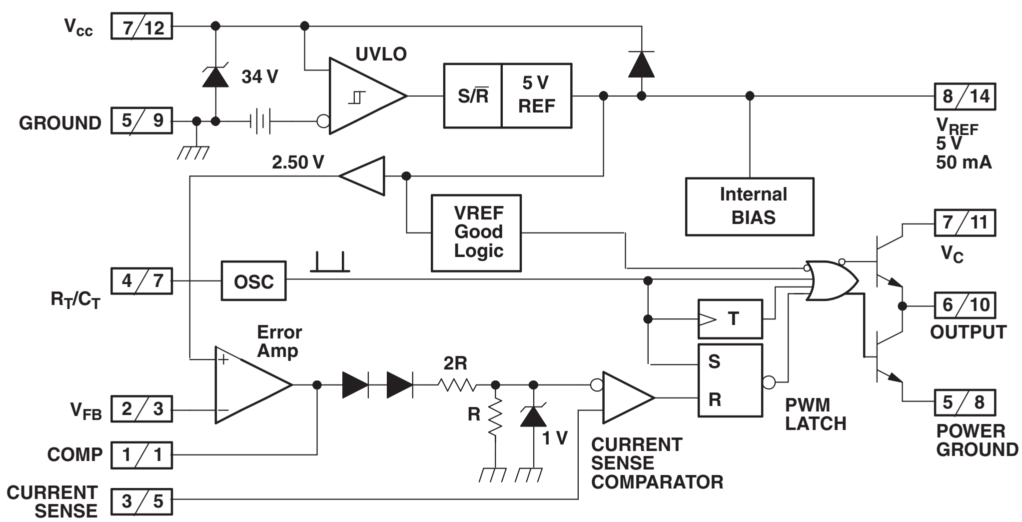
FEATURES

- **–55°C to 125°C Known Good Die**
- **Controlled Baseline**
- **Optimized For Off-line and DC-to-DC Converters**
- **Low Start-Up Current (<1 mA)**
- **Automatic Feed Forward Compensation**
- **Pulse-by-Pulse Current Limiting**
- **Enhanced Load Response Characteristics**
- **Under-Voltage Lockout With Hysteresis**
- **Double Pulse Suppression**
- **High Current Totem Pole Output**
- **Internally Trimmed Bandgap Reference**
- **500-kHz Operation**
- **Low R_O Error Amp**

DESCRIPTION

The UC1843 family of control devices provides the necessary features to implement off-line or dc-to-dc fixed frequency current mode control schemes with a minimal external parts count. Internally implemented circuits include under-voltage lockout featuring start up current less than 1 mA, a precision reference trimmed for accuracy at the error amp input, logic to insure latched operation, a PWM comparator which also provides current limit control, and a totem pole output stage designed to source or sink high peak current. The output stage, suitable for driving N-Channel MOSFETs, is low in the off state. The under-voltage lockout threshold is 8.4 V and maximum duty cycle range is around 100%.

BLOCK DIAGRAM



Note 1: A/B A = DIL–8 Pin Number B = SO–14 and CFP–14 Pin Number

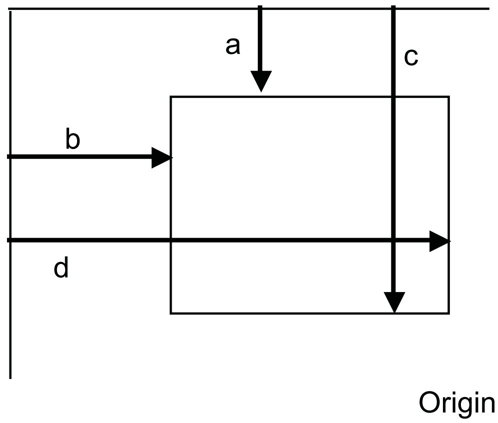
ORDERING INFORMATION(1)

T_A	PACKAGE(2)	ORDERABLE PART NUMBER	TOP-SIDE MARKING
–55°C to 125°C	KGD	UC1843KGD1	NA

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.
(2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.

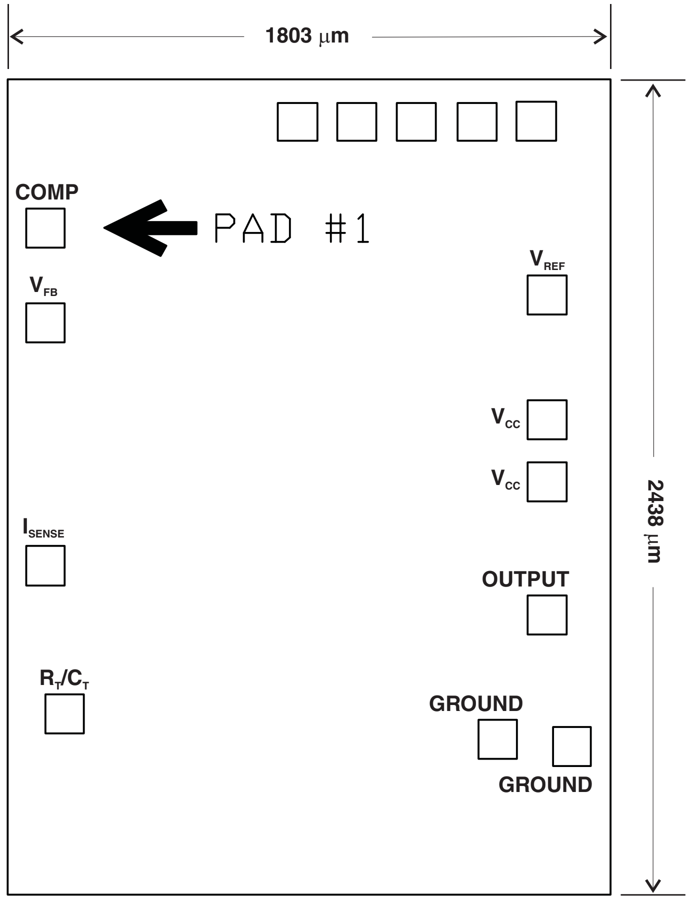
BARE DIE INFORMATION

DIE THICKNESS	BACKSIDE FINISH	BACKSIDE POTENTIAL	BOND PAD METALLIZATION COMPOSITION
15 mils.	Silicon with backgrind	GND	Al-Si-Cu (0.5%)



BOND PAD COORDINATES (in Mils)

DESCRIPTION	PAD NUMBER	a	b	c	d
COMP	1	78.70	63.40	82.90	67.60
V_{FB}	2	70.60	63.40	74.80	67.60
I_{SENSE}	3	39.40	63.40	43.60	67.60
R_T/C_T	4	18.60	61.20	22.60	65.60
GROUND	5	17.80	11.70	22.00	15.90
GROUND	6	17.40	3.90	21.80	8.10
OUTPUT	7	32.60	6.40	36.80	10.60
V_{CC}	8	47.50	6.40	51.70	10.60
V_{CC}	9	54.60	6.40	58.80	10.60
V_{REF}	10	68.70	6.40	72.90	10.60
NC	TESTPAD	87.10	6.30	90.80	10.30
NC	TESTPAD	87.10	12.60	90.80	16.60
NC	TESTPAD	87.10	18.00	90.80	22.00
NC	TESTPAD	87.10	24.30	90.80	28.30
NC	TESTPAD	87.10	30.60	90.80	34.60



ABSOLUTE MAXIMUM RATINGS

		UNIT
Supply voltage	Low impedance source	30 V
	I_{CC} < 30 mA	Self Limiting
Output current		±1 A
Output energy (capacitive load)		5 µJ
Analog inputs (Pins 2, 3)		–0.3 V to 6.3 V
Error amp output sink current		10 mA
Storage temperature range		–65°C to 150°C
Junction temperature range		–55°C to 150°C

ELECTRICAL CHARACTERISTICS

Unless otherwise stated, these specifications apply for –55°C ≤ T_A ≤ 125°C; V_{CC} = 15 V(1); R_T = 10 kW; C_T = 3.3 nF,T_A = T_J.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
REFERENCE SECTION					
Output Voltage	T_J = 25°C, I_O = 1 mA	4.95	5.00	5.05	V
Line Regulation	12 ≤ V_{IN} ≤ 25 V		6	20	mV
Load Regulation	1 ≤ I_0 ≤ 20 mA		6	25	mV
Temperature Stability	See (2)(3)		0.2	0.4	mV/°C
Total Output Variation	Line, load, tempature (2)	4.9		5.1	V
Output Noise Voltage	10 Hz≤ f ≤ 10 kHz, T_J = 25°C (2)		50		µV
Long Term Stability	T_A = 125°C, 1000 Hrs (2)		5	25	mV
Output Short Circuit		–30	–100	–180	mA
OSCILLATOR SECTION					
Initial Accuracy	T_J = 25°C(4)	47	52	57	kHz
Voltage Stability	12 ≤ V_{CC} ≤ 25 V		0.2%	1%	
Temperature Stability	T_{MIN} ≤ T_A ≤ T_{MAX} (2)		5%		
Amplitude	V_{PIN} 4 peak-to-peak (2)		1.7		V
ERROR AMP SECTION					
Input Voltage	$V_{PIN\ 1}$ = 2.5 V	2.45	2.50	2.55	V
Input Bias Current			–0.3	–1	µA
A_{VOL}	2 ≤ V_O ≤ 4 V	65	90		dB
Unity Gain Bandwidth	T_J = 25°C (2)	0.7	1		MHz
PSRR	12 ≤ V_{CC} ≤ 25 V	60	70		dB
Output Sink Current	$V_{PIN\ 2}$ = 2.7 V, $V_{PIN\ 1}$ = 1.1 V	2	6		mA
Output Source Current	$V_{PIN\ 2}$ = 2.3 V, $V_{PIN\ 1}$ = 5 V	–0.5	–0.8		mA
V_{OUT} High	$V_{PIN\ 2}$ = 2.3 V, R_L = 15 kΩ to ground	5	6		V
V_{OUT} Low	$V_{PIN\ 2}$ = 2.7 V, R_L = 15 kΩ to Pin 8		0.7	1.1	V
CURRENT SENSE SECTION					
Gain	See (5)(6)	2.85	3	3.15	V/V
Maximum Input Signal	$V_{PIN\ 1}$ = 5 V (5)	0.9	1	1.1	V
PSRR	12 ≤ V_{CC} ≤ 25 V (2)(5)		70		dB
Input Bias Current			–2	–10	µA
Delay to Output	$V_{PIN\ 3}$ = 0 V to 2 V (2)		150	300	ns
OUTPUT SECTION					
Output Low Level	I_{SINK} = 20 mA		0.1	0.4	V
	I_{SINK} = 200 mA		1.5	2.2	V
Output High Level	I_{SOURCE} = 20 mA	13	13.5		V
	I_{SOURCE} = 200 mA	12	13.5		V
Rise Time	T_J = 25°C, C_L = 1 nF (2)		50	150	ns
Fall Time	T_J = 25°C, C_L = 1nF(2)		50	150	ns

(1) Adjust V_{CC} above the start threshold before setting at 15 V.
(2) These parameters, although specified, are not 100% tested in production.
(3) Temperature stability, sometimes referred to as average temperature coefficient, is described by the equation:

$$\text{Temp Stability} = \frac{V_{REF}(\text{max}) - \text{VREF (min)}}{\text{TJ(max)} - \text{TJ (min)}}$$

$V_{REF(max)}$ and $V_{REF(min)}$ are the maximum and minimum reference voltages measured over the appropriate temperature range. Note that the extremes in voltage do not necessarily occur at the extremes in temperature.
(4) Output frequency equals oscillator frequency.
(5) Parameter measured at trip point of latch with $V_{PIN\ 2}$ = 0.
(6) Gain defined as: $A = \frac{\Delta\text{VPIN 1}}{\Delta\text{VPIN 3}},\ 0 \le \text{VPIN 3} \le 0.8\ \text{V}$

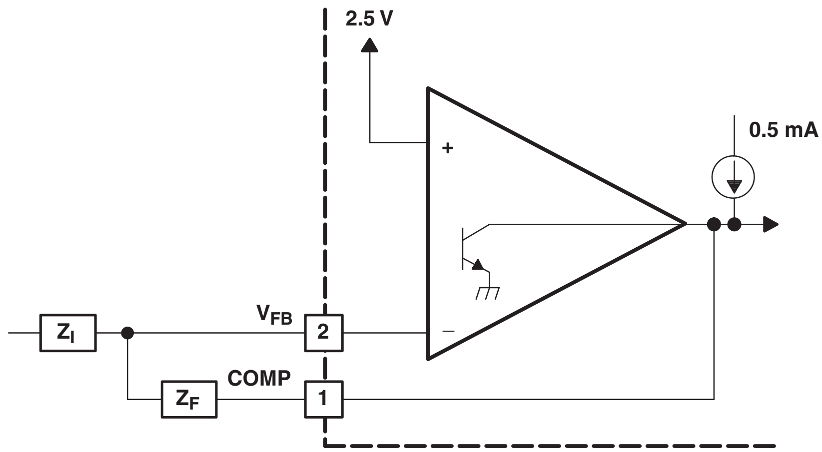
ELECTRICAL CHARACTERISTICS (continued)

Unless otherwise stated, these specifications apply for –55°C ≤ T_A ≤ 125°C; V_{CC} = 15 V; R_T = 10 kW; C_T = 3.3 nF,T_A = $T_{J.}$

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
UNDER-VOLTAGE LOCKOUT SECTION					
Start Threshold		7.8	8.4	9.0	V
Min. Operating Voltage After Turn On		7.0	7.6	8.2	
PWM SECTION					
Maximum Duty Cycle		95%	97%	100%	
Minimum Duty Cycle				0%	
TOTAL STANDBY CURRENT					
Start-Up Current			0.5	1	mA
Operating Supply Current	$V_{PIN\ 2}$ = $V_{PIN\ 3}$ = 0 V		11	17	
V_{CC} Zener Voltager	I_{CC} = 25 mA	30	34		V

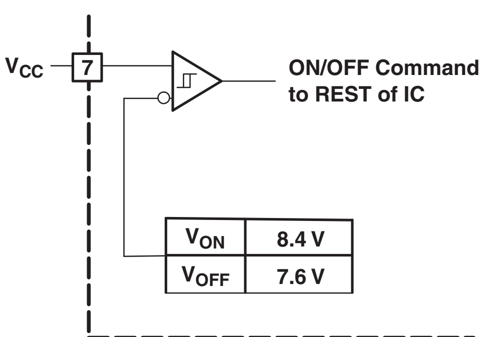
ERROR AMP CONFIGURATION

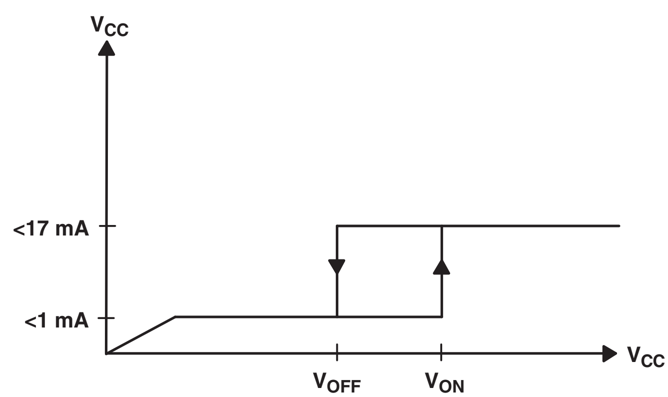
Error amp can source or sink up to 0.5 mA.



UNDER-VOLTAGE LOCKOUT

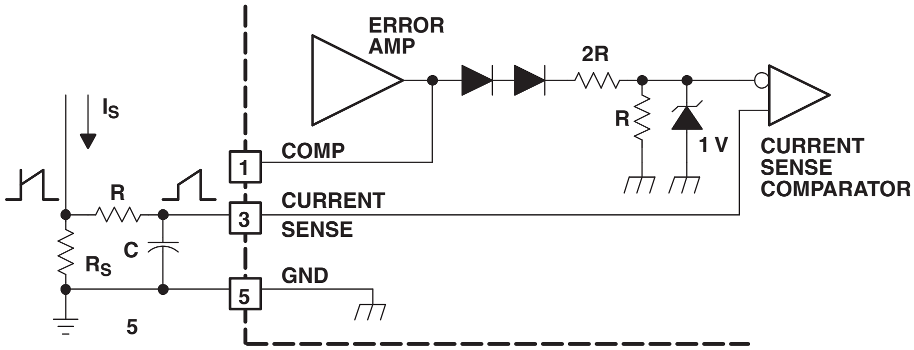
During under-voltage lock-out, the output drive is biased to sink minor amounts of current. Pin 6 should be shunted to ground with a bleeder resistor to prevent activating the power switch with extraneous leakage currents.





CURRENT SENSE CIRCUIT

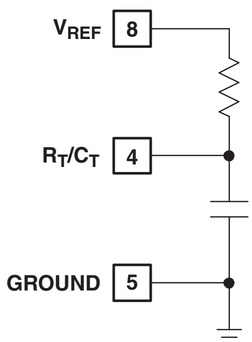
A small RC filter may be required to suppress switch transients.



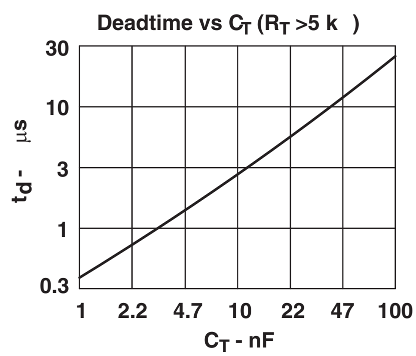
Peak Current (I_S) is Determined By The Formula

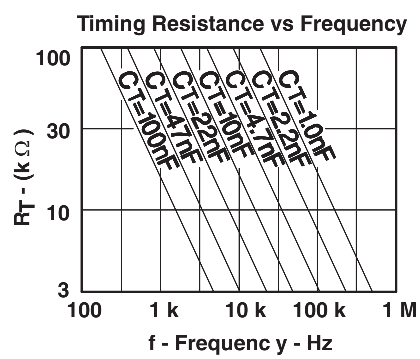
$$I_{SMAX} \approx \frac{1.0\,V}{RS}$$

OSCILLATOR SECTION

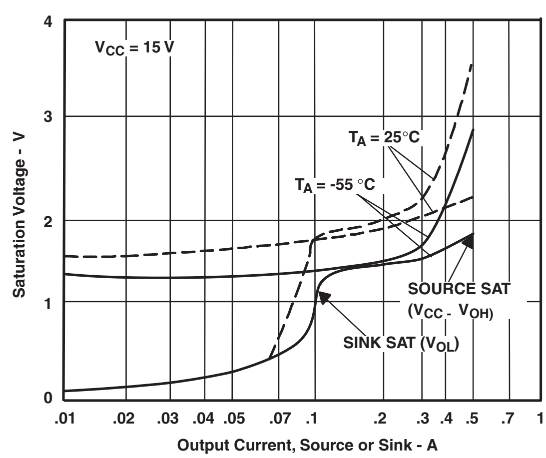


For $R_T > 5\,K$ $f \approx \frac{1.72}{R_T C_T}$

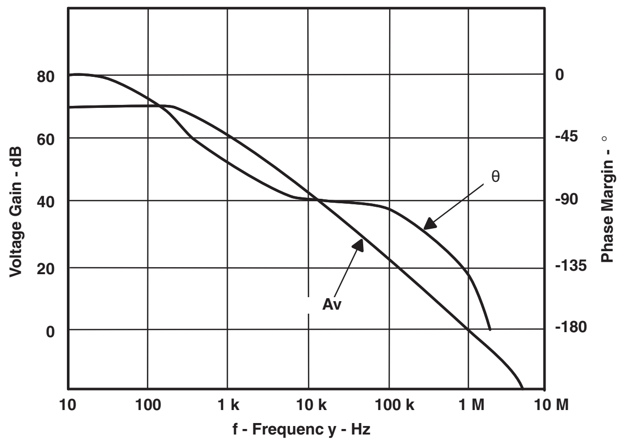




OUTPUT SATURATION CHARACTERISTICS

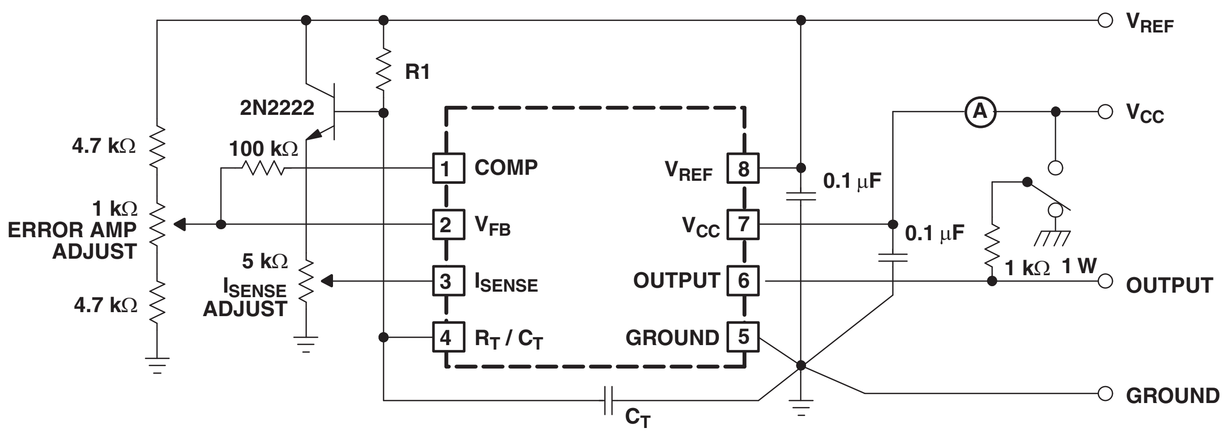


ERROR AMPLIFIER OPEN-LOOP FREQUENCY RESPONSE



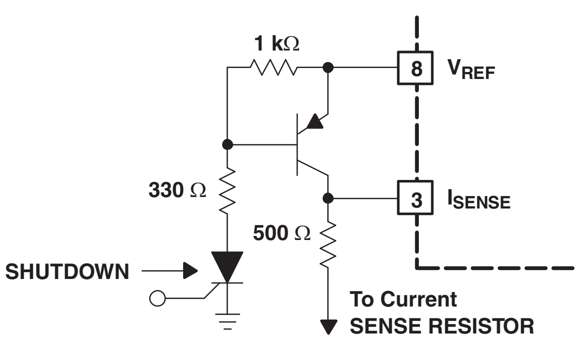
OPEN-LOOP LABORATORY FIXTURE

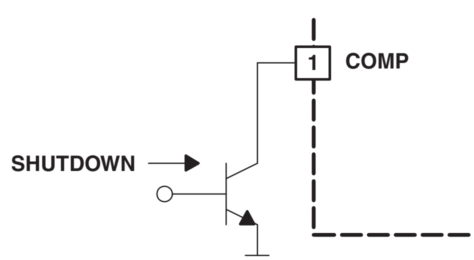
High peak currents associated with capacitive loads necessitate careful grounding techniques. Timing and bypas capacitors should be conected close to pin 5 in a single point ground. The transistor and 5k potentiometer are used to sample the oscillator waveform and apply an adjustable ramp to pin 3.



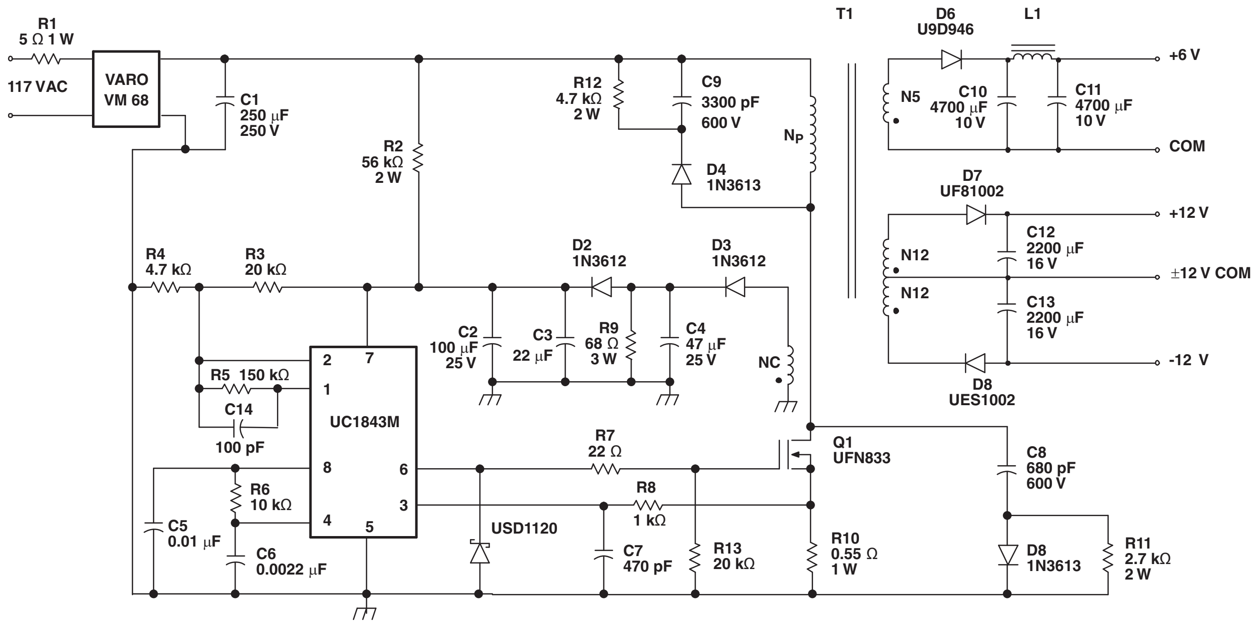
SHUTDOWN TECHNIQUES

Shutdown of the UC1843 can be accomplished by two methods; either raise pin 3 above 1 V or pull pin 1 below a voltage two diode drops above ground. Either method causses the output of the PWM comparator to be high (refer to block diagram). The PWM latch is reset dominant so that the output will remain low until the next clock cycle after the shutdown condition at pin 1 and/or 3 is removed. In one example, an externally latched shutdown may be accomplished by adding an SCR which will be reset by cycling V_{CC} below the lower UVLO threshold. At this pint the reference turns off, allowing the SCR to reset.





OFFLINE FLYBACK REGULATOR

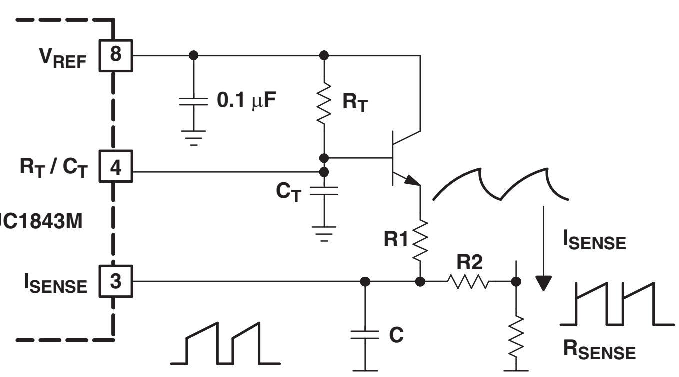


Power Supply Specifications

1. Input Voltages
   a. 5VAC to 130VA (50 Hz/60 Hz)
2. Line Isolation: 3750 V
3. Switchng Frequency: 40 kHz
4. Efficiency at Full Load 70%
5. Output Voltage:
   a. +5 V, ±5%; 1A to 4A load
      Ripple voltage: 50 mV P-P Max
   b. +12 V, ±3%; 0.1A to 0.3A load
      Ripple voltage: 100 mV P-P Max
   c. –12 V, ±3%; 0.1A to 0.3A load
      Ripple voltage: 100 mV P-P Max

SLOPE COMPENSATION

A fraction of the oscillator ramp can be resistively summed with the current sense signal to provide slope compensation for converters requiring duty cycles over 50%.



PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
UC1843MKGD1	ACTIVE	XCEPT	KGD	0	100	TBD	Call TI	N / A for Pkg Type	-55 to 125		Samples

[(1)] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[(2)] Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

[(3)] MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

[(4)] Only one of markings shown within the brackets will appear on the physical device.

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