

AM / FM - PLL

Description

The U4283BM is an integrated circuit in BICMOS technology for frequency synthesizer. It performs all the functions of a PLL radio tuning system and is controlled

by I²C bus. The device is designed for all frequency synthesizer applications of radio receivers, as well as RDS (Radio Data System) applications.

Features

- Reference oscillator up to 15 MHz
- Two programmable 16 bit dividers adjustable from 2 to 65535
- Fine tuning steps: AM \geq 1 kHz
FM \geq 2 kHz
- Three programmable switching outputs (open drain up to 20 V)
- Few external component requirements due to integrated loop-transistor for AM/FM
- High signal/ noise ratio

Block Diagram

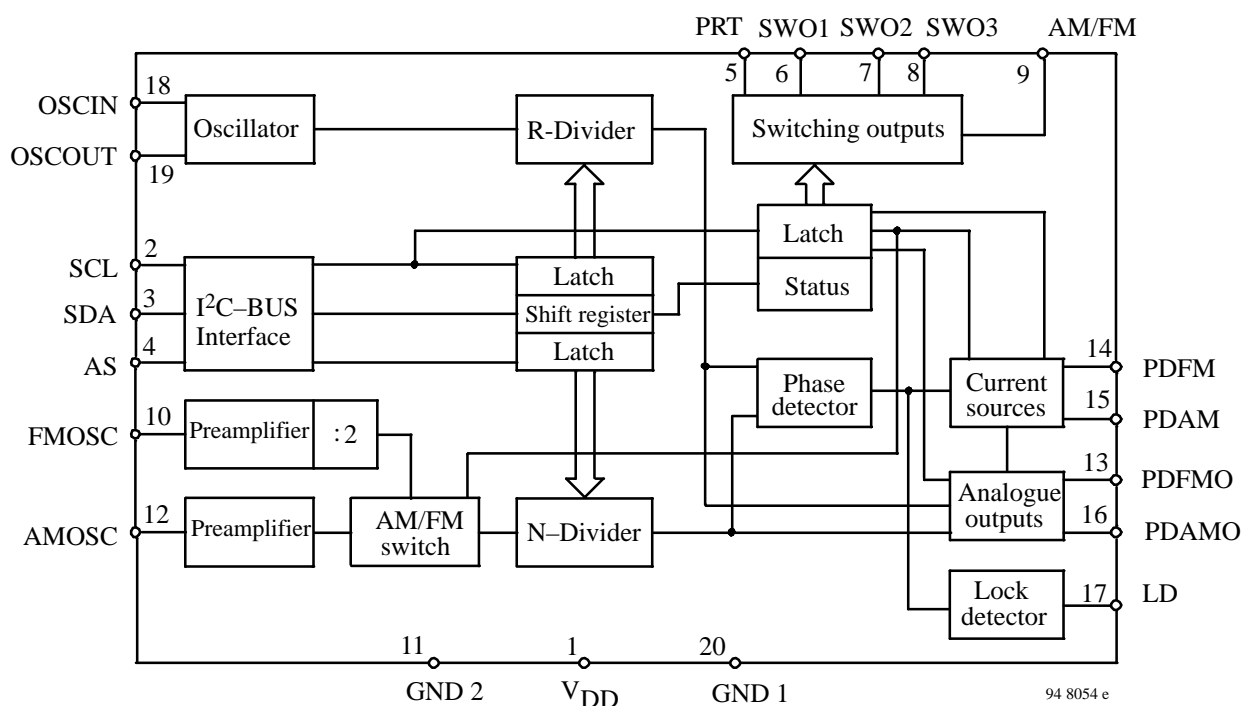
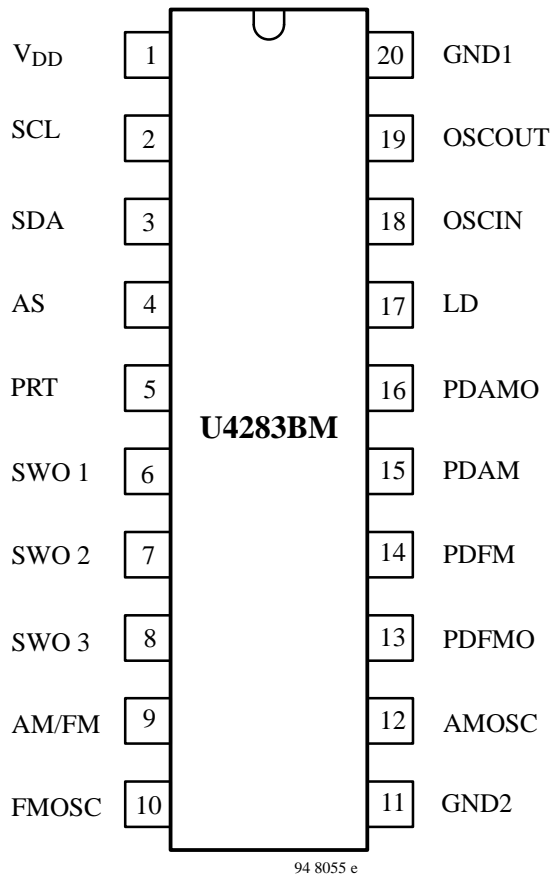


Figure 1.

Ordering and Package Information

Extended Type Number	Package	Remarks
U4283BM-BFL	SO20 plastic	
U4283BM-BFLG3	SO20 plastic	Taping according to IEC-286-3
U4283BM-BFS	SSO20 plastic	

Pin Description



Pin	Symbol	Function
1	V _{DD}	Supply voltage
2	SCL	I ² C bus clock
3	SDA	I ² C bus data
4	AS	Address selection
5	PRT	Switching port
6	SWO 1	Switching output 1
7	SWO 2	Switching output 2
8	SWO3	Switching output 3
9	AM/FM	Switching output AM/FM
10	FMOSC	FM oscillator input
11	GND 2	Ground 2 (analogue)
12	AMOSC	AM oscillator input
13	PDFMO	FM analogue output
14	PDFM	FM current output
15	PDAM	AM current output
16	PDAMO	AM analogue output
17	LD	Lock detector
18	OSCIN	Oscillator input
19	OSCOUT	Oscillator output
20	GND 1	Ground 1 (digital)

Functional Description

The U4283BM is controlled via the 2-wire I²C bus. For programming there are one module address byte, two subaddress bytes and five data bytes.

The module address contains a programmable address bit A 1 which with address select input AS (Pin 4) makes it possible to operate two U4283BM-B in one system. If bit A 1 is identical with the status of the address select input AS, the chip is selected.

The subaddress determines which one of the data bytes is transmitted first. If subaddress of R-divider is transmitted, the sequence of the next data bytes is DB 0 (Status), DB 1 and DB 2.

If subaddress of N-divider is transmitted, the sequence of the next data bytes is DB 3 and DB 4. The bit organisation of the module address, subaddress and 5 data bytes are shown in figure 2

Each transmission on the I²C bus begins with the "START"-condition and has to be ended by the "STOP"-condition (see figure 3).

The integrated circuit U 4283 BM has two separate inputs for AM and FM oscillator. Pre-amplified AM signal is directed to the 16 bit N-divider via AM/FM switch, whereas (pre-amplified) FM signal is first divided by a fixed prescaler (:2). AM/FM switch is controlled by software. Tuning steps can be selected by 16 bit R-divider. Further there is a digital memory phase detector. There are two separate current sources for AM and FM amplifier (charge pump) as given in electrical characteristics. It allows independent adjustment of gain, whereby providing high current for high speed tuning and low current for stable tuning.

Bit Organization

	MSB							LSB
Module address	1	1	0	0	1	0	0/1	0
	A7	A6	A5	A4	A3	A2	A1	A0

Subaddress (R-divider)	X	X	X	X	0	1	X	X
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Subaddress (N-divider)	X	X	X	X	1	1	X	X
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	MSB							LSB
Data byte 0 (Status)	PRT	SWO1	SWO2	SWO3	AM/ FM	PD ANA	PD POL	PD CUR
	D7	D6	D5	D4	D3	D2	D1	D0

Data byte 1	2^{15}	R-divider						2^8
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Data byte 2	2^7	R-divider						2^0
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Data byte 3	2^{15}	N-divider						2^8
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Data byte 4	2^7	N-divider						2^0
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	LOW	HIGH
AM/FM	FM-operation	AM-operation
PD - ANA	PD analog	TEST
PD - POL	Negative polarity	Positive polarity
PD - CUR	Output current 2	Output current 1

Figure 2.

Transmission Protocol

	MSB	LSB									
S	Address		A	Subaddress	A	Data 0	A	Data 1	A	Data 2	P
	A7	A0		R-divider							

	MSB	LSB							
S	Address		A	Subaddress	A	Data 3	A	Data 4	P
	A7	A0		N-divider				A	

S = Start P = Stop A = Acknowledge

Figure 3.

Absolute Maximum Ratings

Parameters	Symbol	Value	Unit
Supply voltage	Pin 1 V_{DD}	-0.3 to +6	V
Input voltage	Pins 2, 3, 4, 10, 12, 18 and 19 V_I	-0.3 to $V_{DD} + 0.3$	V
Output current	Pins 3, 5, 6, 7, 8 and 9 I_O	-1 to +5	mA
Output drain voltage	Pins 6, 7, 8 and 9 V_{OD}	20	V
Output voltage	Pins 13 and 16 V_{AO}	15	V
Output current	Pins 13 and 16 I_{AO}	-1 to +20	mA
Ambient temperature range	T_{amb}	-25 to +85	°C
Storage temperature range	T_{stg}	-40 to +125	°C
Junction temperature	T_j	125	°C
Electrostatic handling (MIL Standard 883C)	$\pm V_{ESD}$	2000	V

Thermal Resistance

Parameters	Symbol	Value	Unit
Junction ambient	R_{thJA}	160	K/W

Electrical Characteristics

$V_{DD} = 5\text{ V}$, $T_{amb} = 25^\circ\text{C}$, unless otherwise specified.

Parameters	Test Conditions / Pins	Symbol	Min.	Typ.	Max.	Unit
Supply voltage	Pin 1	V_{DD}	4.5	5.0	5.5	V
Quiescent supply current	Pin 1	I_{DD}		6.0	11.6	mA
FM input sensitivity, $R_G = 50\ \Omega$ FMOSC						
$f_i = 70$ to 120 MHz	Pin 10	V_{SFM}	25			mV
$f_i = 120$ to 130 MHz	Pin 10	V_{SFM}	50			mV
AM input sensitivity, $R_G = 50\ \Omega$ AMOSC						
$f_i = 0.5$ to 35 MHz	Pin 12	V_{SAM}	25			mV
Oscillator input sensitivity, $R_G = 50\ \Omega$ OSCIN						
$f_i = 0.1$ to 15 MHz	Pin 14	V_{SOSC}	100			mV
Switching output SWO 1, SWO 2, SWO3, AM/FM (open drain)						
Output voltage LOW	Pins 6, 7, 8 and 9 $I_L = 1\text{ mA}$	V_{SWOL}		200	400	mV
Output voltage LOW	$I_L = 0.1\text{ mA}$	V_{SWOL}		20	100	mV
Output leakage current HIGH	Pins 6, 7, 8 and 9 $V_5, V_6 = 20\text{ V}$	I_{OHL}			100	nA
Lock detector output (open drain)						
Output voltage LOW	$I = 3\text{ mA}$				0.4	V
Switching output PRT Pin 5						
Output voltage HIGH	$I_L = 1\text{ mA}$	V_{OH}	$V_{DD} - 0.4$			V
Output voltage LOW	$I_L = 1\text{ mA}$	V_{OL}			0.4	V
Output voltage LOW	$I_L = 0.1\text{ mA}$	V_{OL}			0.1	V
Phase detector PDFM						
Output current 1	Pin 14	$\pm I_{PDFM}$	400	500	600	μA
Output current 2	Pin 14	$\pm I_{PDFM}$	100	125	150	μA
Phase detector PDAM						
Output current 1	Pin 15	$\pm I_{PDAM}$	75	100	125	μA
Output current 2	Pin 15	$\pm I_{PDAM}$	20	25	30	μA
Analogue output PDFMO, PDAMO						
Saturation voltage	$I = 15\text{ mA}$ Pins 13 and 16	V_{sat}		270	400	mV
Leakage current	Pins 13 and 16	I_{LEAK}			1	μA
I²C bus SCL, SDA, AS						
Input voltage HIGH	Pins 2, 3 and 4	V_{iBUS}	3.0		V_{DD}	V
Input voltage LOW			0		1.5	V
Output voltage Acknowledge LOW	$I_{SDA} = 3\text{ mA}$ Pin 3	V_O			0.4	V
Clock frequency	Pin 2	f_{SCL}			100	kHz
Rise time SDA, SCL	Pins 2 and 3	t_r			1	μs

Parameters	Test Conditions / Pins	Symbol	Min.	Typ.	Max.	Unit
Fall time SDA, SCL	Pins 2 asn 3	t_f			300	ns
Period of SCL	Pin 2					
HIGH		t_H	4.0			μ s
LOW		t_L	4.7			μ s
Setup Time						
Start condition		t_{sSTA}	4.7			μ s
Data		t_{sDAT}	250			ns
Stop condition		t_{sSTOP}	4.7			μ s
Time the bus must be free before a new transmission can be started		t_{wSTA}	4.7			μ s
Hold time						
Start condition		t_{hSTA}	4.0			μ s
DATA		t_{hDAT}	0			μ s

Bus Timing

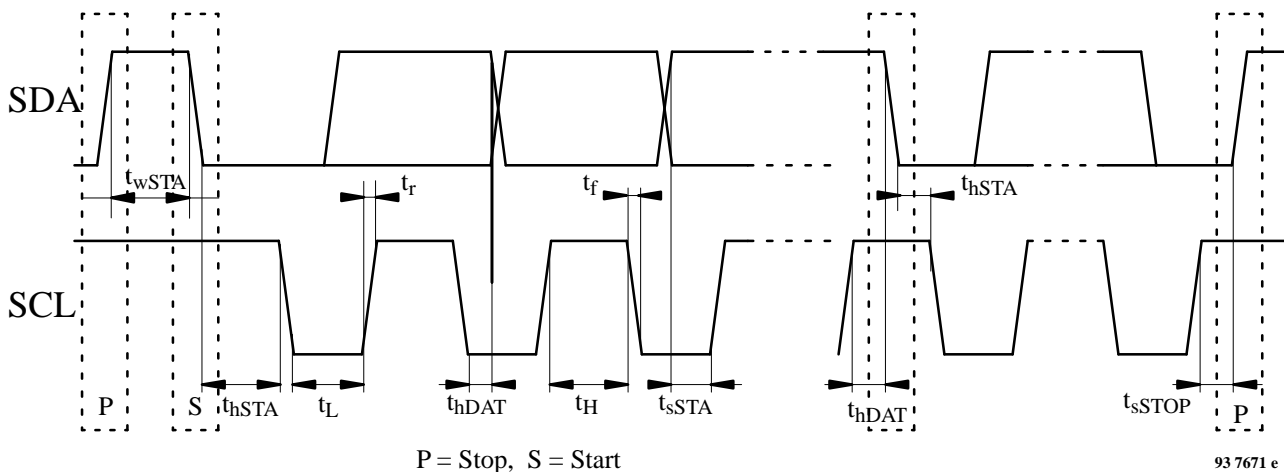


Figure 4.

The following hints are recommended:

- $C_3 = 100 \text{ nF}$ should be very close to Pin 1 (V_{DD}) and Pin 20 (GND1)
- 4 MHz quartz must be very close to Pin 18 and Pin 19
- Components of the charge pump (C_1/R_1 for AM and C_2/R_2 for FM) should be very close to Pin 15 with respect to Pin 14.
- GND2 (Pin 10 - analog ground) and GND 1 (Pin 20 - digital ground) must be connected according to figure 6

Application Circuit

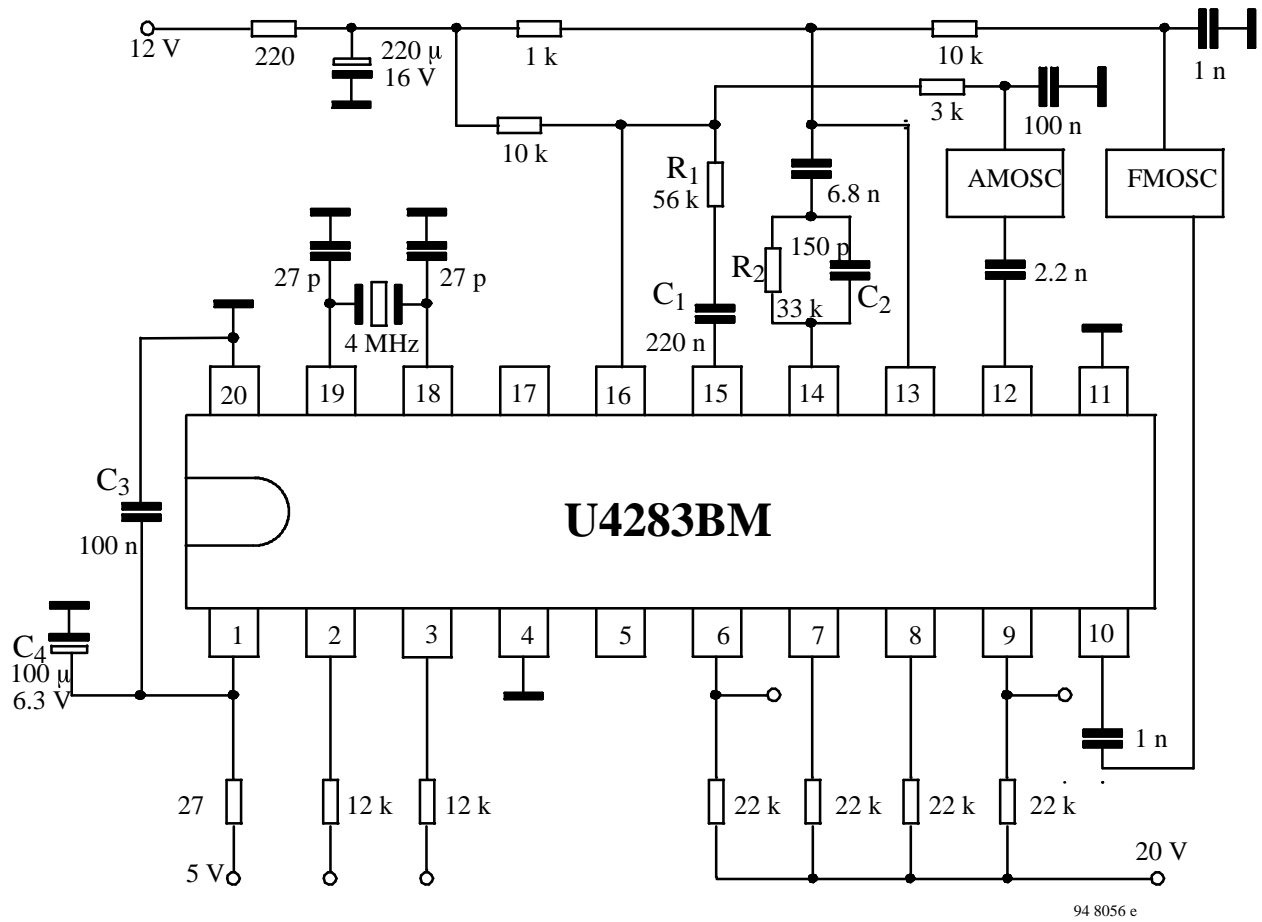


Figure 5.

PCB-Layout

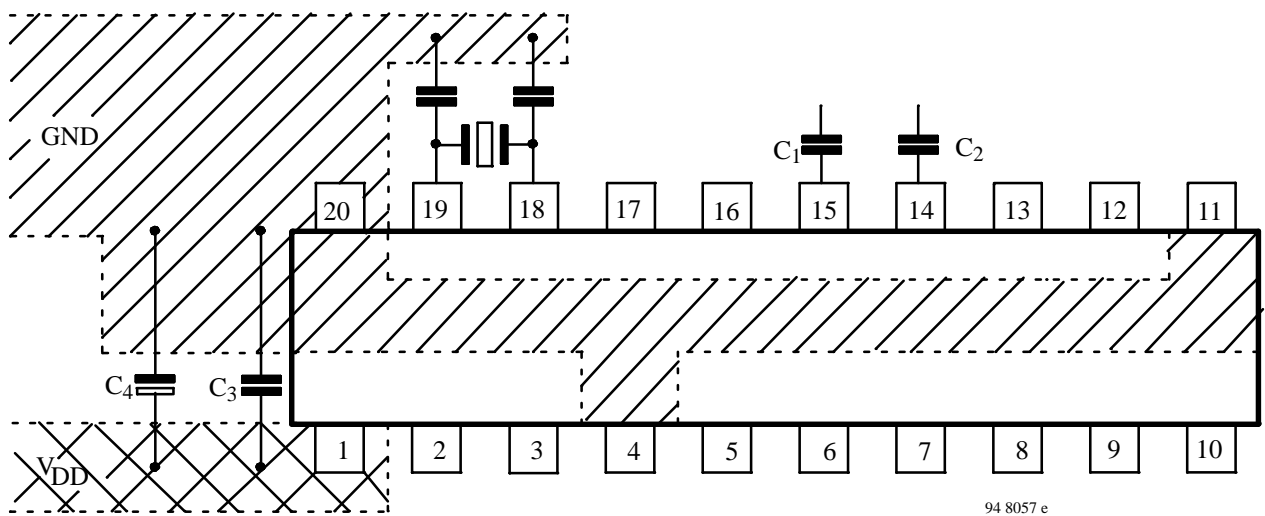
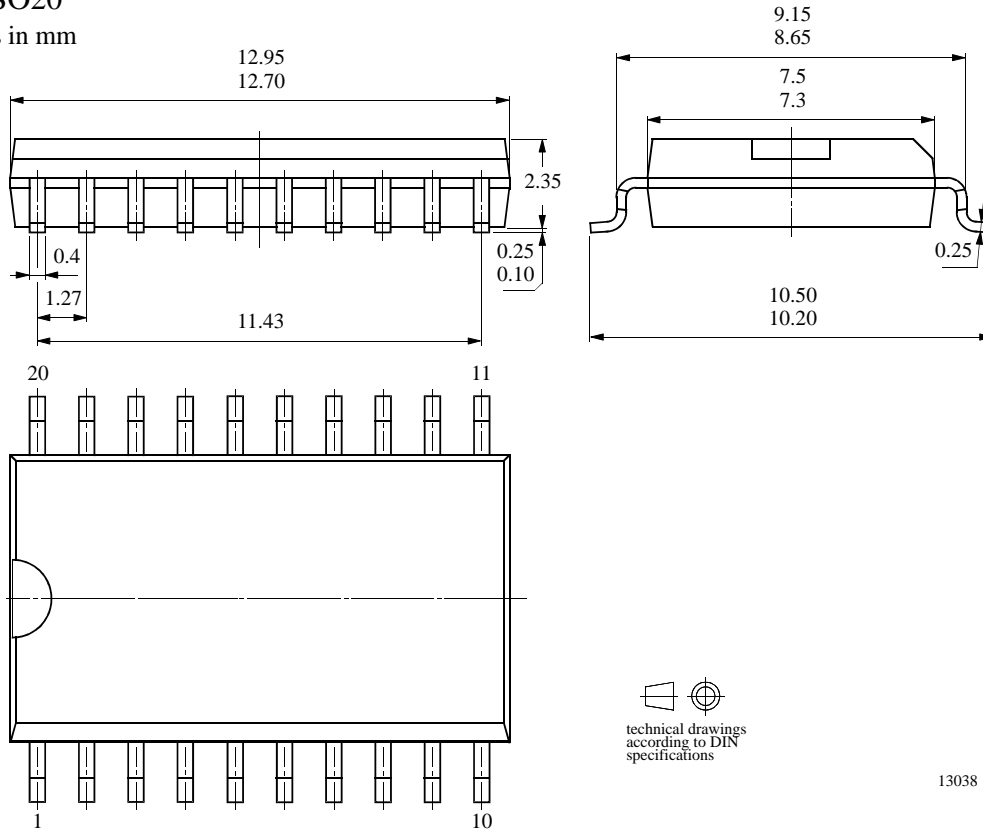


Figure 6.

Package Information

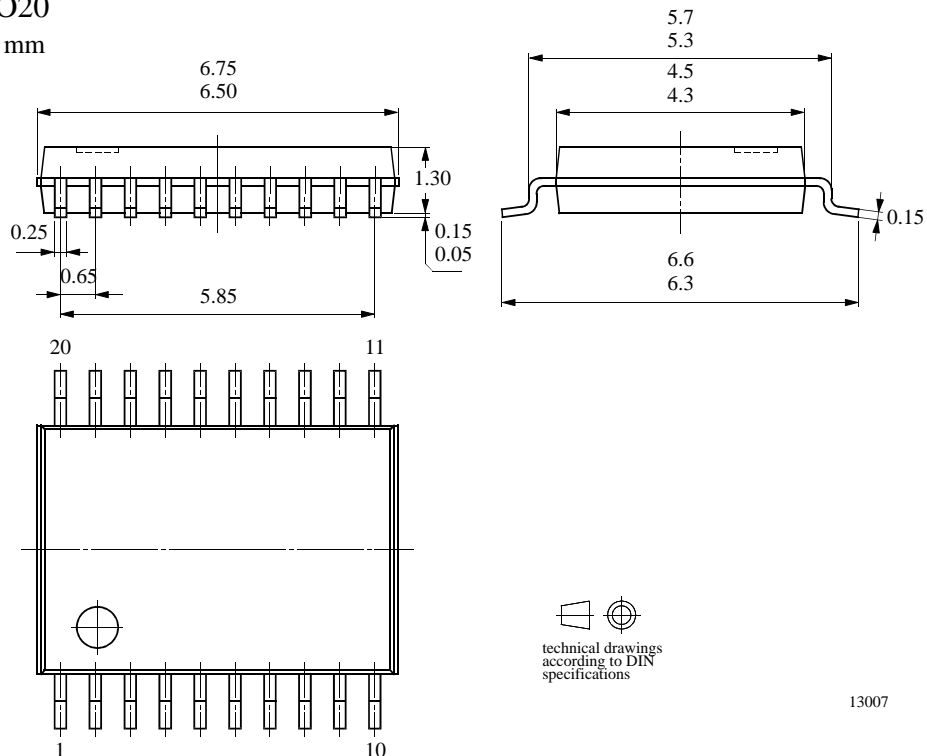
Package SO20

Dimensions in mm



Package SSO20

Dimensions in mm



Ozone Depleting Substances Policy Statement

It is the policy of **TEMIC TELEFUNKEN microelectronic GmbH** to

1. Meet all present and future national and international statutory requirements.
2. Regularly and continuously improve the performance of our products, processes, distribution and operating systems with respect to their impact on the health and safety of our employees and the public, as well as their impact on the environment.

It is particular concern to control or eliminate releases of those substances into the atmosphere which are known as ozone depleting substances (ODSs).

The Montreal Protocol (1987) and its London Amendments (1990) intend to severely restrict the use of ODSs and forbid their use within the next ten years. Various national and international initiatives are pressing for an earlier ban on these substances.

TEMIC TELEFUNKEN microelectronic GmbH semiconductor division has been able to use its policy of continuous improvements to eliminate the use of ODSs listed in the following documents.

1. Annex A, B and list of transitional substances of the Montreal Protocol and the London Amendments respectively
2. Class I and II ozone depleting substances in the Clean Air Act Amendments of 1990 by the Environmental Protection Agency (EPA) in the USA
3. Council Decision 88/540/EEC and 91/690/EEC Annex A, B and C (transitional substances) respectively.

TEMIC can certify that our semiconductors are not manufactured with ozone depleting substances and do not contain such substances.

We reserve the right to make changes to improve technical design and may do so without further notice.

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