DATA SHEET

TSA5522
1.4 GHz I²C-bus controlled synthesizer

Product specification
Supersedes data of 1995 Mar 22
File under Integrated Circuits, IC02

1996 Jan 23

Philips Semiconductors

PHILIPS

1.4 GHz I²C-bus controlled synthesizer TSA5522

FEATURES

- Complete 1.4 GHz single chip system
- Three PNP band switch buffers (20 mA)
- Four bus-controlled bidirectional ports (NPN open-collector outputs); only one port in 16-pin version
- 33 V tuning voltage output
- In-lock detector
- 5-step ADC
- Mixer-Oscillator (M/O) band switch output
- 15-bit programmable divider
- Programmable reference divider ratio (512, 640 or 1024)
- Programmable charge-pump current (50 or 250 μA)
- Varicap drive disable
- I²C-bus format
  - address plus 4 data bytes transmission (write mode)
  - address plus 1 status byte transmission (read mode)
  - three independent addresses
- Low power and low radiation.

APPLICATIONS

- TV tuners and front-ends
- VCR tuners.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TSA5522M	SSOP20	plastic shrink small outline package; 20 leads; body width 4.4 mm	SOT266-1
TSA5522T	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{CC1}	supply voltage (+5 V)		4.5	–	5.5	V
V_{CC2}	band switch supply voltage (+12 V)		V_{CC1}	12	13.5	V
I_{CC1}	supply current		–	22	30	mA
I_{CC2}	band switch supply current	note 1	–	27	32	mA
f_{RF}	RF input frequency		64	–	1400	MHz
$V_{i(RF)}$	RF input voltage	f_i = 80 to 150 MHz	– 25	–	3	dBm
		f_i = 150 to 1000 MHz	– 28	–	3	dBm
		f_i = 1000 to 1400 MHz	– 26	–	3	dBm
f_{xtal}	crystal oscillator input frequency		–	4	–	MHz
$I_{o(PNP)}$	PNP band switch buffers output current		–	20	25	mA
$I_{o(NPN)}$	NPN open-collector output current		–	20	25	mA
T_{amb}	operating ambient temperature		–20	–	+85	°C
T_{stg}	storage temperature (IC)		–40	–	+150	°C

Note

1. One band switch buffer ON; I_o = 20 mA.

GENERAL DESCRIPTION (see Fig.1)

The device is a single chip PLL frequency synthesizer designed for TV and VCR tuning systems. The circuit consists of a divide-by-eight prescaler with its own preamplifier, a 15-bit programmable divider, a crystal oscillator and its programmable reference divider and a phase/frequency detector combined with a charge-pump which drives the tuning amplifier, including 33 V output. Three high-current PNP band switch buffers are provided for band switching together with four open-collector NPN outputs (only one open-collector output on 16-pin devices). These ports can also be used as input ports [one Analog-to Digital Converter (ADC) and three general purpose I/O ports (not available on 16-pin devices)]. An output is provided to control a Philips mixer/oscillator IC in combination with the PNP buffers state.

Depending on the reference divider ratio (512, 640 or 1024), the phase comparator operates at 3.90625 kHz, 6.25 kHz or 7.8125 kHz with a 4 MHz crystal. The LOCK detector bit FL is set to logic 1 when the loop is locked and is read on the SDA line (status byte) during a read operation.

The ADC is available for digital AFC control. The ADC code is read during a read operation on the I²C-bus. The ADC input is combined with the port P6. In the TEST mode, this port is also used as a TEST output for f_{ref} and $\frac{1}{2}f_{div}$ (see Table 4).

I²C-bus format

Five serial bytes (including address byte) are required to address the device, select the VCO frequency, program the ports, set the charge-pump current and the reference divider ratio. The device has three independent I²C-bus addresses selected by applying a specific voltage on AS input (see Table 3). The general address C2 is always valid.

BLOCK DIAGRAM

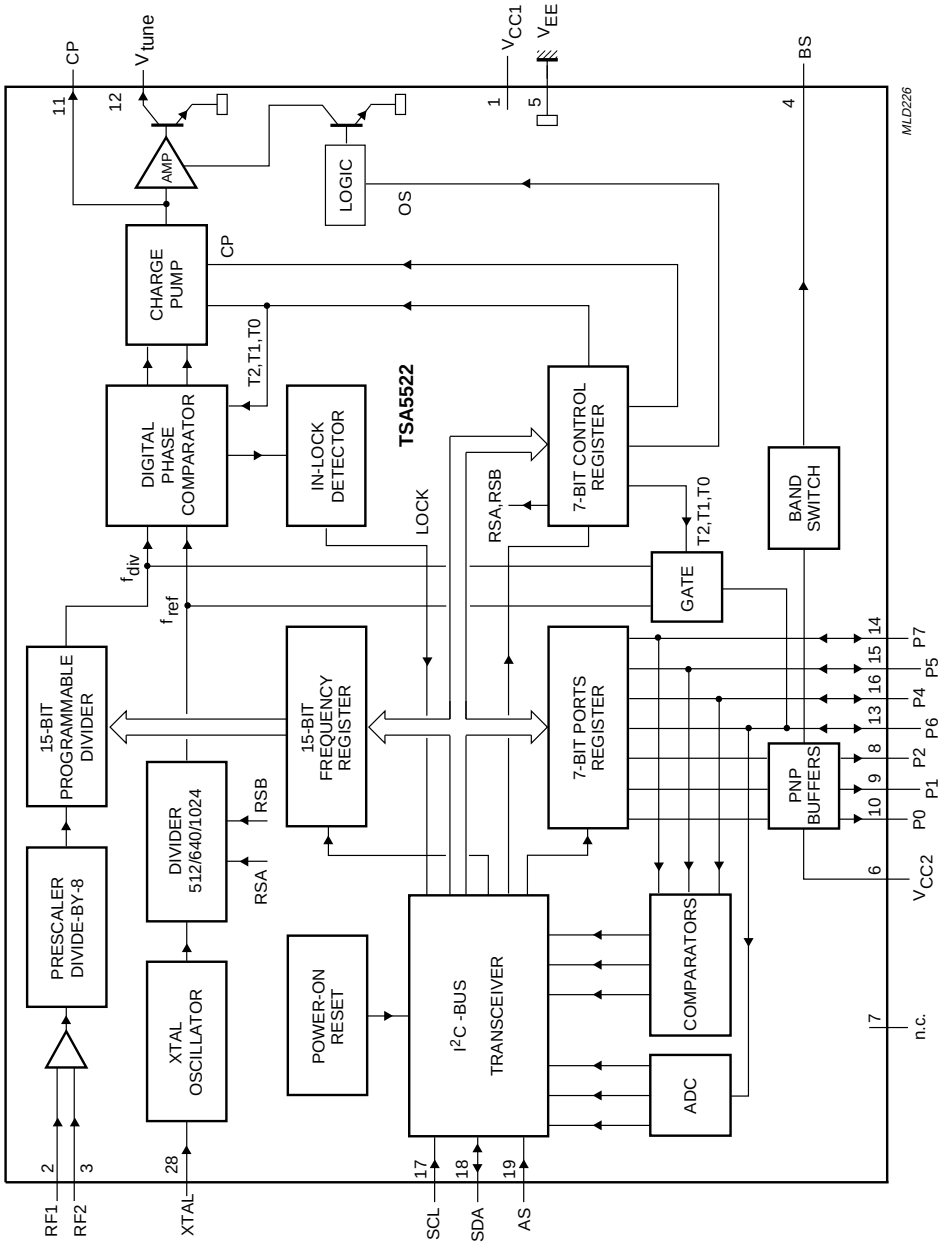


Fig.1 Block diagram (SSOP20).

PINNING

SYMBOL	SO16	SSOP20	DESCRIPTION
V_{CC1}	1	1	voltage supply (+5 V)
RF1	2	2	RF signal input 1
RF2	3	3	RF signal input 2
BS	4	4	band switch output to mixer/oscillator drive
V_{EE}	5	5	ground
V_{CC2}	6	6	voltage supply (+12 V)
n.c.	–	7	not connected
P2	7	8	PNP band switch buffer output 2
P1	8	9	PNP band switch buffer output 1
P0	9	10	PNP band switch buffer output 0
CP	10	11	charge-pump output
V_{tune}	11	12	tuning voltage output
P6	12	13	NPN open-collector output/ADC input
P7	–	14	NPN open-collector output/comparator input
P5	–	15	NPN open-collector output/comparator input
P4	–	16	NPN open-collector output/comparator input
SCL	13	17	serial clock input
SDA	14	18	serial data input/output
AS	15	19	address selection input
XTAL	16	20	crystal oscillator input

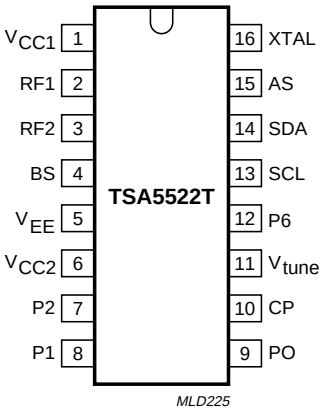


Fig.2 Pin configuration (SO16).

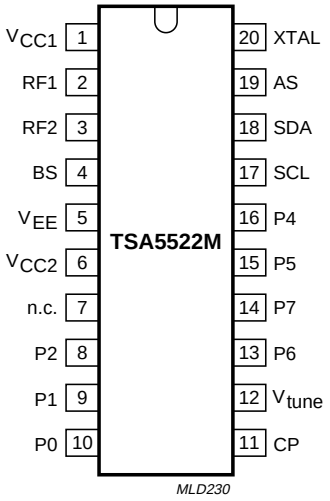


Fig.3 Pin configuration (SSOP20).

FUNCTIONAL DESCRIPTION

The device is controlled via the two-wire I²C-bus. For programming, there is one module address (7 bits) and the R/W bit for selecting the READ or the WRITE mode.

I²C-bus mode

WRITE MODE (R/W = 0); see Table 1

Data bytes can be sent to the device after the address transmission (first byte). Four data bytes are required to fully program the device. The bus transceiver has an auto-increment facility which permits the programming of the device within one single transmission (address + 4 data bytes).

The device can also be partially programmed providing that the first data byte following the address is divider byte 1 (DB1) or control byte (CB). The bits in the data bytes are defined in Table 1. The first bit of the first data byte transmitted indicates whether frequency data (first bit = 0) or control and ports data (first bit = 1) will follow. Until an I²C-bus STOP command is sent by the controller, additional data bytes can be entered without the need to re-address the device. The frequency register is loaded after the 8th clock pulse of the second divider byte (DB2), the control register is loaded after the 8th clock pulse of the control byte (CB) and the ports register is loaded after the 8th clock pulse of the ports byte (PB).

I²C-BUS ADDRESS SELECTION

The module address contains programmable address bits (MA1 and MA0) which offer the possibility of having several synthesizers (up to 3) in one system by applying a specific voltage on the AS input.

The relationship between MA1 and MA0 and the input voltage on the AS input is given in Table 3.

Table 1 I²C-bus data format

BYTE	MSB	DATA BYTE						LSB	COMMAND
Address byte (ADB)	1	1	0	0	0	MA1	MA0	0	A
Divider byte 1 (DB1)	0	N14	N13	N12	N11	N10	N9	N8	A
Divider byte 2 (DB2)	N7	N6	N5	N4	N3	N2	N1	N0	A
Control byte (CB)	1	CP	T2	T1	T0	RSA	RSB	OS	A
Ports byte (PB)	P7(1)	P6	P5(1)	P4(1)	X	P2	P1	P0	A

Note

1. Not available on 16-pin devices.

Table 2 Description of Table 1

SYMBOL	DESCRIPTION
MA1, MA0	programmable address bits (see Table 3)
N14 to N0	programmable divider bits $N = N14 \times 2^{14} + N13 \times 2^{13} + ... + N1 \times 2 + N0$
CP	charge-pump current; CP = 0 = 50 μA; CP = 1 = 250 μA
T2 to T0	test bits (see Table 4). For normal operation T2 = 0; T1 = 0; T0 = 1
RSA, RSB	reference divider ratio select bits (see Table 5)
OS	tuning amplifier control bit; for normal operation OS = 0 and tuning voltage is ON; when OS = 1 tuning voltage is OFF (high impedance)
P2 to P0	PNP band switch buffers control bits
P7 to P4	NPN open collector control bits when P_n = 0 output n is OFF; when P_n = 1 output n is ON
X	don't care

Table 3 Address selection

VOLTAGE APPLIED ON AS INPUT	MA1	MA2
0 to $0.1V_{CC1}$	0	0
Always valid	0	1
$0.4V_{CC1}$ to $0.6V_{CC1}$	1	0
$0.9V_{CC1}$ to V_{CC1}	1	1

Table 4 Test bits

T2	T1	T0	DEVICE OPERATION
0	0	1	normal mode
0	1	X	charge-pump is OFF
1	1	0	charge-pump is sinking current
1	1	1	charge-pump is sourcing current
1	0	0	f_{ref} is available at LOCK output
1	0	1	$\frac{1}{2}f_{div}$ is available at LOCK output

Table 5 Ratio select bits

RSA	RSB	REFERENCE DIVIDER
X	0	640
0	1	1024
1	1	512

Table 6 Band switch output levels

P2	P1	P0	VOLTAGE ON BS OUTPUT	PHILIPS M/O BAND
0	1	0	0.25 V	band A
1	0	0	$0.4V_{CC1}$	band B
0	0	1	$0.8V_{CC1}$	band C

READ MODE; R/W = 1 (see Table 7)

Data can be read from the device by setting the R/W bit to logic 1. After the slave address has been recognized, the device generates an acknowledge pulse and the first data byte (status byte) is transferred on the SDA line (MSB first). Data is valid on the SDA line during a HIGH level of the SCL clock signal. A second data byte can be read from the device if the microcontroller generates an acknowledge on the SDA line (master acknowledge). End of transmission will occur if no master acknowledge occurs. The device will then release the data line to allow the microcontroller to generate a STOP condition. When ports P4 to P7 are used as inputs, the corresponding bits **must** be logic 0 (high impedance state). The POR flag is set to logic 1 at power-on. The flag is reset when an end-of-data is detected by the device (end of a read sequence). Control of the loop is made possible with the in-lock flag (FL) which indicates when the loop is locked (FL = 1).

The bits I2, to I0 represent the status of the I/O ports P7, P5 and P4 respectively. A logic 0 indicates a LOW level and a logic 1 indicates a HIGH level (see “Characteristics”).

A built-in ADC is available at pin P6. This converter can be used to apply AFC information to the microcontroller from the IF section of the television. The relationship between the bits A2 to A0 is given in Table 8.

Table 7 READ data format

BYTE	MSB	DATA BYTE						LSB	COMMAND
Address byte (ADB)	1	1	0	0	0	MA1	MA0	1	A[1]
Status byte (SB)	POR[2]	FL[3]	I2[4]	I1[4]	I0[4]	A2[5]	A1[5]	A0[5]	–

Notes

1. A = acknowledge.
2. POR = power-on-reset (POR = 1 at power-on).
3. FL = in-lock flag (FL = 1 when loop is locked).
4. I2 to I0 = digital levels for I/O ports P7, P5 and P4 respectively.
5. A2 to A0 = digital outputs of the 5-level ADC.

Table 8 ADC levels

VOLTAGE APPLIED ON PORT P6(1)	A2	A1	A0
$0.6V_{CC1}$ to 13.5V	1	0	0
$0.45V_{CC1}$ to $0.6V_{CC1}$	0	1	1
$0.3V_{CC1}$ to $0.45V_{CC1}$	0	1	0
$0.15V_{CC1}$ to $0.3V_{CC1}$	0	0	1
0 to $0.15V_{CC1}$	0	0	0

Note

1. Accuracy is $0.02V_{CC1}$.

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	MIN.	MAX	UNIT
V_{CC1}	supply voltage +5 V	–0.3	6.0	V
V_{CC2}	supply voltage + 12 V	–0.3	16	V
$V_{i(RF)}$	prescaler input voltage	–0.3	V_{CC1}	V
$V_{o(BS)}$	band switch output voltage	–0.3	V_{CC1}	V
$V_{o(PNP)}$	PNP band switch buffer output voltage	– 0.3	V_{CC2}	V
$I_{o(PNP)}$	PNP band switch buffers output current	–1	25	mA
V_{NPN}	NPN open-collector output voltage	–0.3	16	V
I_{NPN}	NPN open-collector output current	–1	25	mA
$V_{o(CP)}$	charge-pump output voltage	–0.3	V_{CC1}	V
$V_{o(tune)}$	output tuning voltage	–0.3	35	V
$V_{i(SCL)}$	serial clock input voltage	–0.3	6.0	V
$V_{i/o(SDA)}$	serial data input/output voltage	–0.3	6.0	V
$I_{o(SDA)}$	serial data output current	–1	5	mA
$V_{i(AS)}$	address selection input voltage	–0.3	V_{CC1}	V
$V_{i(xtal)}$	crystal oscillator input voltage	–0.3	V_{CC1}	V
T_{stg}	storage temperature range (IC)	–40	+150	°C
T_j	maximum junction temperature	–	+150	°C
t_{sc}	short circuit time; every pin to V_{CC1} or GND	–	10	s

HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling bipolar devices. Every pin withstands the ESD test in accordance with *MIL-STD-883C* category B (2000 V). Every pin withstands the ESD test in accordance with Philips Semiconductors Machine Model 0 Ω, 200 pF (200 V).

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	MAX	UNIT
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient in free air		
	SO16	110	K/W
	SSOP20	120	K/W

CHARACTERISTICS

V_{CC1} = 4.5 to 5.5 V; V_{CC2} = V_{CC1} to 13.2 V; T_{amb} = –20 to 85 °C; unless otherwise specified; see note 1

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX	UNIT
V_{CC1}	supply voltage (+5 V)		4.5	–	5.5	V
V_{CC2}	supply voltage (+12 V)		V_{CC1}	–	13.5	V
I_{CC1}	supply current		–	22	30	mA
I_{CC2}	supply current	One band switch buffer is ON; I_{source} = 20 mA	–	27	32	mA
f_{RF}	RF input frequency		64	–	1400	MHz
DR	divider ratio	15-bit frequency word	256	–	32767	MHz
Crystal oscillator						
f_{xtal}	crystal oscillator input frequency	R_{xtal} = 25 to 300 Ω	3.2	4	4.48	MHz
Z_{xtal}	crystal oscillator input impedance (absolute value)	f_i = 4 MHz	600	1200	–	Ω
Prescaler						
$V_{i(RF)}$	RF input level	V_{CC1} = 4.5 to 5.5 V; see Fig.4; f_i = 80 to 150 MHz	–25	–	3	dB
		V_{CC1} = 4.5 to 5.5 V; see Fig.4; f_i = 150 to 1000 MHz	–28	–	3	dB
		V_{CC1} = 4.5 to 5.5 V; see Fig.4; f_i = 1000 to 1400 MHz	–26	–	3	dB
PNP band switch buffers outputs						
$\|I_{LO}\|$	output leakage current	V_{CC2} = 13.5 V; V_o = 0 V	–10	–	–	µA
$V_{o(sat)}$	output saturation voltage	I_{source} = 20 mA; note 1	-	0.2	0.5	V
NPN open-collector outputs P4, P5, P6 and P7; see note 2						
$\|I_{LO}\|$	output leakage current	V_{CC1} = 5.5 V; V_o = 13.5 V	–	–	10	µA
$V_{o(sat)}$	output saturation voltage	I_{sink} = 20 mA; note 3	–	0.2	0.5	V
C_{OL}	allowed capacitive loading on output pins	V_{OL} = 13.5 V			10	nF
Input ports P7, P5 and P4; see note 2						
V_{IL}	LOW level input voltage		–	–	1.5	V
V_{IH}	HIGH level input voltage		3	–	–	V
AS input (Address Selection)						
$I_{IH(AS)}$	HIGH level input current	V_{AS} = V_{CC1}	–	–	50	µA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX	UNIT
$I_{IL(AS)}$	LOW level input current	V_{AS} = 0 V	–50	–	–	µA
SCL and SDA inputs						
V_{IL}	LOW level input voltage		–	–	1.5	V
V_{IH}	HIGH level input voltage		3.0	–	5.5	V
I_{IH}	HIGH level input current	V_{IH} = 5.5 V; V_{CC1} = 0 V	–	–	10	µA
		V_{IH} = 5.5 V; V_{CC1} = 5.5 V	–	–	10	µA
I_{IL}	LOW level input current	V_{IL} = 0 V; V_{CC1} = 5.5 V	–10	–	–	µA
f_{clk}	input clock frequency		–	100	400	kHz
SDA output (I²C bus mode)						
I_{ILO}	output leakage current	V_O = 5.5 V	–	–	10	µA
V_o	output voltage	I_{sink} = 3 mA	–	–	0.4	µA
BS output (M/O band selection)						
$V_{o(BS)}$	output voltage	band A; I_{source} = 20 µA	–	0.25	0.5	V
		band B; I_{source} = 20 µA	$0.36V_{CC1}$	$0.4V_{CC1}$	$0.43V_{CC1}$	V
		band C; I_{source} = 20 µA	$0.7V_{CC1}$	$0.8V_{CC1}$	$0.9V_{CC1}$	V
		band C; I_{source} = 50 µA	3.1	–	–	V
Charge-pump output CP						
$\lvert I_{ICPH} \rvert$	HIGH charge pump current (absolute value)	CP = 1	–	250	–	µA
$\lvert I_{ICPL} \rvert$	LOW charge pump current (absolute value)	CP = 0	–	50	–	µA
$V_{o(CP)}$	output voltage	in-lock; T_{amb} = +25 °C	–	1.95	–	V
$I_{LI(off)}$	off-state leakage current	T2 = 0; T1 = 1	–5	1	15	nA
Tuning voltage output V_{tune}						
$I_{LO(off)}$	leakage current when switched-off	OS = 1; V_{tune} = 33 V	–	–	10	µA
V_o	output voltage when the loop is closed	OS = 0; T2 = 0; T1 = 0; T0 = 1; R_L = 27 k Ω; V_{tune} = 33 V	0.4	–	32.6	V
$V_{ripple(p-p)}$	acceptable ripple voltage on V_{CC1} (peak-to-peak value)	f_{ripple} = 300 Hz to 300 kHz	–	–	30	mV

Notes

1. A single PNP band switch buffer is ON.
2. P4, P5 and P7 I/O ports are not available in 16-pin package. In 20-pin package, when a port is active, the collector voltage must not exceed 6 V.
3. A single NPN open-collector output is ON.

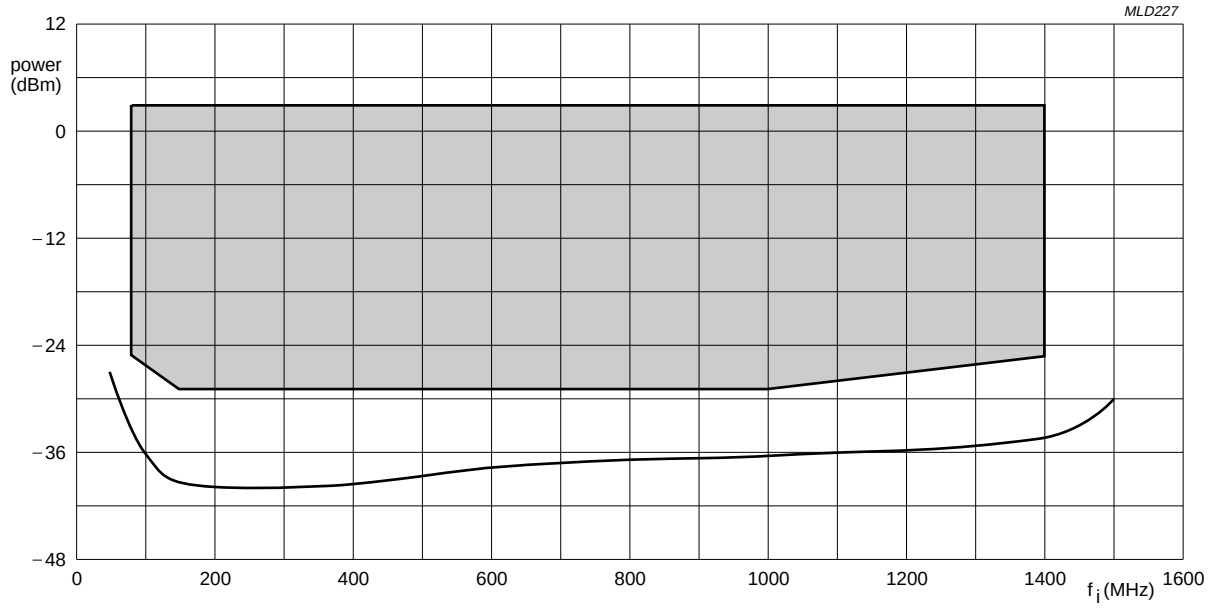


Fig.4 Prescaler typical input sensitivity curve.

INTERNAL PIN CONFIGURATION

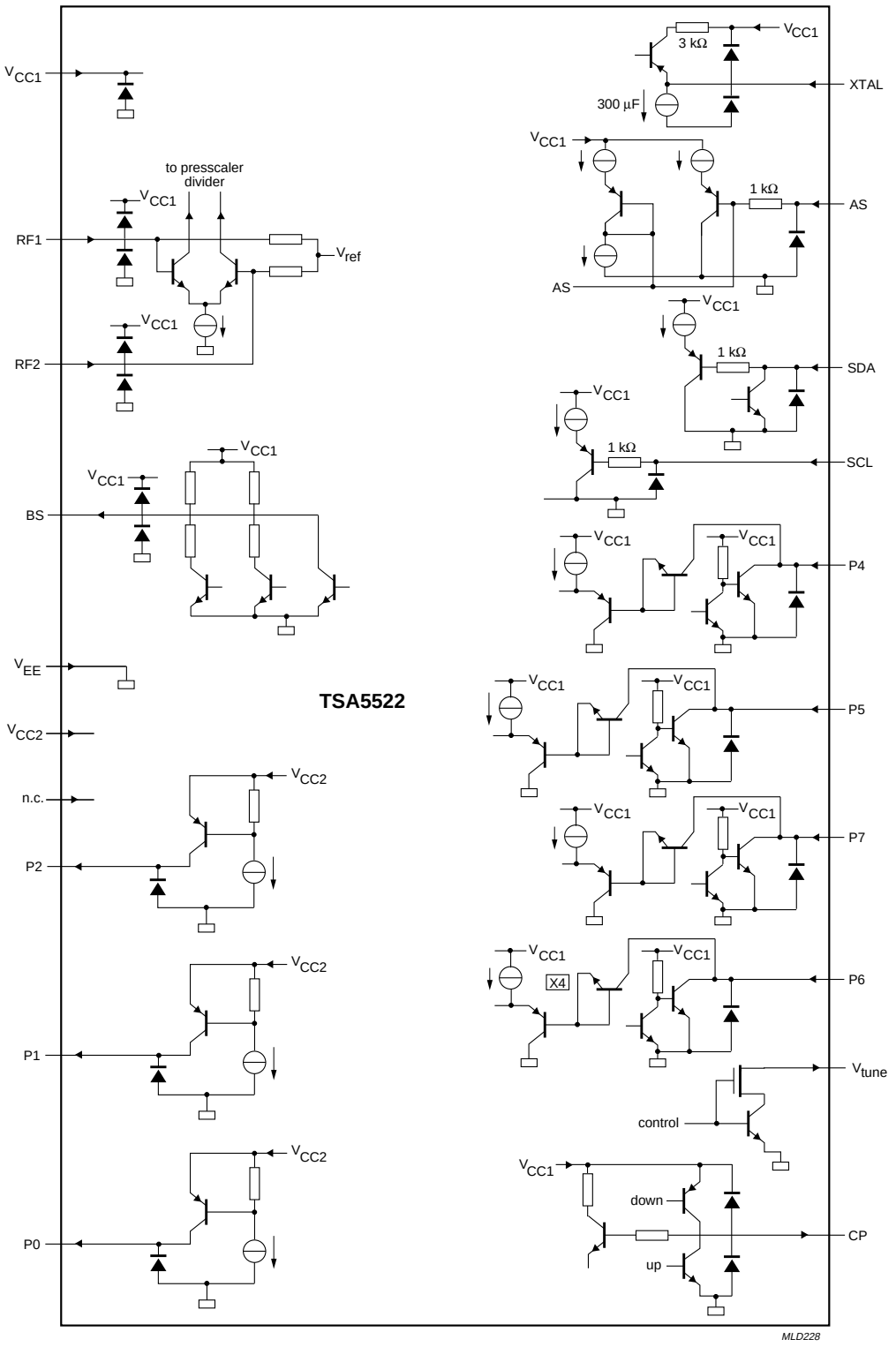


Fig.5 Internal pin configuration.

APPLICATION INFORMATION

Tuning amplifier

The tuning amplifier is capable of driving the varicap voltage without an external transistor. The tuning voltage output must be connected to an external load of 27 kΩ which is connected to the tuning voltage supply rail. Figure 6 shows a possible loop filter. The component values depend on the oscillator characteristics and the selected reference frequency.

Crystal oscillator

The crystal oscillator uses a 4 MHz crystal connected in series with an 18 pF capacitor thereby operating in the series resonance mode. Connecting the oscillator to the supply voltage is preferred, but it can, however, also be connected to ground.

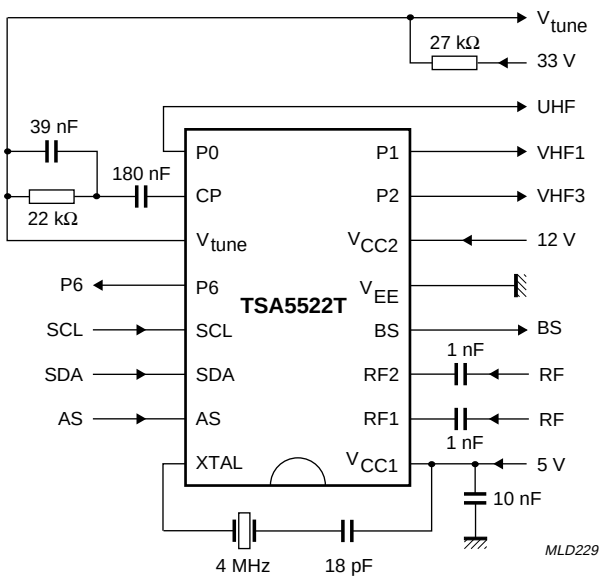


Fig.6 Typical application (SO16).

Flock flag (FL) definition

When the LOCK output is LOW the maximum frequency deviation (Δf) from stable frequency can be expressed as follows: $\Delta f = \pm\frac{K_{VCO}}{K_O} \times I_{CP} \times \frac{(C1 + C2)}{(C1 \times C2)}$

where:

K_{vco} = oscillator slope Hz/V

I_{CP} = charge-pump current (A)

$K_O = 4 \times 10E6$

C1, C2 = loop filter capacitors.

In the application:

K_{VCO} = 16 MHz/V (UHF band)

I_{CP} = 250 µA

C1 = 180 nF, C2 = 39 nF

$\Delta f = \pm 31.2$ kHz.

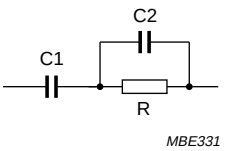


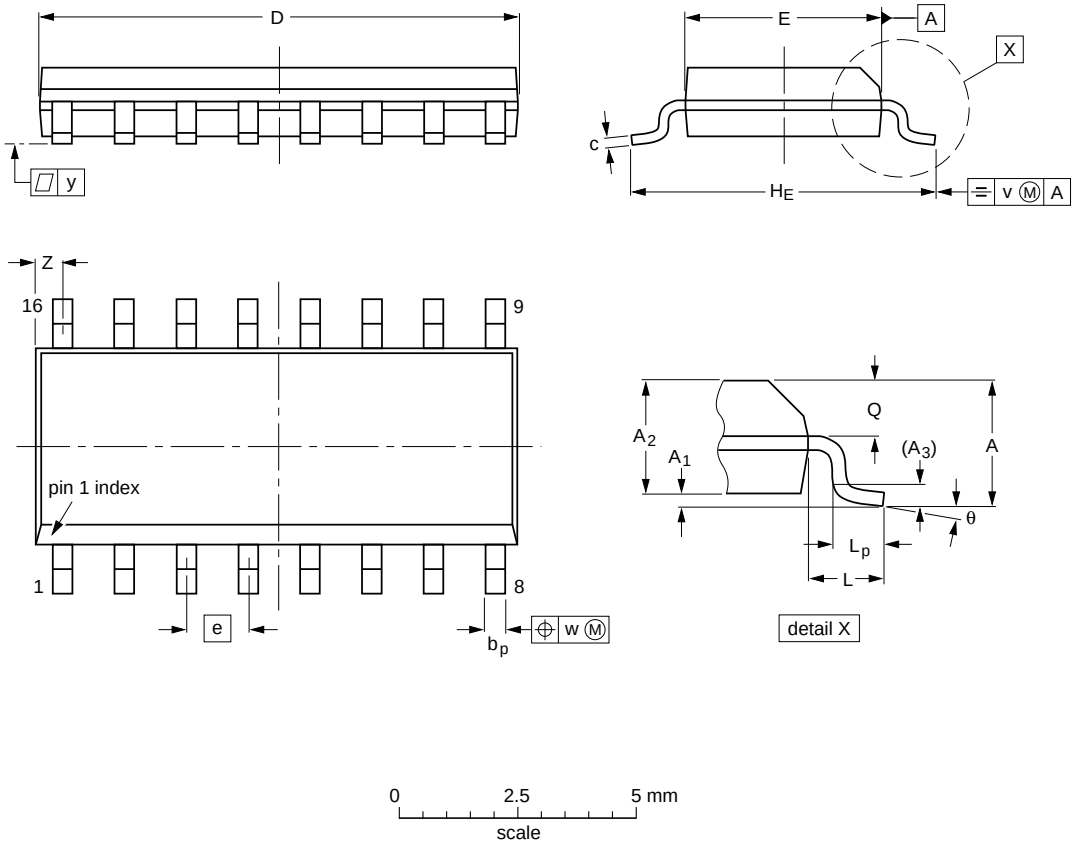
Fig.7 Loop filter.

Table 9 LOCK output / FL flag setting

DESCRIPTION	CONDITION	MIN.	MAX.	UNIT
Time span between actual phase lock and LOCK bit is LOW (or FL flag = 1)	RSA = 1; RSB = 1	1024	1152	µs
	RSA = 1; RSB = 1	2048	2304	µs
	RSB = 0	1280	1440	µs
Time span between the loop losing lock and LOCK bit is HIGH or (FL flag = 0)		0	300	µs

PACKAGE OUTLINES

SO16: plastic small outline package; 16 leads; body width 3.9 mm **SOT109-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

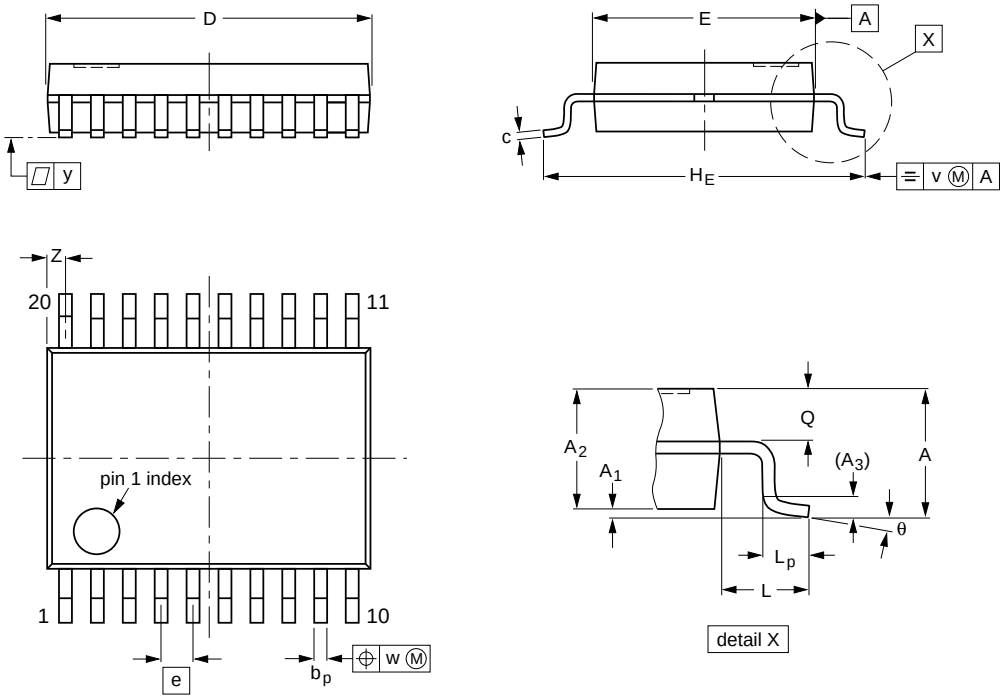
UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	10.0 9.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8^o 0^o
inches	0.069	0.0098 0.0039	0.057 0.049	0.01	0.019 0.014	0.0098 0.0075	0.39 0.38	0.16 0.15	0.050	0.24 0.23	0.041	0.039 0.016	0.028 0.020	0.01	0.01	0.004	0.028 0.012	

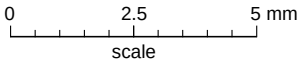
Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT109-1	076E07S	MS-012AC				~~91-08-13~~ 95-01-23

SSOP20: plastic shrink small outline package; 20 leads; body width 4.4 mm **SOT266-1**





DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.5	0.15 0	1.4 1.2	0.25	0.32 0.20	0.20 0.13	6.6 6.4	4.5 4.3	0.65	6.6 6.2	1.0	0.75 0.45	0.65 0.45	0.2	0.13	0.1	0.48 0.18	10^o 0^o

Note

1. Plastic or metal protrusions of 0.20 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES					EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ				
SOT266-1							~~90-04-05~~ 95-02-25

SOLDERING

Introduction

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these situations reflow soldering is often used.

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"IC Package Databook"* (order code 9398 652 90011).

Reflow soldering

Reflow soldering techniques are suitable for all SO and SSOP packages.

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several techniques exist for reflowing; for example, thermal conduction by heated belt. Dwell times vary between 50 and 300 seconds depending on heating method. Typical reflow temperatures range from 215 to 250 °C.

Preheating is necessary to dry the paste and evaporate the binding agent. Preheating duration: 45 minutes at 45 °C.

Wave soldering

SO

Wave soldering techniques can be used for all SO packages if the following conditions are observed:

- A double-wave (a turbulent wave with high upward pressure followed by a smooth laminar wave) soldering technique should be used.
- The longitudinal axis of the package footprint must be parallel to the solder flow.
- The package footprint must incorporate solder thieves at the downstream end.

SSOP

Wave soldering is **not** recommended for SSOP packages. This is because of the likelihood of solder bridging due to closely-spaced leads and the possibility of incomplete solder penetration in multi-lead devices.

If wave soldering cannot be avoided, the following conditions must be observed:

- **A double-wave (a turbulent wave with high upward pressure followed by a smooth laminar wave) soldering technique should be used.**
- **The longitudinal axis of the package footprint must be parallel to the solder flow and must incorporate solder thieves at the downstream end.**

Even with these conditions, only consider wave soldering SSOP packages that have a body width of 4.4 mm, that is SSOP16 (SOT369-1) or SSOP20 (SOT266-1).

METHOD (SO AND SSOP)

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Maximum permissible solder temperature is 260 °C, and maximum duration of package immersion in solder is 10 seconds, if cooled to less than 150 °C within 6 seconds. Typical dwell time is 4 seconds at 250 °C.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

Repairing soldered joints

Fix the component by first soldering two diagonally-opposite end leads. Use only a low voltage soldering iron (less than 24 V) applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C. When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

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