

3.5-MHz High Efficiency Step-Up Converter

 Check for Samples: [TPS61240](#), [TPS61241](#)

FEATURES

- Efficiency > 90% at Nominal Operating Conditions
- Total DC Output Voltage Accuracy 5.0V±2%
- Typical 30 μ A Quiescent Current
- *Best in Class* Line and Load Transient
- Wide V_{IN} Range From 2.3V to 5.5V
- Output current up to 450mA
- Automatic PFM/PWM Mode transition
- Low Ripple Power Save Mode for Improved Efficiency at Light Loads
- Internal Softstart, 250 μ s typical Start-Up time
- 3.5MHz Typical Operating Frequency
- Load Disconnect During Shutdown
- Current Overload and Thermal Shutdown Protection
- Three Surface-Mount External Components Required (One MLCC Inductor, Two Ceramic Capacitors)
- Total Solution Size <13 mm²
- Available in a 6-pin WCSP and 2×2-SON Package

APPLICATIONS

- USB-OTG Applications
- Portable HDMI Applications
- Cell Phones, Smart-Phones
- PDAs, Pocket PCs
- Portable Media Players
- Digital Cameras

DESCRIPTION

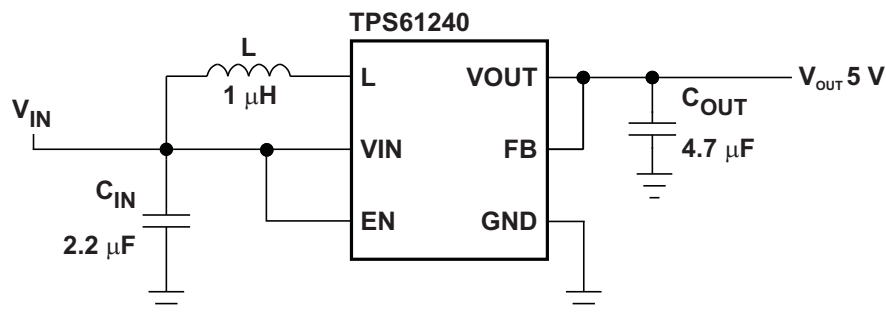
The TPS6124x device is a high efficient synchronous step up DC-DC converter optimized for products powered by either a three-cell alkaline, NiCd or NiMH, or one-cell Li-Ion or Li-Polymer battery. The TPS6124x supports output currents up to 450mA. The TPS61240 has an input valley current limit of 500mA, and the TPS61241 has an input valley current of 600mA.

With an input voltage range of 2.3V to 5.5V the device supports batteries with extended voltage range and are ideal to power portable applications like mobile phones and other portable equipment. The TPS6124x boost converter is based on a quasi-constant on-time valley current mode control scheme.

The TPS6124x presents a high impedance at the V_{OUT} pin when shut down. This allows for use in applications that require the regulated output bus to be driven by another supply while the TPS6124x is shut down.

During light loads the device will automatically pulse skip allowing maximum efficiency at lowest quiescent currents. In the shutdown mode, the current consumption is reduced to less than 1 μ A.

TPS6124x allows the use of small inductors and capacitors to achieve a small solution size. During shutdown, the load is completely disconnected from the battery. The TPS6124x is available in a 6-pin WCSP and 2×2 SON package.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

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These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ORDERING INFORMATION

| PART NUMBER ⁽¹⁾ | OUTPUT VOLTAGE | DEVICE SPECIFIC FEATURES | PACKAGE | ORDERING | PACKAGE MARKING |
|----------------------------|----------------|---|---------|-------------|-----------------|
| TPS61240 | 5V | | 6-WCSP | TPS61240YFF | GM |
| | | | 6-QFN | TPS61240DRV | OCJ |
| TPS61241 | | Supports 5V, up to 300mA loading down to 3.2V input voltage | 6-WCSP | TPS61241YFF | NF |
| TPS61242 ⁽²⁾ | | Optimized to drive an inductive load | 6-WCSP | TPS61242YFF | RY |

(1) The YFF package is available in tape on reel. Add R suffix (TPS61240YFFR) to order quantities of 3000 parts per reel. Add a T suffix (TPS61240YFFT) to order quantities of 250 parts.

(2) Product preview. [Contact TI factory for more information](#)

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)^{(1) (2)}

| | | VALUE | UNIT |
|---------------------------|---|--------------------|------|
| V_I | Input voltage range on V_{IN} , L, EN | -0.3 to 7 | V |
| | Voltage on V_{OUT} | -2.0 to 7 | V |
| | Voltage on FB | -2.0 to 14 | V |
| | Peak output current | Internally limited | A |
| ESD rating ⁽³⁾ | Human Body Model | 4000 | V |
| | CDM Charged Device Model | 500 | V |
| | Machine Model | 200 | V |
| T_J | Maximum operating junction temperature | -40 to 125 | °C |
| T_{stg} | Storage temperature range | -65 to 150 | °C |

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) All voltage values are with respect to network ground terminal.

(3) The human body model is a 100pF capacitor discharged through a 1.5 kΩ resistor into each pin. The machine model is a 200pF capacitor discharged directly into each pin.

DISSIPATION RATINGS TABLE⁽¹⁾

| PACKAGE | $R_{\theta JA}$ | POWER RATING $T_A \leq 25^\circ\text{C}$ | DERATING FACTOR ABOVE $T_A = 25^\circ\text{C}$ |
|---------|-----------------|---|---|
| DRV | 76°C/W | 1300mW | 13mW/°C |
| YFF | 125°C/W | 800mW | 8mW/°C |

(1) Maximum power dissipation is a function of $T_{J(max)}$, θ_{JA} and T_A . The maximum allowable power dissipation at any allowable ambient temperature is $P_D = [T_{J(max)} - T_A] / \theta_{JA}$.

(2) This thermal data is measured with high-K board (4 layer board according to JESD51-7 JEDEC standard).

RECOMMENDED OPERATING CONDITIONS

| | | MIN | NOM | MAX | UNIT |
|-----------------|--------------------------------|----------------------|-----|-----|------|
| V _{IN} | Input voltage range | 2.3 | | 5.5 | V |
| L | Inductance | 0.4 | 1 | 1.5 | μH |
| C _O | Output capacitance | TPS61240 TPS61241 | 1 | 20 | μF |
| | | TPS61242 | 0.8 | 10 | μF |
| T _A | Operating ambient temperature | –40 | | 85 | °C |
| T _J | Operating junction temperature | –40 | | 125 | °C |

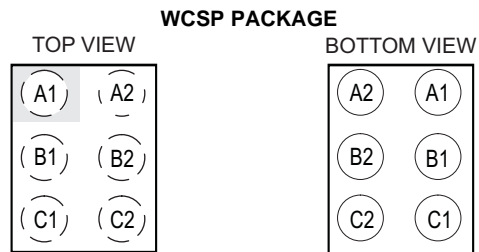
ELECTRICAL CHARACTERISTICS

Over full operating ambient temperature range, typical values are at T_A = 25°C. Unless otherwise noted, specifications apply for condition V_{IN} = EN = 3.6V. External components C_{IN} = 2.2μF, C_{OUT} = 4.7μF 0603, L = 1μH, refer to PARAMETER MEASUREMENT INFORMATION.

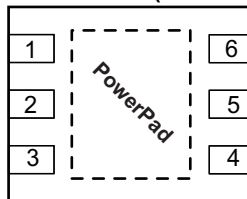
| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|-------------------------|--|---|------|-----|------|------|
| DC/DC STAGE | | | | | | |
| V _{IN} | Input voltage range | | 2.3 | | 5.5 | V |
| V _{OUT} | Fixed output voltage range | 2.3 V ≤ V _{IN} ≤ 5.5 V, 0 mA ≤ I _{OUT} ≤ 200 mA | 4.9 | 5.0 | 5.1 | V |
| V _{O_Ripple} | Ripple voltage, PWM mode | I _{LOAD} = 150 mA | | | 20 | mVpp |
| I _{SW} | Output current | V _{IN} 2.3 V to 5.5 V | 200 | | | mA |
| | Switch valley current limit | V _{OUT} = V _{GS} = 5.0 V (TPS61240) | 500 | 600 | | mA |
| | | V _{OUT} = V _{GS} = 5.0 V (TPS61241, TPS61242) | 600 | 700 | | mA |
| | Short circuit current | V _{OUT} = V _{GS} = 5.0 V | 200 | 350 | | mApk |
| | High side MOSFET on-resistance ⁽¹⁾ | V _{IN} = V _{GS} = 5.0V, T _A = 25°C ⁽¹⁾ | | 290 | | mΩ |
| | Low Side MOSFET on-resistance ⁽¹⁾ | V _{IN} = V _{GS} = 5.0 V, T _A = 25°C ⁽¹⁾ | | 250 | | mΩ |
| | Operating quiescent current | I _{OUT} = 0 mA, Power save mode | | 30 | 40 | μA |
| | Shutdown current | EN = GND | | | 1.5 | μA |
| | Reverse leakage current V _{OUT} | EN = 0, V _{OUT} = 5 V | | | 2.5 | μA |
| | Leakage current from battery to V _{OUT} | EN = GND | | | 2.5 | μA |
| | Line transient response | V _{IN} 600 mVp-p AC square wave, 200Hz, 12.5% DC at 50/200mA load | | ±25 | ±50 | mVpk |
| Load transient response | 0–50 mA, 50–0 mA V _{IN} = 3.6V T _{Rise} = T _{Fall} = 0.1μs | | 50 | | mVpk | |
| | 50–200 mA, 200–50 mA, V _{IN} = 3.6 V, T _{Rise} = T _{Fall} = 0.1μs | | 150 | | | |
| I _{IN} | Input bias current, EN | EN = GND or V _{IN} | 0.01 | 1.0 | | μA |
| V _{UVLO} | Undervoltage lockout threshold | Falling | | 2.0 | 2.1 | V |
| | | Rising | | 2.1 | 2.2 | V |
| CONTROL STAGE | | | | | | |
| V _{IH} | High level input voltage, EN | 2.3 V ≤ V _{IN} ≤ 5.5 V | | | 1.0 | V |
| V _{IL} | Low level input voltage, EN | 2.3 V ≤ V _{IN} ≤ 5.5 V | 0.4 | | | V |
| OVC | Input over-voltage threshold | Falling | | 5.9 | | V |
| | | Rising | | 6.0 | | |
| t _{Start} | Start-up time | Time from active EN to start switching, no-load until V _{OUT} is stable 5V | | | 300 | μs |
| DC/DC STAGE | | | | | | |
| Freq | | See Figure 7 (Frequency Dependency vs I _{OUT}) | | 3.5 | | MHz |
| T _{SD} | Thermal shutdown | Increasing junction temperature | | 140 | | °C |
| | Thermal shutdown hysteresis | Decreasing junction temperature | | 20 | | °C |

(1) DRV package has an increased R_{DSon} of about 40mΩ due to bond wire resistance.

PIN ASSIGNMENTS



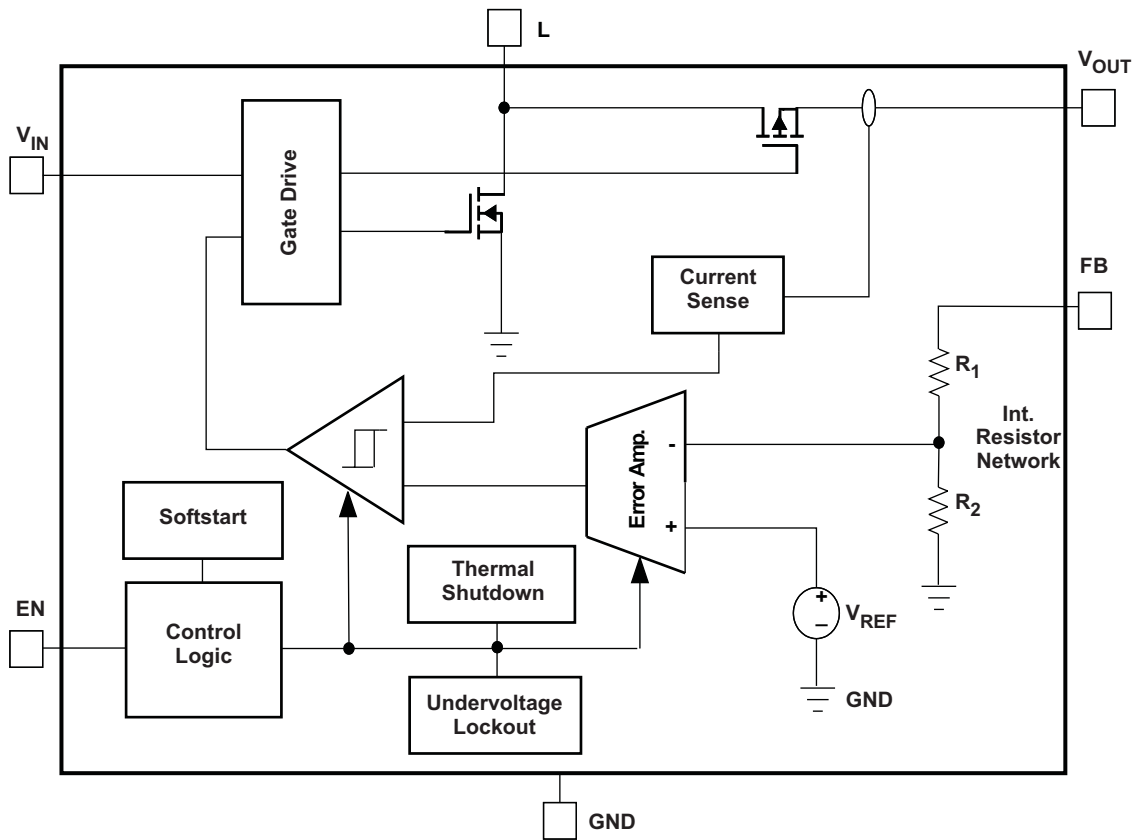
QFN PACKAGE (TOP VIEW)



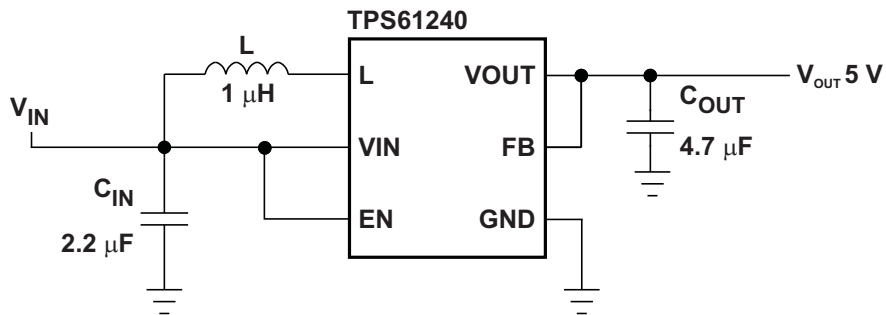
PIN FUNCTIONS

| PIN NO. | | PIN NAME | FUNCTION | REMARKS |
|---------|------|-----------|-----------------------------------|---------------------------------------|
| QFN | WCSP | | | |
| 2 | B2 | V_{OUT} | Output | Connected to load |
| 6 | A1 | V_{IN} | Supply voltage | Supply from battery |
| 5 | B1 | L | Boost and rectifying switch input | Inductor connection to FETs |
| 4 | C1 | EN | Enable | Positive polarity. Low = IC shutdown. |
| 3 | C2 | FB | Feedback input | Feedback for regulation. |
| 1 | A2 | GND | Ground | Power ground and IC ground |

FUNCTIONAL BLOCK DIAGRAM



PARAMETER MEASUREMENT INFORMATION



List of Components

| COMPONENT REFERENCE | PART NUMBER | MANUFACTURER | VALUE |
|---------------------|-----------------|--------------|--------------------------|
| C _{IN} | JMK105BJ225MV | Taiyo Yuden | 2.2 μF, X5R, 6.3 V, 0402 |
| C _{OUT} | JDK105BJ475MV | Taiyo Yuden | 4.7 μF, X5R, 6.3 V, 0402 |
| L | MDT2012-CH1R0AN | TOKO | 1.0 μH, 900mA, 0805 |

TYPICAL CHARACTERISTICS

Table of Graphs

Table 1.

| | | Figure |
|------------------------|--|--------|
| Maximum Output Current | vs Input Voltage | 1 |
| Efficiency | vs Output Current, $V_{out} = 5V$, $V_{in} = [2.3V; 3.0V; 3.6V; 4.2V]$ | 2 |
| | vs Input Voltage, $V_{out} = 5V$, $I_{out} = [100\mu A; 1mA; 10mA; 100mA; 200mA]$ | 3 |
| Input Current | at No Output Load, Device Disabled | 4 |
| Output Voltage | vs Output Current, $V_{out} = 5V$, $V_{in} = [2.3V; 3.0V; 3.6V; 4.2V]$ | 5 |
| | vs Input Voltage | 6 |
| Frequency | vs Output Load, $V_{out} = 5V$, $V_{in} = [3.0V; 4.0V; 5.0V]$ | 7 |
| Waveforms | Output Voltage Ripple, PFM Mode, $I_{out} = 10mA$ | 8 |
| | Output Voltage Ripple, PWM Mode, $I_{out} = 150mA$ | 9 |
| | Load Transient Response, $V_{in} = 3.6V$, 0 - 50mA | 10 |
| | Load Transient Response, $V_{in} = 3.6V$, 50 - 200mA | 11 |
| | Line Transient Response, $V_{in} = 3.6V - 4.2V$, $I_{out} = 50mA$ | 12 |
| | Line Transient Response, $V_{in} = 3.6V - 4.2V$, $I_{out} = 200mA$ | 13 |
| | Startup after Enable, $V_{in} = 3.6V$, $V_{out} = 5V$, Load = 5K Ω | 14 |
| | Startup after Enable, $V_{in} = 3.6V$, $V_{out} = 5V$, Load = 16.5 Ω | 15 |
| | Startup and Shutdown, $V_{in} = 3.6V$, $V_{out} = 5V$, Load = 16.5 Ω | 16 |

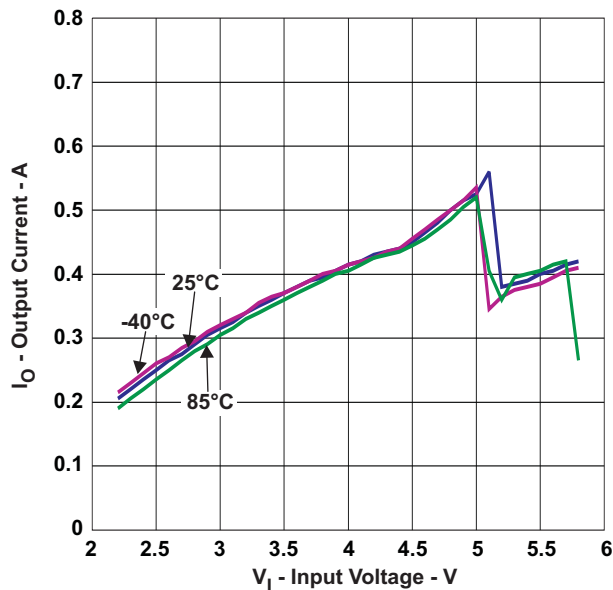


Figure 1. Maximum Output Current vs Input Voltage

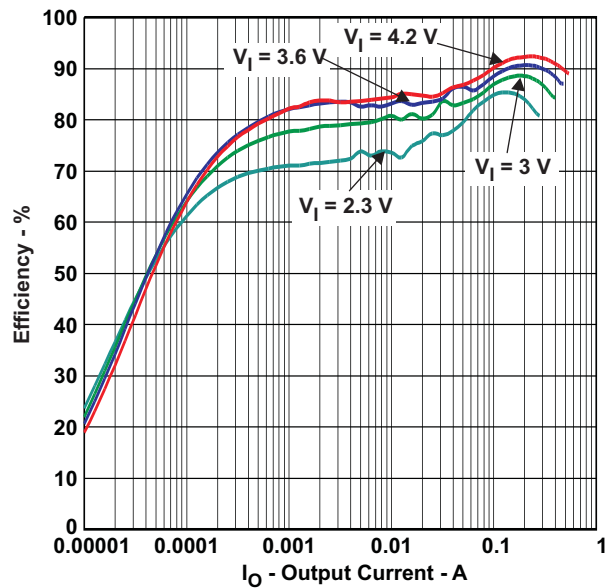


Figure 2. Efficiency vs Output Current

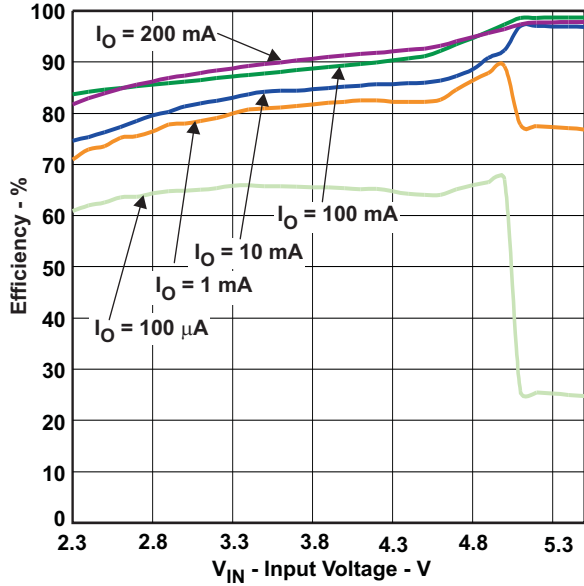


Figure 3. Efficiency vs Input Voltage

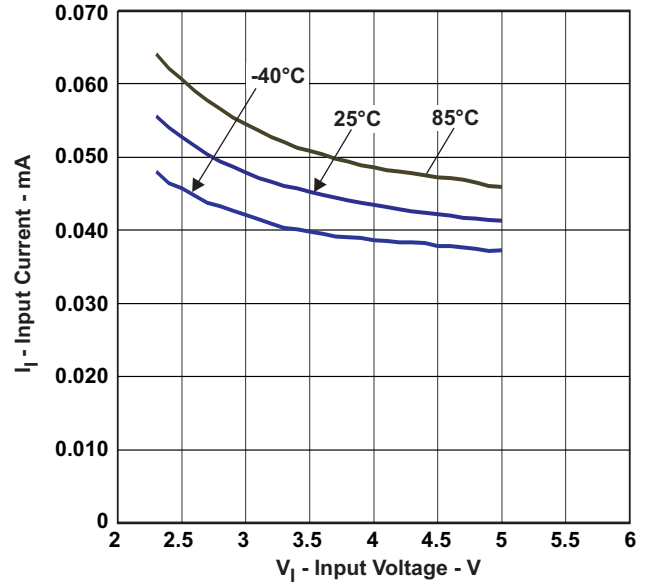


Figure 4. Input at No Output Load

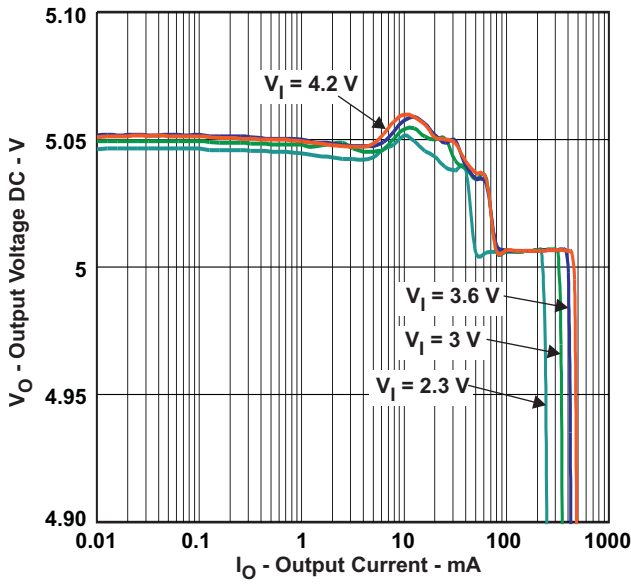


Figure 5. Output Voltage vs Output Current

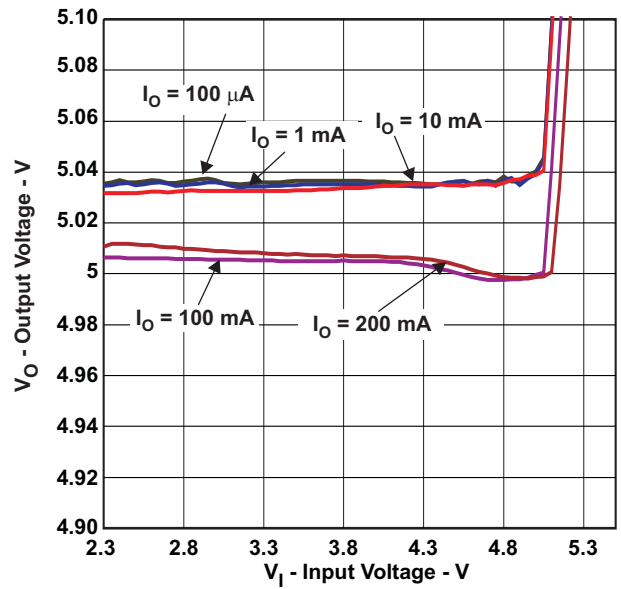


Figure 6. Output Voltage vs Input Voltage

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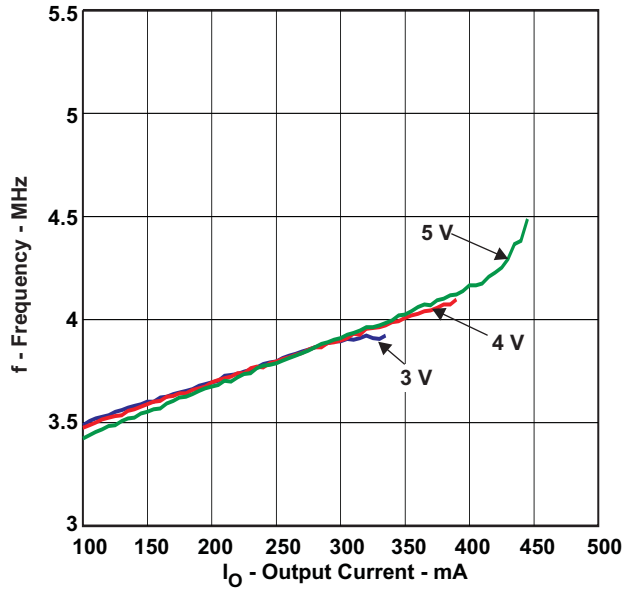


Figure 7. Frequency vs Output Load

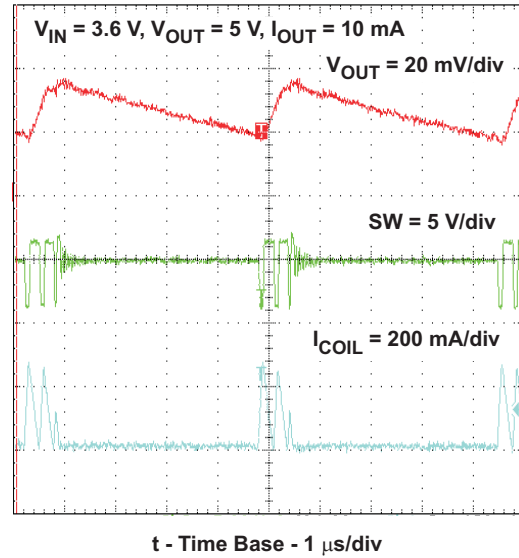


Figure 8. Output Voltage Ripple – PFM Mode

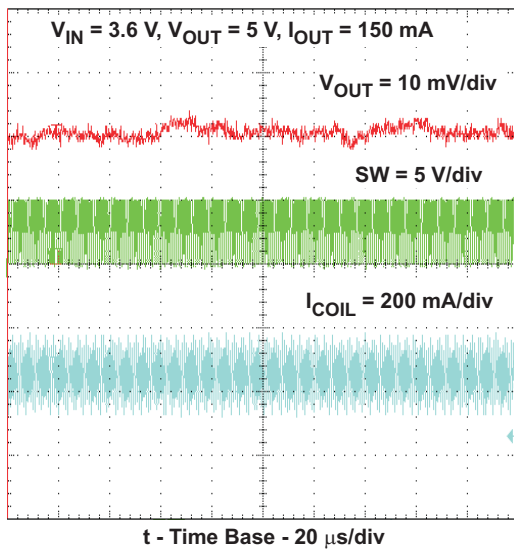


Figure 9. Output Voltage Ripple – PWM Mode

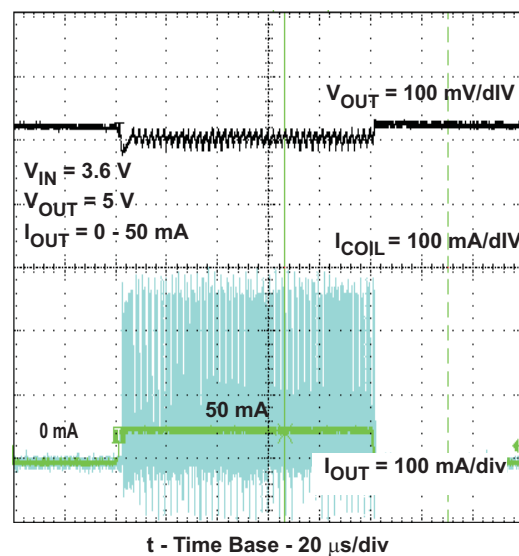


Figure 10. Load Transient Response 0mA–50mA and 50mA–0mA

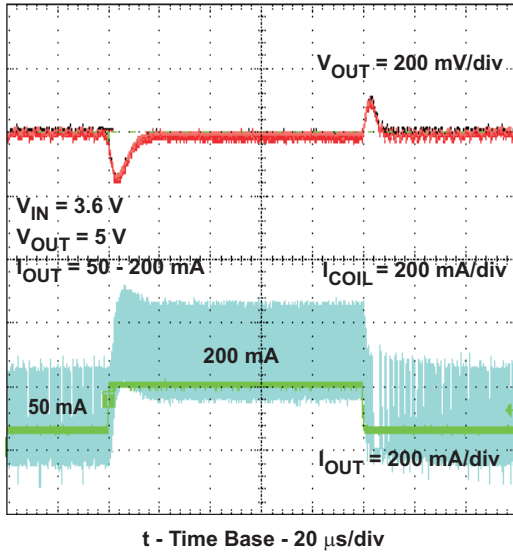


Figure 11. Load Transient Response 0mA–200mA and 200mA–0mA

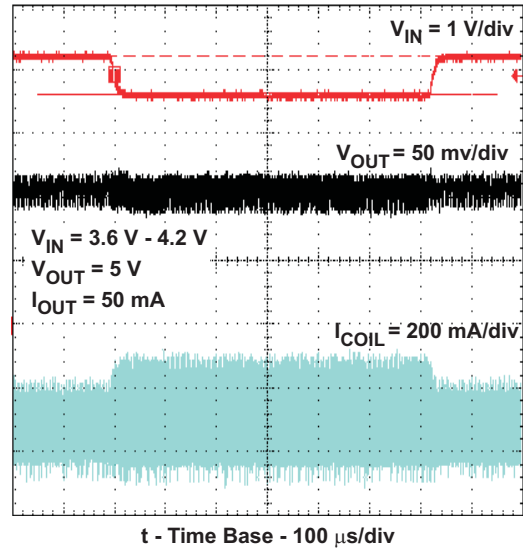


Figure 12. Line Transient Response 3.6V–4.2V at 50mA Load

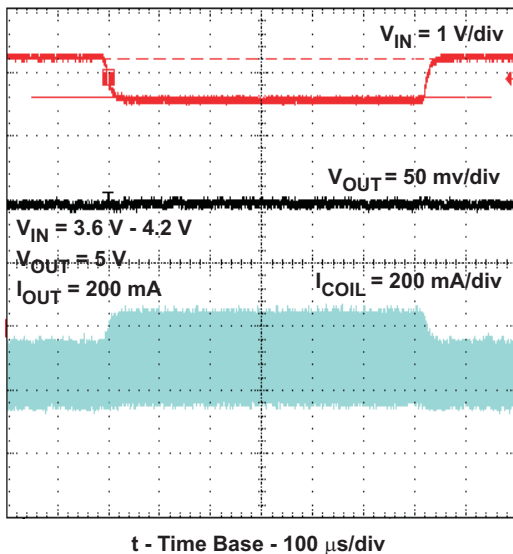


Figure 13. Line Transient Response 3.6V–4.2V at 200mA Load

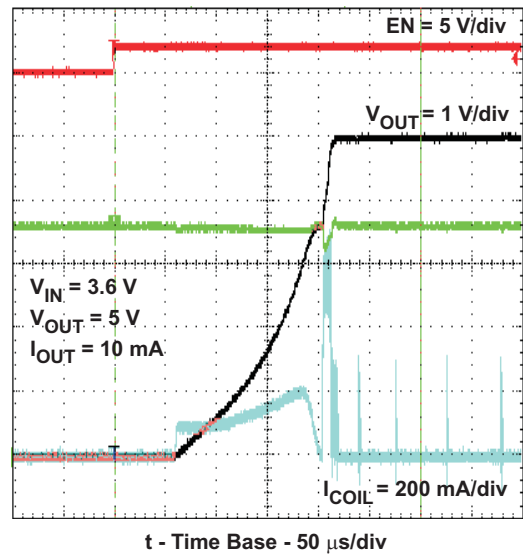
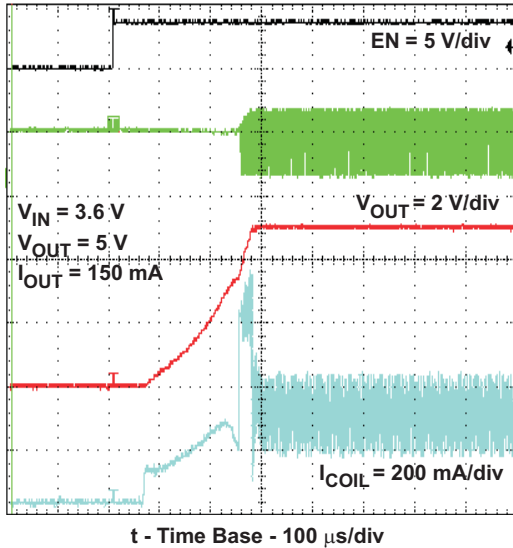
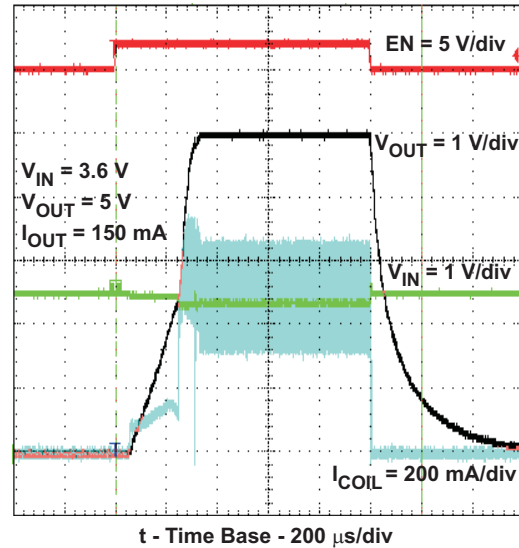


Figure 14. Startup After Enable – No Load


Figure 15. Startup After Enable – With Load

Figure 16. Startup and Shutdown

DETAILED DESCRIPTION

OPERATION

The TPS6124x Boost Converter operates with typically 3.5MHz fixed frequency pulse width modulation (PWM) at moderate to heavy load currents. At light load currents the converter will automatically enter Power Save Mode and operates then in PFM (Pulse Frequency Modulation) mode. During PWM operation the converter uses a unique fast response quasi-constant on-time valley current mode controller scheme which allows “Best in Class” line and load regulation allowing the use of small ceramic input and output capacitors.

Based on the V_{IN}/V_{OUT} ratio, a simple circuit predicts the required on-time. At the beginning of the switching cycle, the low-side N-MOS switch is turned-on and the inductor current ramps up to a defined peak current. In the second phase, once the peak current is reached, the current comparator trips, the on-timer is reset turning off the switch, and the current through the inductor then decays to an internally set valley current limit. Once this occurs, the on-timer is set to turn the boost switch back on again and the cycle is repeated.

CURRENT LIMIT OPERATION

The current limit circuit employs a valley current sensing scheme. Current limit detection occurs during the off time through sensing of the voltage drop across the synchronous rectifier.

The output voltage is reduced as the power stage of the device operates in a constant current mode. The maximum continuous output current ($I_{OUT(CL)}$), before entering current limit operation, can be defined by [Equation 1](#) as shown.

$$I_{OUT(CL)} = (1 - D) \times (I_{VALLEY} + \frac{1}{2} \Delta I_L) \quad \text{with } \Delta I_L = \frac{V_{IN}}{L} \times \frac{D}{f} \quad \text{and } D \approx \frac{V_{OUT} - V_{IN}}{V_{OUT}} \quad (1)$$

[Figure 17](#) illustrates the inductor and rectifier current waveforms during current limit operation. The output current, I_{OUT} , is the average of the rectifier ripple current waveform. When the load current is increased such that the lower peak is above the current limit threshold, the off time is lengthened to allow the current to decrease to this threshold before the next on-time begins (so called frequency fold-back mechanism).

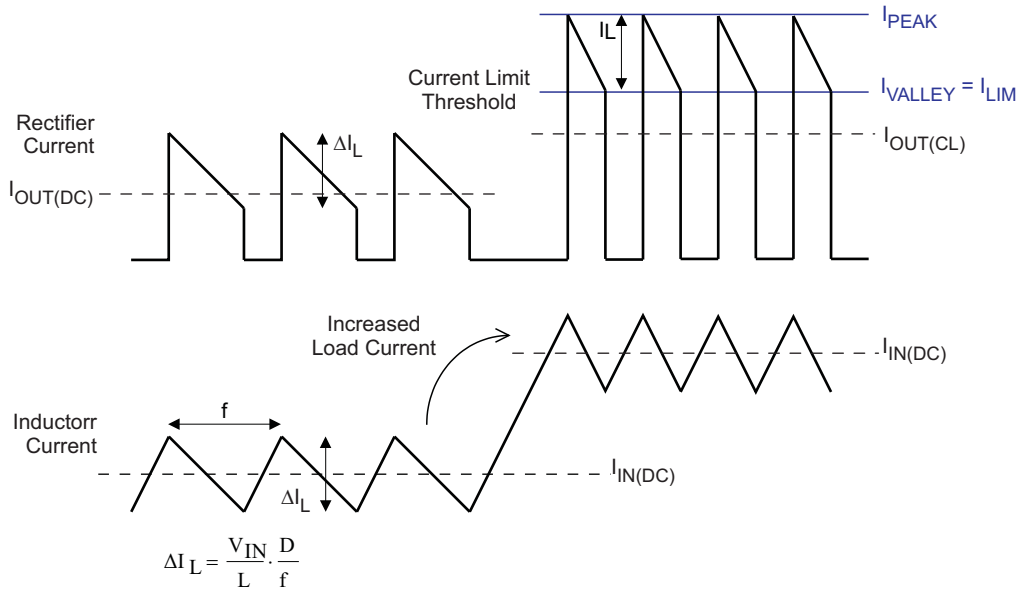
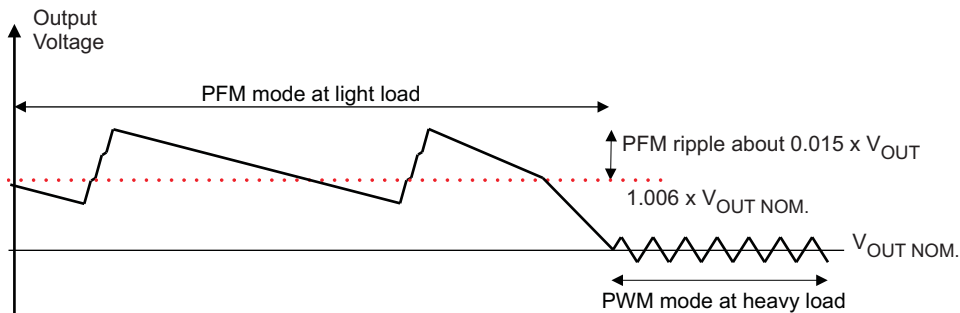


Figure 17. Inductor/Rectifier Currents in Current Limit Operation

POWER-SAVE MODE

The TPS6124x family of devices integrates a power save mode to improve efficiency at light load. In power save mode the converter only operates when the output voltage trips below a set threshold voltage. It ramps up the output voltage with several pulses and goes into power save mode once the output voltage exceeds the set threshold voltage.



The PFM mode is left and PWM mode entered in case the output current can not longer be supported in PFM mode.

UNDER-VOLTAGE LOCKOUT

The under voltage lockout circuit prevents the device from malfunctioning at low input voltages and from excessive discharge of the battery. It disables the output stage of the converter once the falling V_{IN} trips the under-voltage lockout threshold V_{UVLO} . The under-voltage lockout threshold V_{UVLO} for falling V_{IN} is typically 2.0V. The device starts operation once the rising V_{IN} trips under-voltage lockout threshold V_{UVLO} again at typ. 2.1V.

INPUT OVER-VOLTAGE PROTECTION

In the event of an overvoltage condition appearing on the input rail, the output voltage will also experience the overvoltage due to being in dropout condition. A input overvoltage protection feature has been implemented into the TPS6124x which has an input overvoltage threshold of 6.0V. Once this level is triggered, the device will go into a shutdown mode to protect itself. If the voltage drops to 5.9V or below, the device will startup once more into normal operation.

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ENABLE

The device is enabled setting EN pin to high. At first, the internal reference is activated and the internal analog circuits are settled. Afterwards, the soft start is activated and the output voltage is ramped up. The output voltage reaches its nominal value in typically 250 μ s after the device has been enabled.

The EN input can be used to control power sequencing in a system with various DC/DC converters. The EN pin can be connected to the output of another converter, to drive the EN pin high and getting a sequencing of supply rails. With EN = GND, the device enters shutdown mode.

SOFT START

The TPS6124x has an internal soft start circuit that controls the ramp up of the output voltage. The output voltage reaches its nominal value within t_{Start} of typically 250 μ s after EN pin has been pulled to high level. The output voltage ramps up from 5% to its nominal value within t_{RAMP} of typ. 300 μ s.

This limits the inrush current in the converter during start up and prevents possible input voltage drops when a battery or high impedance power source is used.

During soft start, the switch current limit is reduced to 300mA until the output voltage reaches V_{IN} . Once the output voltage trips this threshold, the device operates with its nominal current limit I_{LIMF} .

LOAD DISCONNECT

Load disconnect electrically removes the output from the input of the power supply when the supply is disabled. This is especially important during shutdown. In shutdown of a boost converter, the load is still connected to the input through the inductor and catch diode. Since the input voltage is still connected to the output, a small current continues to flow, even when the supply is disabled. Even small leakage currents significantly reduce battery life during extended periods of off time.

The benefit of this implemented feature for the system design engineer is that the battery is not depleted during shutdown of the converter. No additional components must be added to the design to make sure that the battery is disconnected from the output of the converter.

THERMAL SHUTDOWN

As soon as the junction temperature, T_{J} , exceeds 140°C (typical) the device goes into thermal shutdown. In this mode, the High Side and Low Side MOSFETs are turned-off. When the junction temperature falls below the thermal shutdown hysteresis, the device continues operation.

APPLICATION INFORMATION

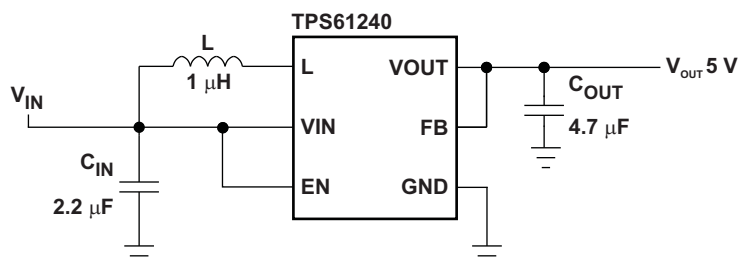


Figure 18. TPS61240 Fixed 5.0V for HDMI / USB-OTG Applications

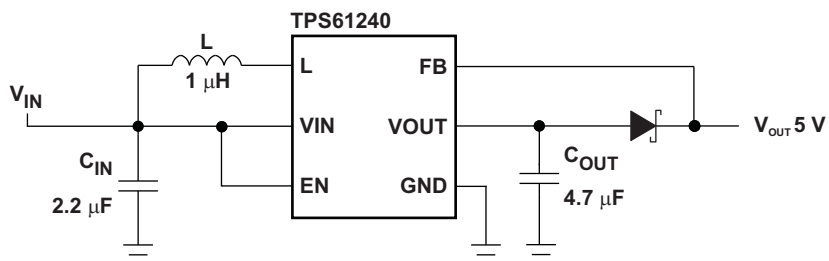


Figure 19. TPS61240 Fixed 5.0V With Schottky Diode for Output Overvoltage Protection

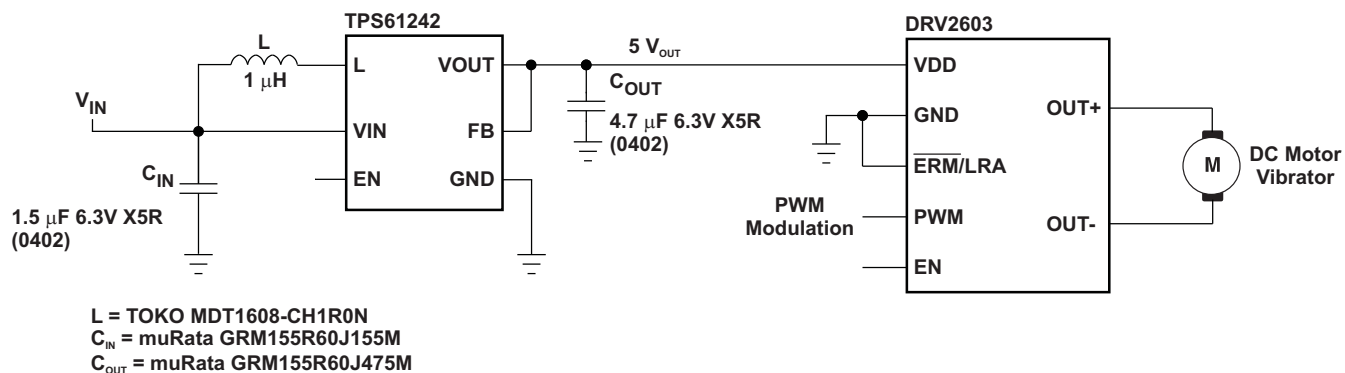


Figure 20. DRV2603 + TPS61242 Haptic Driver Solution featuring PWM Modulation Control

DESIGN PROCEDURE

PROGRAMMING THE OUTPUT VOLTAGE

The output voltage is set by a resistor divider internally. The FB pin is used to sense the output voltage. To configure the output properly, the FB pin needs to be connected directly as shown in [Figure 18](#) and [Figure 19](#).

INDUCTOR SELECTION

To make sure that the TPS6124x devices can operate, an inductor must be connected between pin V_{IN} and pin L. A boost converter normally requires two main passive components for storing energy during the conversion. A boost inductor and a storage capacitor at the output are required. To select the boost inductor, it is recommended to keep the possible peak inductor current below the current limit threshold of the power switch in the chosen configuration. The highest peak current through the inductor and the switch depends on the output load, the input (V_{IN}), and the output voltage (V_{OUT}). Estimation of the maximum average inductor current can be done using [Equation 2](#).

$$I_{L_MAX} \approx I_{OUT} \times \frac{V_{OUT}}{\eta \times V_{IN}} \quad (2)$$

For example, for an output current of 200mA at 5.0V V_{OUT} , at least 540mA of average current flows through the inductor at a minimum input voltage of 2.3V.

The second parameter for choosing the inductor is the desired current ripple in the inductor. Normally, it is advisable to work with a ripple of less than 20% of the average inductor current. A smaller ripple reduces the magnetic hysteresis losses in the inductor, as well as output voltage ripple and EMI. But in the same way, regulation time at load changes rises. In addition, a larger inductor increases the total system size and cost. With these parameters, it is possible to calculate the value of the minimum inductance by using [Equation 3](#).

$$L_{MIN} \approx \frac{V_{IN} \times (V_{OUT} - V_{IN})}{\Delta I_L \times f \times V_{OUT}} \quad (3)$$

Parameter f is the switching frequency and ΔI_L is the ripple current in the inductor, i.e., $20\% \times I_L$. In this example, the desired inductor has the value of 1.7 μH . With this calculated value and the calculated currents, it is possible to choose a suitable inductor. In typical applications a 1.0 μH inductance is recommended. The device has been optimized to operate with inductance values between 1.0 μH and 2.2 μH . It is recommended that inductance values of at least 1.0 μH is used, even if [Equation 3](#) yields something lower. Care has to be taken that load transients and losses in the circuit can lead to higher currents as estimated in Equation 3. Also, the losses in the inductor caused by magnetic hysteresis losses and copper losses are a major parameter for total circuit efficiency.

With the chosen inductance value, the peak current for the inductor in steady state operation can be calculated. [Equation 4](#) shows how to calculate the peak current I .

$$I_{L(\text{peak})} = \frac{V_{IN} \times D}{2 \times f \times L} + \frac{I_{OUT}}{(1 - D) \times \eta} \quad \text{with } D = \frac{V_{OUT} - V_{IN}}{V_{OUT}} \quad (4)$$

This would be the critical value for the current rating for selecting the inductor. It also needs to be taken into account that load transients and error conditions may cause higher inductor currents.

Table 2. Table 1. List of Inductors

| Manufacturer | Series | Dimensions |
|----------------|-------------------|------------------------------|
| TOKO | MDT2012-CH1R0AN | 2.0 x 1.2 x 1.0 max. height |
| | MDT1608-CH1R0N | 1.6 x 0.8 x 0.95 max. height |
| Hitachi Metals | KSLI-201210AG-1R0 | 2.0 x 1.2 x 1.0 max. height |
| | KSLI-201610AG-1R0 | 2.0 x 1.6 x 1.0 max. height |
| muRata | LQM21PN1R0MC0 | 2.0 x 1.2 x 0.55 max. height |
| FDK | MIPS2012D1R0-X2 | 2.0 x 1.2 x 1.0 max. height |

INPUT CAPACITOR

At least 2.2µF input capacitor is recommended to improve transient behavior of the regulator and EMI behavior of the total power supply circuit. It is recommended to place a ceramic capacitor as close as possible to the VIN and GND pins

OUTPUT CAPACITOR

For the output capacitor, it is recommended to use small ceramic capacitors placed as close as possible to the V_{OUT} and GND pins of the IC. If, for any reason, the application requires the use of large capacitors which can not be placed close to the IC, using a smaller ceramic capacitor in parallel to the large one is recommended. This small capacitor should be placed as close as possible to the V_{OUT} and GND pins of the IC. To get an estimate of the recommended minimum output capacitance, Equation 5 can be used.

$$C_{\min} = \frac{I_{\text{OUT}} \times (V_{\text{OUT}} - V_{\text{IN}})}{f \times \Delta V \times V_{\text{OUT}}} \quad (5)$$

Parameter f is the switching frequency and ΔV is the maximum allowed ripple.

With a chosen ripple voltage of 10 mV, a minimum effective capacitance of 2.7 µF is needed. The total ripple is larger due to the ESR of the output capacitor. This additional component of the ripple can be calculated using $\Delta V_{\text{ESR}} = I_{\text{OUT}} \times R_{\text{ESR}}$

A capacitor with a value in the range of the calculated minimum should be used. This is required to maintain control loop stability. There are no additional requirements regarding minimum ESR. There is no upper limit for the output capacitance value. Larger capacitors cause lower output voltage ripple as well as lower output voltage drop during load transients.

Note that ceramic capacitors have a DC Bias effect, which will have a strong influence on the final effective capacitance needed. Therefore the right capacitor value has to be chosen carefully. Package size and voltage rating in combination with material are responsible for differences between the rated capacitor value and the effective capacitance.

CHECKING LOOP STABILITY

The first step of circuit and stability evaluation is to look from a steady-state perspective at the following signals:

- Switching node, SW
- Inductor current, I_L
- Output ripple voltage, V_{O(AC)}

These are the basic signals that need to be measured when evaluating a switching converter. When the switching waveform shows large duty cycle jitter or the output voltage or inductor current shows oscillations, the regulation loop may be unstable. This is often a result of board layout and/or L-C combination.

As a next step in the evaluation of the regulation loop, the load transient response is tested. The time between the application of the load transient and the turn on of the P-channel MOSFET, the output capacitor must supply all of the current required by the load. V_O immediately shifts by an amount equal to ΔI_(LOAD) × ESR, where ESR is the effective series resistance of C_O. ΔI_(LOAD) begins to charge or discharge C_O generating a feedback error signal used by the regulator to return V_O to its steady-state value. The results are most easily interpreted when the device operates in PWM mode. During this recovery time, V_O can be monitored for settling time, overshoot or ringing that helps judge the converter's stability. Without any ringing, the loop has usually more than 45° of phase margin. Because the damping factor of the circuitry is directly related to several resistive parameters (e.g., MOSFET r_{DS(on)}) that are temperature dependant, the loop stability analysis has to be done over the input voltage range, load current range, and temperature range.

TPS61240, TPS61241

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LAYOUT CONSIDERATIONS

As for all switching power supplies, the layout is an important step in the design, especially at high peak currents and high switching frequencies. If the layout is not carefully done, the regulator could show stability problems as well as EMI problems. Therefore, use wide and short traces for the main current path and for the power ground tracks. The input and output capacitor, as well as the inductor should be placed as close as possible to the IC.

Use a common ground node for power ground and a different one for control ground to minimize the effects of ground noise. Connect these ground nodes at any place close to one of the ground pins of the IC. The feedback divider should be placed as close as possible to the control ground pin of the IC. To lay out the control ground, it is recommended to use short traces as well, separated from the power ground traces. This avoids ground shift problems, which can occur due to superimposition of power ground current and control ground current.

LAYOUT GUIDELINES

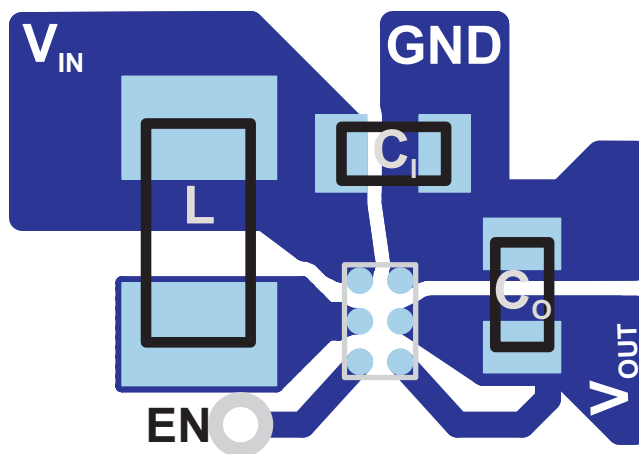


Figure 21. Suggested Layout (Top)

THERMAL INFORMATION

Implementation of integrated circuits in low-profile and fine-pitch surface-mount packages typically requires special attention to power dissipation. Many system-dependant issues such as thermal coupling, airflow, added heat sinks, and convection surfaces, and the presence of other heat-generating components, affect the power-dissipation limits of a given component.

Three basic approaches for enhancing thermal performance are listed below:

- Improving the power dissipation capability of the PCB design
- Improving the thermal coupling of the component to the PCB
- Introducing airflow into the system

The maximum recommended junction temperature (T_J) of the TPS6124x devices is 105°C. The thermal resistance of the 6-pin CSP package (YFF-6) is $R_{\theta JA} = 125^\circ\text{C/W}$. Regulator operation is specified to a maximum steady-state ambient temperature T_A of 85°C. Therefore, the maximum power dissipation is about 160 mW.

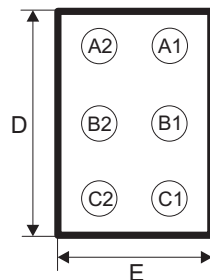
$$P_{D(\text{Max})} = [T_J(\text{max}) - T_A] / \theta_{JA} = [105^\circ\text{C} - 85^\circ\text{C}] / 125^\circ\text{C/W} = 160\text{mW}$$

CHIP SCALE PACKAGE DIMENSIONS

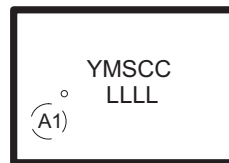
The TPS6124x device is available in a 6-bump chip scale package (YFF, NanoFree™). The package dimensions are given as:

| D | E |
|--------------------------|-------------------------|
| Max = 1280 μm | Max = 890 μm |
| Min = 1220 μm | Min = 830 μm |

Chip Scale Package
(Bottom View)



Chip Scale Package
(Top View)



- Code:
- YM - Year Month date code
 - S - Assembly site code
 - CC - Chip Code
 - LLLL - Lot trace code

PACKAGING INFORMATION

| Orderable Device | Status ⁽¹⁾ | Package Type | Package Drawing | Pins | Package Qty | Eco Plan ⁽²⁾ | Lead/ Ball Finish | MSL Peak Temp ⁽³⁾ | Samples (Requires Login) |
|------------------|-----------------------|--------------|-----------------|------|-------------|----------------------------|----------------------|------------------------------|-----------------------------|
| TPS61240DRVR | ACTIVE | SON | DRV | 6 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| TPS61240DRVT | ACTIVE | SON | DRV | 6 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| TPS61240YFFR | ACTIVE | DSBGA | YFF | 6 | 3000 | Green (RoHS & no Sb/Br) | SNAGCU | Level-1-260C-UNLIM | |
| TPS61240YFFT | ACTIVE | DSBGA | YFF | 6 | 250 | Green (RoHS & no Sb/Br) | SNAGCU | Level-1-260C-UNLIM | |
| TPS61241YFFR | ACTIVE | DSBGA | YFF | 6 | 3000 | Green (RoHS & no Sb/Br) | SNAGCU | Level-1-260C-UNLIM | |
| TPS61241YFFT | ACTIVE | DSBGA | YFF | 6 | 250 | Green (RoHS & no Sb/Br) | SNAGCU | Level-1-260C-UNLIM | |

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSELETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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OTHER QUALIFIED VERSIONS OF TPS61240 :

- Automotive: [TPS61240-Q1](#)

NOTE: Qualified Version Definitions:

- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



| | |
|----|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

TAPE AND REEL INFORMATION

*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|--------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| TPS61240DRVR | SON | DRV | 6 | 3000 | 179.0 | 8.4 | 2.2 | 2.2 | 1.2 | 4.0 | 8.0 | Q2 |
| TPS61240DRVT | SON | DRV | 6 | 250 | 179.0 | 8.4 | 2.2 | 2.2 | 1.2 | 4.0 | 8.0 | Q2 |
| TPS61240YFFR | DSBGA | YFF | 6 | 3000 | 180.0 | 8.4 | 0.98 | 1.41 | 0.69 | 4.0 | 8.0 | Q1 |
| TPS61240YFFT | DSBGA | YFF | 6 | 250 | 180.0 | 8.4 | 0.98 | 1.41 | 0.69 | 4.0 | 8.0 | Q1 |
| TPS61241YFFR | DSBGA | YFF | 6 | 3000 | 180.0 | 8.4 | 0.98 | 1.41 | 0.69 | 4.0 | 8.0 | Q1 |
| TPS61241YFFT | DSBGA | YFF | 6 | 250 | 180.0 | 8.4 | 0.98 | 1.41 | 0.69 | 4.0 | 8.0 | Q1 |

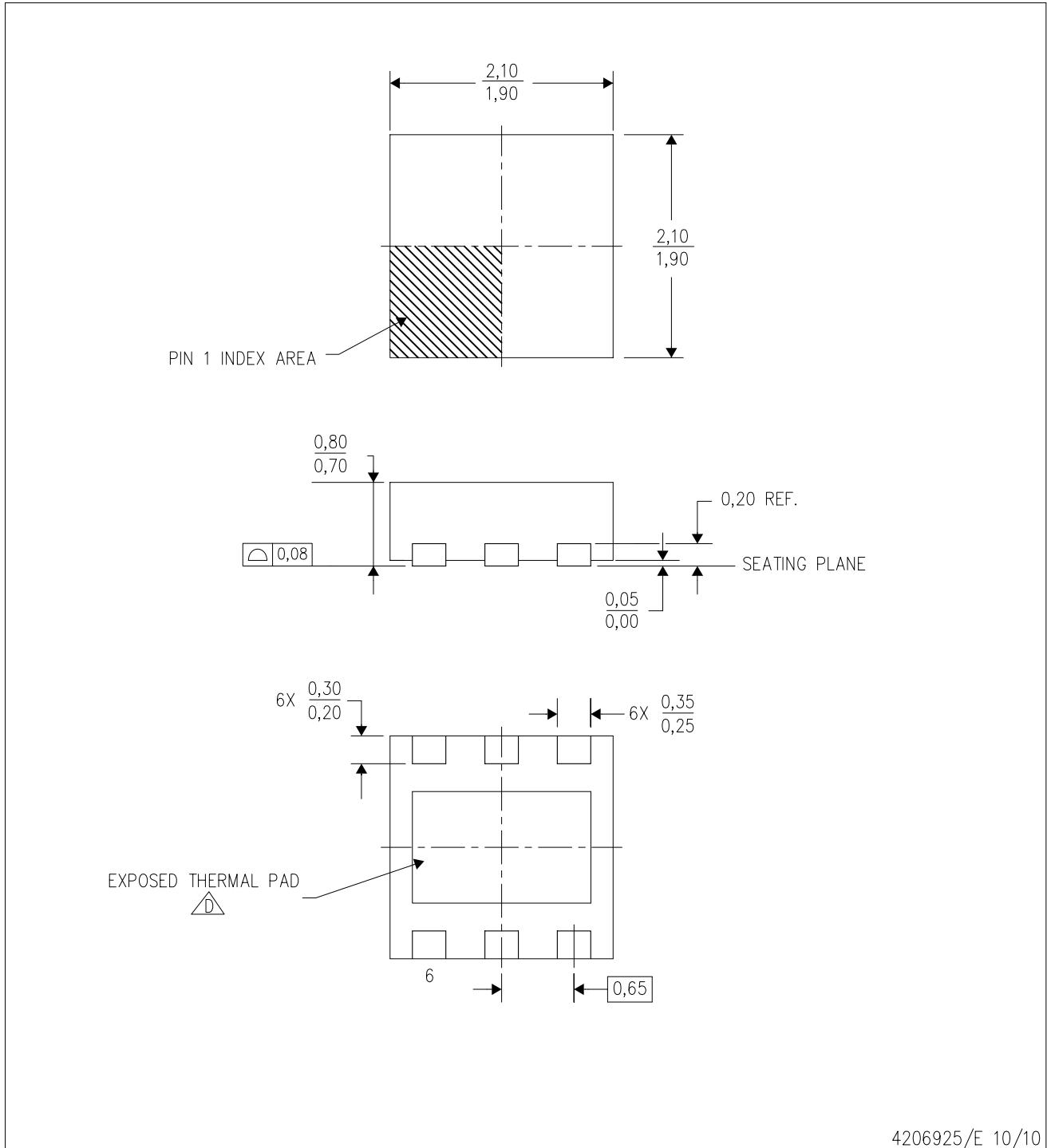
TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|--------------|--------------|-----------------|------|------|-------------|------------|-------------|
| TPS61240DRVR | SON | DRV | 6 | 3000 | 203.0 | 203.0 | 35.0 |
| TPS61240DRVT | SON | DRV | 6 | 250 | 203.0 | 203.0 | 35.0 |
| TPS61240YFFR | DSBGA | YFF | 6 | 3000 | 210.0 | 185.0 | 35.0 |
| TPS61240YFFT | DSBGA | YFF | 6 | 250 | 210.0 | 185.0 | 35.0 |
| TPS61241YFFR | DSBGA | YFF | 6 | 3000 | 210.0 | 185.0 | 35.0 |
| TPS61241YFFT | DSBGA | YFF | 6 | 250 | 210.0 | 185.0 | 35.0 |

DRV (S-PWSON-N6)

PLASTIC SMALL OUTLINE NO-LEAD



4206925/E 10/10

- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. Small Outline No-Lead (SON) package configuration.
 - $\triangle D$ The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.

THERMAL PAD MECHANICAL DATA

DRV (S-PWSON-N6)

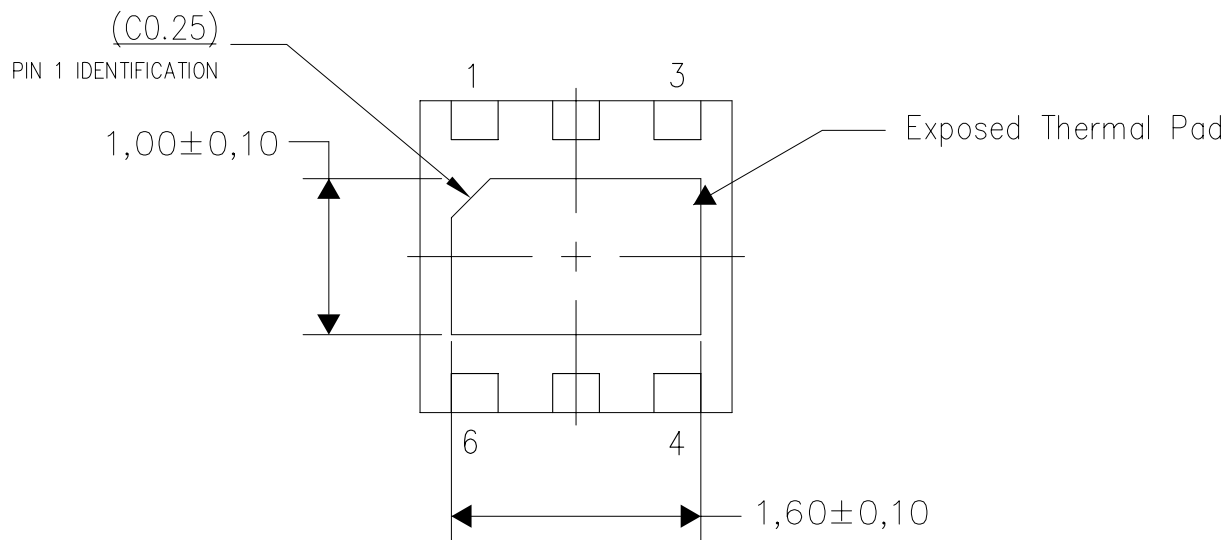
PLASTIC SMALL OUTLINE NO-LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

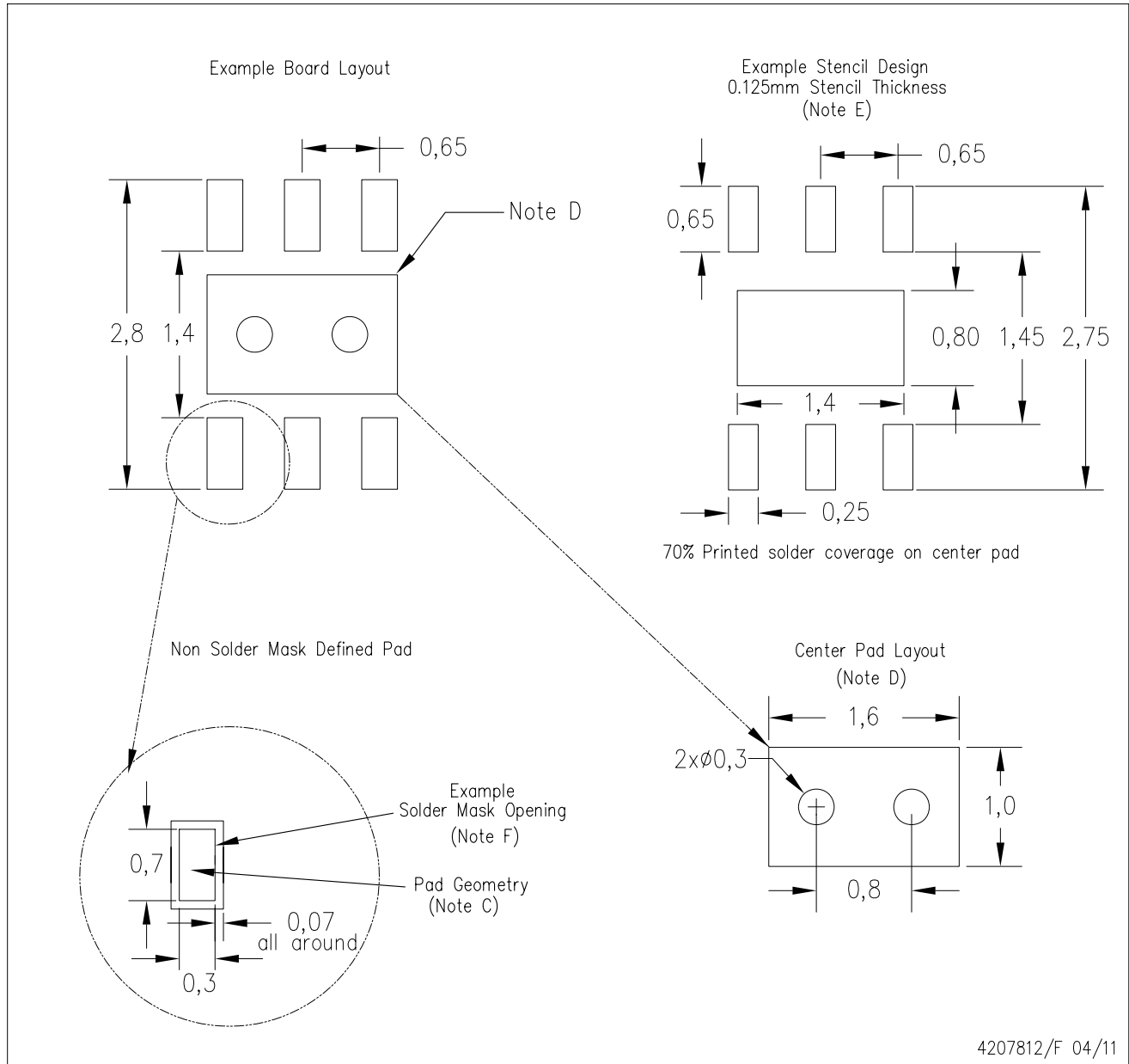
Exposed Thermal Pad Dimensions

4206926-3/L 11/11

NOTE: A. All linear dimensions are in millimeters

DRV (S-PWSON-N6)

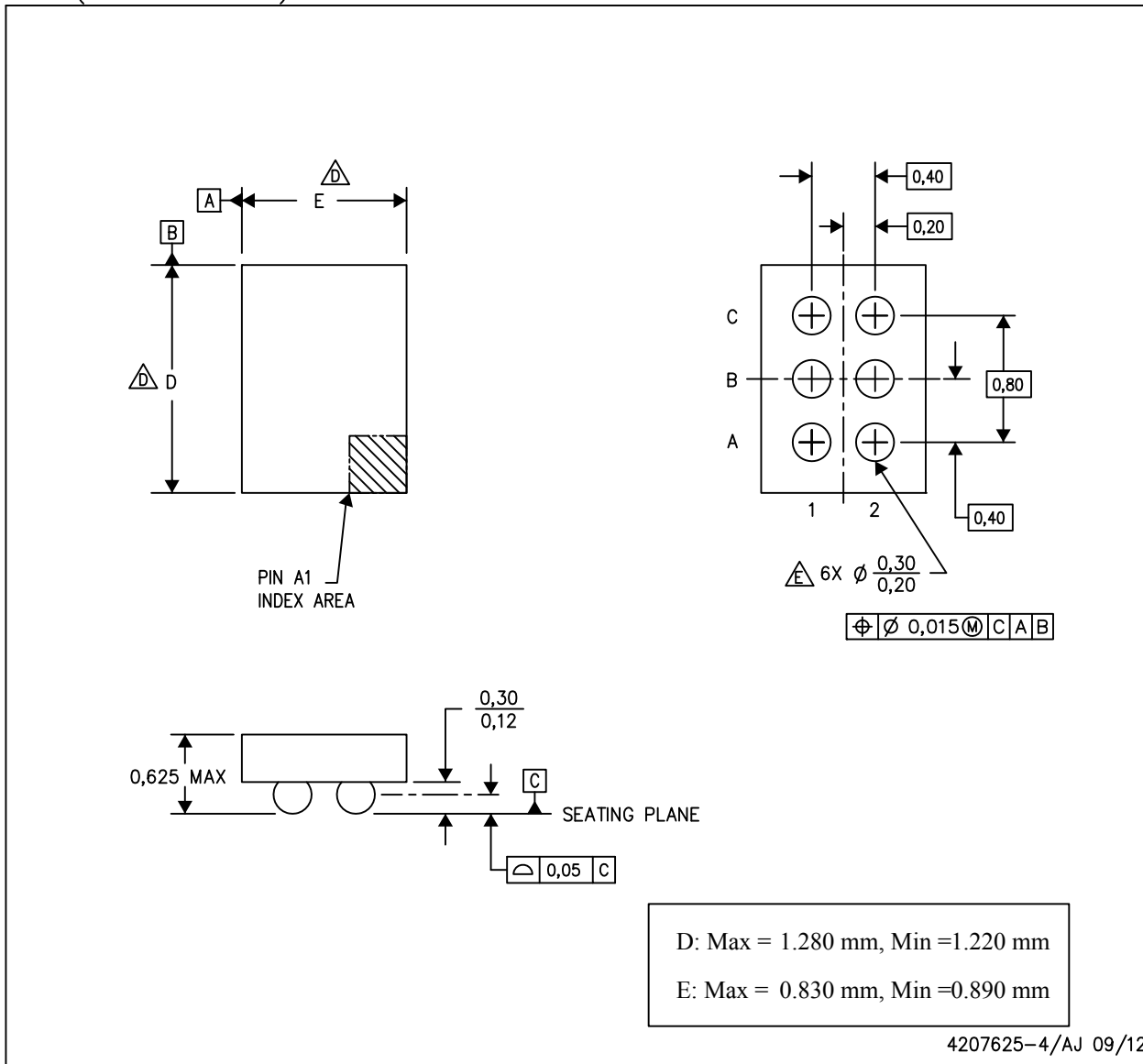
PLASTIC SMALL OUTLINE NO-LEAD



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <<http://www.ti.com>>.
 - E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
 - F. Customers should contact their board fabrication site for solder mask tolerances.

YFF (R-XBGA-N6)

DIE-SIZE BALL GRID ARRAY



- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. NanoFree™ package configuration.
 - \triangle The package size (Dimension D and E) of a particular device is specified in the device Product Data Sheet version of this drawing, in case it cannot be found in the product data sheet please contact a local TI representative.
 - E. Reference Product Data Sheet for array population.
2 x 3 matrix pattern is shown for illustration only.
 - F. This package contains Pb-free balls.

TAPE AND REEL INFORMATION
REEL DIMENSIONS

TAPE DIMENSIONS


| | |
|----|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

TAPE AND REEL INFORMATION

*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|--------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| TPS61240DRVR | SON | DRV | 6 | 3000 | 179.0 | 8.4 | 2.2 | 2.2 | 1.2 | 4.0 | 8.0 | Q2 |
| TPS61240DRVT | SON | DRV | 6 | 250 | 179.0 | 8.4 | 2.2 | 2.2 | 1.2 | 4.0 | 8.0 | Q2 |
| TPS61240YFFR | DSBGA | YFF | 6 | 3000 | 180.0 | 8.4 | 0.98 | 1.41 | 0.69 | 4.0 | 8.0 | Q1 |
| TPS61240YFFT | DSBGA | YFF | 6 | 250 | 180.0 | 8.4 | 0.98 | 1.41 | 0.69 | 4.0 | 8.0 | Q1 |
| TPS61241YFFR | DSBGA | YFF | 6 | 3000 | 180.0 | 8.4 | 0.98 | 1.41 | 0.69 | 4.0 | 8.0 | Q1 |
| TPS61241YFFT | DSBGA | YFF | 6 | 250 | 180.0 | 8.4 | 0.98 | 1.41 | 0.69 | 4.0 | 8.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|--------------|--------------|-----------------|------|------|-------------|------------|-------------|
| TPS61240DRVR | SON | DRV | 6 | 3000 | 203.0 | 203.0 | 35.0 |
| TPS61240DRVT | SON | DRV | 6 | 250 | 203.0 | 203.0 | 35.0 |
| TPS61240YFFR | DSBGA | YFF | 6 | 3000 | 210.0 | 185.0 | 35.0 |
| TPS61240YFFT | DSBGA | YFF | 6 | 250 | 210.0 | 185.0 | 35.0 |
| TPS61241YFFR | DSBGA | YFF | 6 | 3000 | 210.0 | 185.0 | 35.0 |
| TPS61241YFFT | DSBGA | YFF | 6 | 250 | 210.0 | 185.0 | 35.0 |

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