

TANDEM 64-TAP DIGITAL POTENTIOMETER

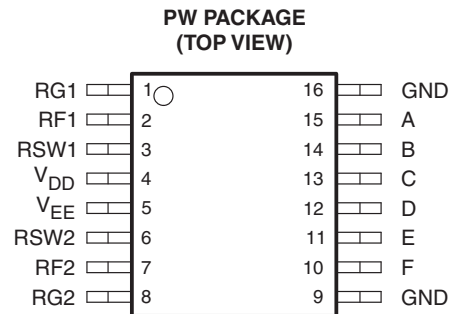
Check for Samples: [TPL8002-25](#)

FEATURES

- Adjustable Gain From 23.25 dB to –24 dB
- 64-Tap Positions With 0.75 dB Per Step
- Supports 8-MHz Analog Bandwidth
- Operating Range up to –4-V V_{EE} /+4-V V_{DD}
- 100- μ A Maximum Static Supply Current
- $\pm 30\%$ End-to-End Resistance Tolerance
- Absolute Tolerance of ± 0.3 dB
- Operating Temperature Range From –40°C to 85°C
- ESD Performance Tested Per JESD 22
 - 2000-V Human-Body Model (A114-B, Class II)

APPLICATIONS

- Tandem Adjustable Feedback and Gain Resistors for Operational Amplifiers



DESCRIPTION/ORDERING INFORMATION

The TPL8002-25 is a programmable resistor device implementing two digital potentiometers with 64 wiper positions each that are tandem controlled through a 6-bit parallel interface. The device has fixed wiper resistances at the respective wiper contacts that tap the potentiometer resistors at a point determined by the binary code present at its digital inputs.

The resistive wiper tap terminals, RSW, of the TPL8002-25 are typically connected to the inverting inputs (–) of an external differential path inverting operational amplifier configuration, with the non-inverting inputs (+) connected through to ground. The application's differential input to the configuration is the device's RG terminals. The differential output of the external operational amplifiers is connected to the device's RF terminals, and thus becomes the differential output of the application configuration.

The resistance between the wiper contacts and the end points RG and RF of the TPL8002-25 provides a logarithmic gain/attenuation response of the configuration. With a digital code of decimal 0 (b000000) the configuration has an inverting maximum attenuation of –24 dB. With a digital code of decimal 32 (b100000) the configuration has inverting unity gain of 0.00 dB. With a digital code of decimal 63 (b111111) the configuration has an inverting maximum gain of +23.25 dB. The response of the configuration with respect to the digital code varies in fixed steps of 0.75 dB.

ORDERING INFORMATION

| T_A | PACKAGE ⁽¹⁾ (2) | | ORDERABLE PART NUMBER | TOP-SIDE MARKING |
|---------------|----------------------------|---------------|-----------------------|------------------|
| –40°C to 85°C | TSSOP – PW | Tape and reel | TPL8002-25PWR | PHY03A |

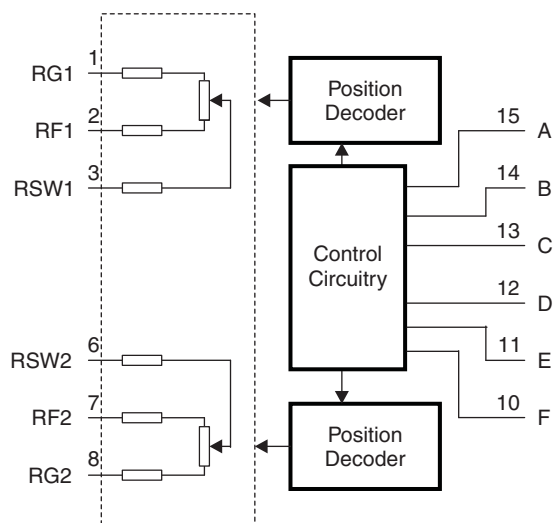
(1) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.

(2) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

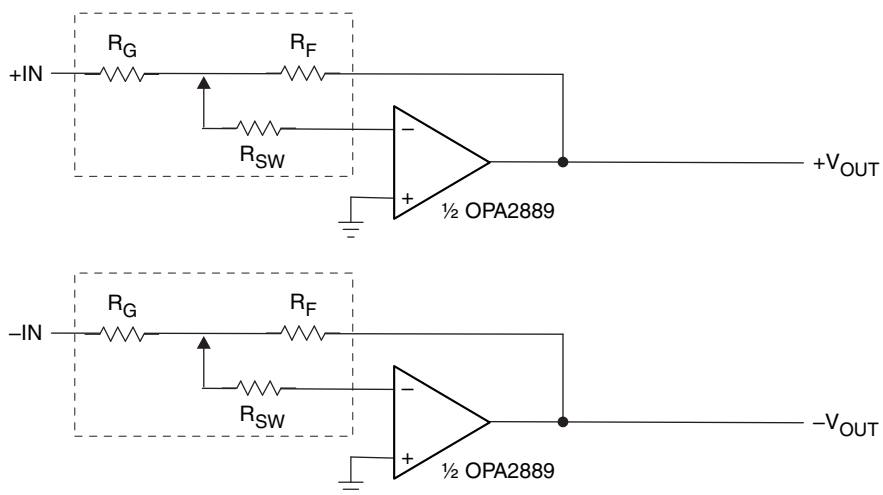


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FUNCTIONAL BLOCK DIAGRAM



TYPICAL APPLICATION CIRCUIT



FUNCTION TABLE

Table 1. Switch Truth Table

| DECIMAL CONTROL | FEDCBA | GAIN/ATTN (dB) | R _G (Ω) | R _F (Ω) |
|--------------------|--------|----------------|--------------------|--------------------|
| 63 | 111111 | 23.25 | 161 | 2339 |
| 62 | 111110 | 22.5 | 174 | 2326 |
| 61 | 111101 | 21.75 | 189 | 2311 |
| 60 | 111100 | 21 | 205 | 2295 |
| 59 | 111011 | 20.25 | 221 | 2279 |
| 58 | 111010 | 19.5 | 239 | 2261 |
| 57 | 111001 | 18.75 | 259 | 2241 |
| 56 | 111000 | 18 | 280 | 2220 |
| 55 | 110111 | 17.25 | 302 | 2198 |
| 54 | 110110 | 16.5 | 325 | 2175 |
| 53 | 110101 | 15.75 | 351 | 2149 |
| 52 | 110100 | 15 | 377 | 2123 |
| 51 | 110011 | 14.25 | 406 | 2094 |
| 50 | 110010 | 13.5 | 436 | 2064 |
| 49 | 110001 | 12.75 | 468 | 2032 |
| 48 | 110000 | 12 | 502 | 1998 |
| 47 | 101111 | 11.25 | 537 | 1963 |
| 46 | 101110 | 10.5 | 575 | 1925 |
| 45 | 101101 | 9.75 | 614 | 1886 |
| 44 | 101100 | 9 | 655 | 1845 |
| 43 | 101011 | 8.25 | 697 | 1803 |
| 42 | 101010 | 7.5 | 742 | 1758 |
| 41 | 101001 | 6.75 | 787 | 1713 |
| 40 | 101000 | 6 | 835 | 1665 |
| 39 | 100111 | 5.25 | 883 | 1617 |
| 38 | 100110 | 4.5 | 933 | 1567 |
| 37 | 100101 | 3.75 | 984 | 1516 |
| 36 | 100100 | 3 | 1036 | 1464 |
| 35 | 100011 | 2.25 | 1089 | 1411 |
| 34 | 100010 | 1.5 | 1142 | 1358 |
| 33 | 100001 | 0.75 | 1196 | 1304 |
| 32 | 100000 | 0 | 1250 | 1250 |
| 31 | 011111 | -0.75 | 1304 | 1196 |
| 30 | 011110 | -1.5 | 1358 | 1142 |
| 29 | 011101 | -2.25 | 1411 | 1089 |
| 28 | 011100 | -3 | 1464 | 1036 |
| 27 | 011011 | -3.75 | 1516 | 984 |
| 26 | 011010 | -4.5 | 1567 | 933 |
| 25 | 011001 | -5.25 | 1617 | 883 |
| 24 | 011000 | -6 | 1665 | 835 |
| 23 | 010111 | -6.75 | 1713 | 787 |
| 22 | 010110 | -7.5 | 1758 | 742 |
| 21 | 010101 | -8.25 | 1803 | 697 |
| 20 | 010100 | -9 | 1845 | 655 |

Table 1. Switch Truth Table (continued)

| DECIMAL CONTROL | FEDCBA | GAIN/ATTN (dB) | R _G (Ω) | R _F (Ω) |
|--------------------|--------|----------------|--------------------|--------------------|
| 19 | 010011 | -9.75 | 1886 | 614 |
| 18 | 010010 | -10.5 | 1925 | 575 |
| 17 | 010001 | -11.25 | 1963 | 537 |
| 16 | 010000 | -12 | 1998 | 502 |
| 15 | 001111 | -12.75 | 2032 | 468 |
| 14 | 001110 | -13.5 | 2064 | 436 |
| 13 | 001101 | -14.25 | 2094 | 406 |
| 12 | 001100 | -15 | 2123 | 377 |
| 11 | 001011 | -15.75 | 2149 | 351 |
| 10 | 001010 | -16.5 | 2175 | 325 |
| 9 | 001001 | -17.25 | 2198 | 302 |
| 8 | 001000 | -18 | 2220 | 280 |
| 7 | 000111 | -18.75 | 2241 | 259 |
| 6 | 000110 | -19.5 | 2261 | 239 |
| 5 | 000101 | -20.25 | 2279 | 221 |
| 4 | 000100 | -21 | 2295 | 205 |
| 3 | 000011 | -21.75 | 2311 | 189 |
| 2 | 000010 | -22.5 | 2326 | 174 |
| 1 | 000001 | -23.25 | 2339 | 161 |
| 0 | 000000 | -24 | 2352 | 148 |

ABSOLUTE MAXIMUM RATINGS^{(1) (2)}

over operating free-air temperature range (unless otherwise noted)

| | | | MIN | MAX | UNIT |
|-------------------|---|--------------------------------|----------------|----------------|------|
| $V_{DD} - V_{EE}$ | Power supply delta voltage ⁽³⁾ | | | 10 | V |
| V_{DD} | Positive supply voltage range ⁽³⁾ | | –0.3 | 5 | V |
| V_{EE} | Negative supply voltage range ⁽³⁾ | | 0.3 | –5 | V |
| V_{IN} | Control input voltage range ^{(2) (3)} | | –0.3 | $V_{DD} + 0.3$ | V |
| $V_{I/O}$ | Resistor I/O voltage range ^{(2) (3) (4)} | | $V_{EE} - 0.3$ | $V_{DD} + 0.3$ | V |
| I_{IK} | Control input clamp current | $V_{IN} < 0$ and $V_{I/O} < 0$ | | –18 | mA |
| $I_{I/OK}$ | I/O port clamp current | $V_{IN} < 0$ and $V_{I/O} < 0$ | | –18 | mA |
| T_{stg} | Storage temperature range | | –40 | 85 | °C |

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltages are with respect to ground, unless otherwise specified.
- (3) The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
- (4) V_I and V_O are used to denote specific conditions for $V_{I/O}$.

RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

| | | MIN | TYP | MAX | UNIT |
|-------------------|----------------------------------|----------------------|------|-----|------|
| $V_{DD} - V_{EE}$ | Power supply delta voltage | | | 8 | V |
| V_{DD} | Positive supply voltage | 2.5 | 3.6 | 4 | V |
| V_{EE} | Negative supply voltage | –2.5 | –3.6 | –4 | V |
| V_{IH} | High-level control input voltage | $V_{DD} \times 0.65$ | | | V |
| V_{IL} | Low-level control input voltage | $V_{DD} \times 0.35$ | | | V |
| V_I | Control input voltage | GND | | | V |
| $V_{I/O}$ | Resistor inputs/outputs | V_{EE} | | | V |
| T_A | Operating free-air temperature | –40 | | | 85 |
| | | | | | °C |

ELECTRICAL CHARACTERISTICS

Dual ± 4 -V Supply

over operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---------------------|------------------------------------|---|------|-----|---------|---------------|
| V_{IK} | Control inputs | $V_{DD} = 4\text{ V}$, $I_{IN} = -18\text{ mA}$ | | | -1.8 | V |
| I_{IN} | | $V_{DD} = 4\text{ V}$, $V_{IN} = V_{DD}$ or GND | | | ± 1 | μA |
| $I_{DD} + I_{EE} $ | | $V_{DD} = 4\text{ V}$, $V_{EE} = -4\text{ V}$, $V_{IN} = V_{DD}$ or GND, $I_{IO} = 0$ | | | 100 | μA |
| C_{IN} | Control capacitance ⁽¹⁾ | $V_{DD} = 4\text{ V}$, $V_{IN} = V_{DD}$ or GND | | 3.2 | | pF |
| C_{RG} | RG capacitance ⁽¹⁾ | $V_{IN} = 0\text{ V}$, frequency = 10 MHz | | 45 | | pF |
| C_{RF} | RF capacitance ⁽¹⁾ | $V_{IN} = 0\text{ V}$, frequency = 10 MHz | | 45 | | pF |
| C_W | Wiper capacitance ⁽¹⁾ | $V_{IN} = 0\text{ V}$, frequency = 10 MHz | | 45 | | pF |
| R | End-to-end resistance | | 1.75 | 2.5 | 3.25 | k Ω |
| R_W | Wiper resistance | | | | 420 | Ω |
| INL | Integral nonlinearity | | -0.3 | | 0.3 | dB |
| DNL | Differential nonlinearity | | -0.3 | | 0.3 | dB |

(1) The AC method is a frequency domain measurement. A 10-MHz ac voltage signal of known dc offset and amplitude of 82.5 mV are applied to the pin under test. The imaginary component of the complex current is measured and used in the equation:

$C = I_{im} / (2 \times \pi \times F \times V_{IN})$ where I_{im} = imaginary component of input current, V_{IN} = magnitude of input voltage, and F = frequency.

SWITCHING CHARACTERISTICS⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|-----------|------------------------------|---|-----|-----|-----|------|
| t_{PS} | Control to output step delay | | | 100 | | ns |
| BW | Analog signal bandwidth | For a typical example, see Figure 2 | 8 | | | MHz |

(1) Typical bandwidth shown in [Figure 2](#) supports 6 MHz minimum.

PARAMETER MEASUREMENT INFORMATION

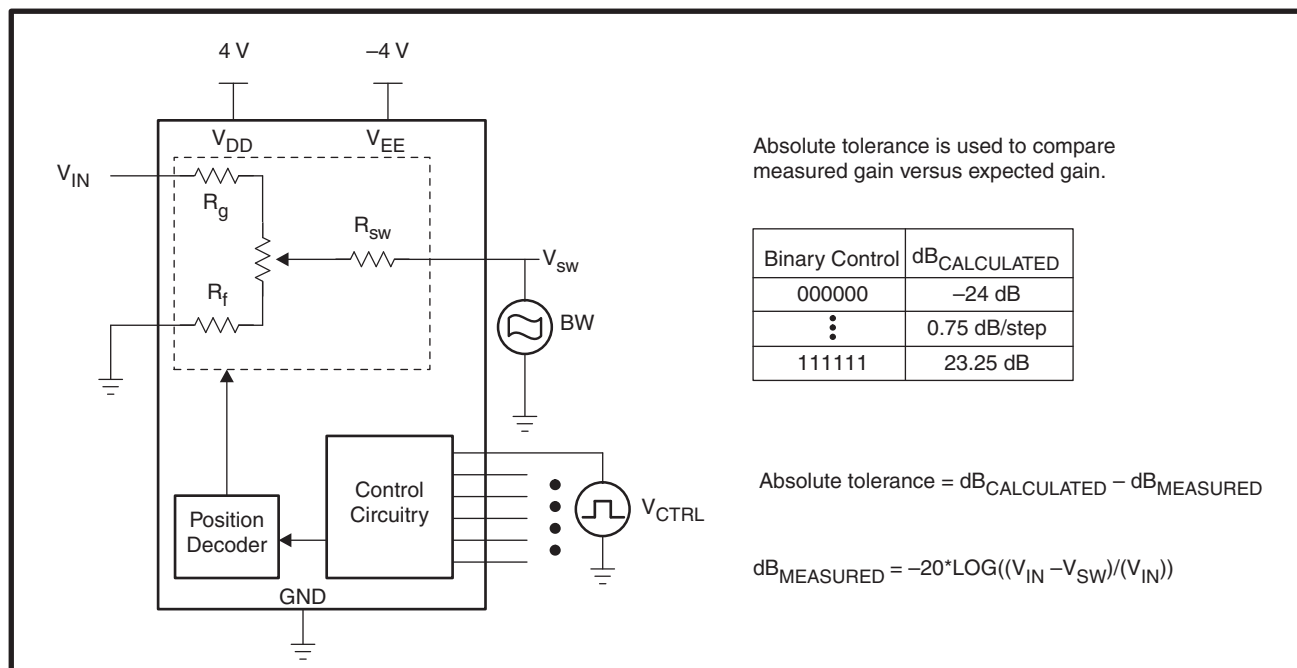


Figure 1. Analog Signal Bandwidth and Absolute Tolerance

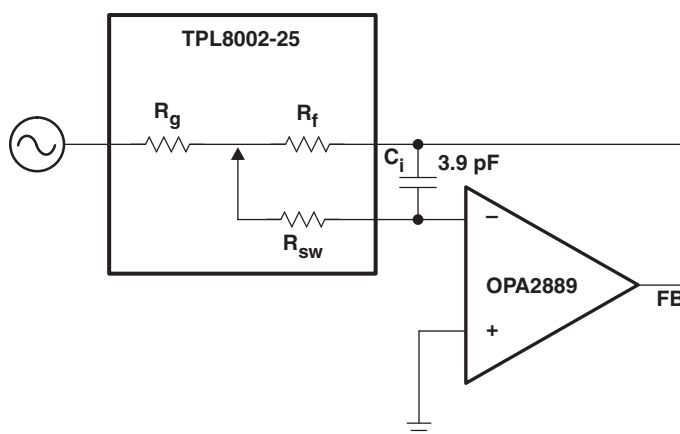


Figure 2. Bandwidth Setup

PACKAGING INFORMATION

| Orderable Device | Status ⁽¹⁾ | Package Type | Package Drawing | Pins | Package Qty | Eco Plan ⁽²⁾ | Lead/Ball Finish | MSL Peak Temp ⁽³⁾ |
|------------------|-----------------------|--------------|-----------------|------|-------------|-------------------------|------------------|------------------------------|
| TPL8002-25PWR | ACTIVE | TSSOP | PW | 16 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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TAPE AND REEL INFORMATION
REEL DIMENSIONS

TAPE DIMENSIONS


| | |
|----|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

TAPE AND REEL INFORMATION

*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| TPL8002-25PWR | TSSOP | PW | 16 | 2000 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS

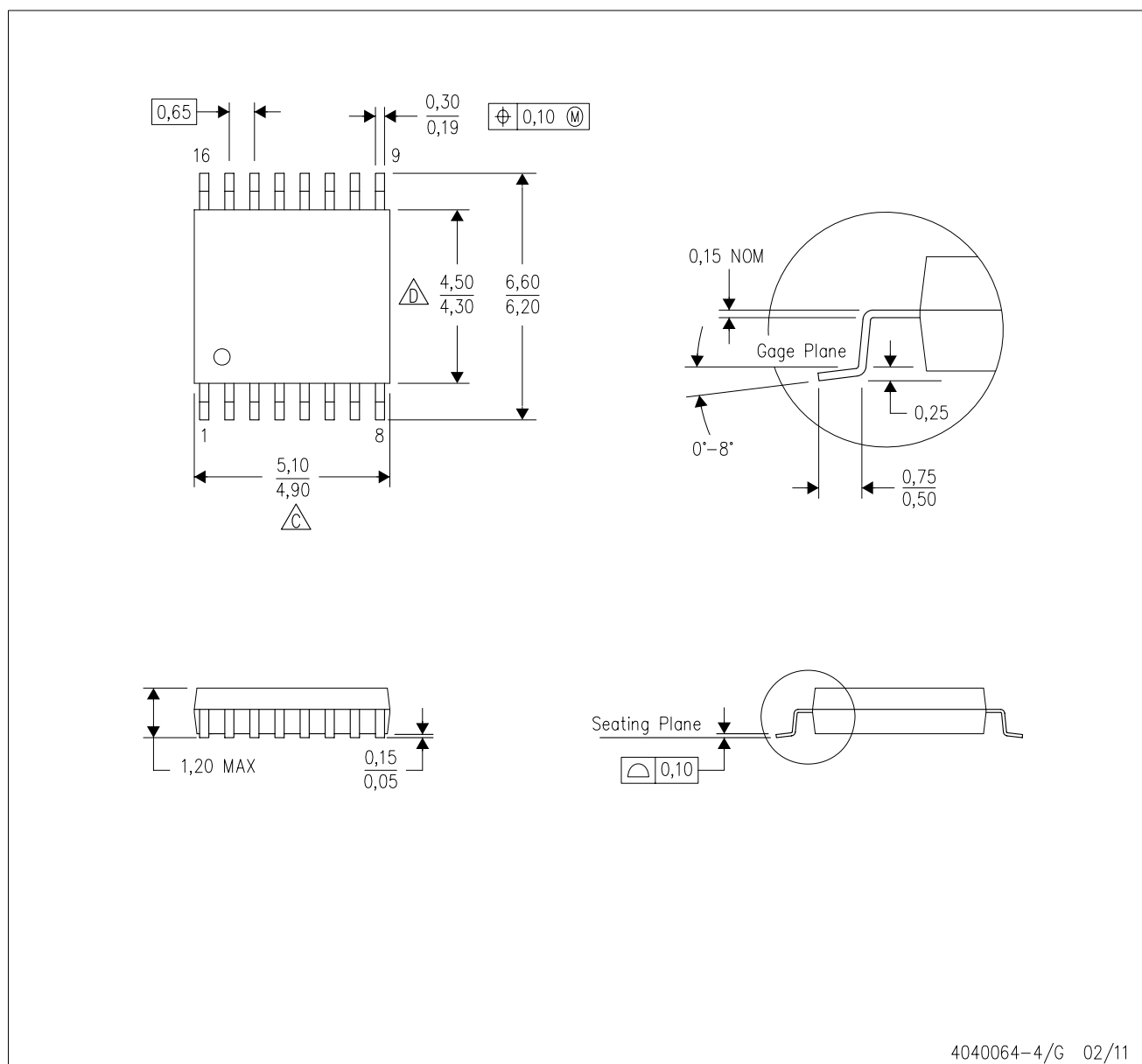


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---------------|--------------|-----------------|------|------|-------------|------------|-------------|
| TPL8002-25PWR | TSSOP | PW | 16 | 2000 | 367.0 | 367.0 | 35.0 |

PW (R-PDSO-G16)

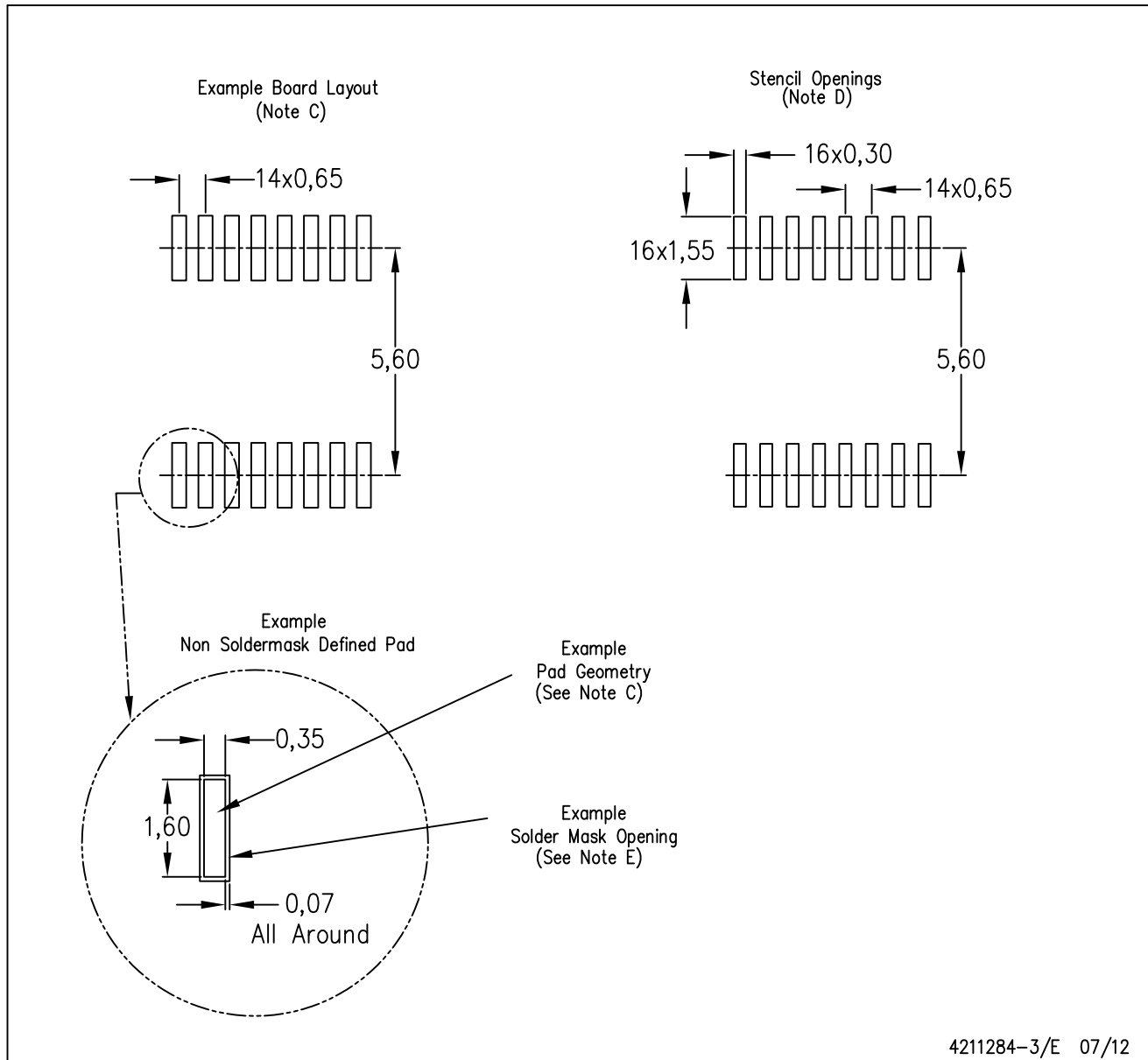
PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
 - D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
 - E. Falls within JEDEC MO-153

PW (R-PDSO-G16)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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