CMOS 8-Bit Microcontroller

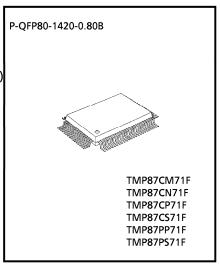
TMP87CM71F, TMP87CN71F, TMP87CP71F, TMP87CS71F

The TMP87CM71/N71/P71/S71 are the high speed and high performance 8-bit single chip microcomputers. These MCU contain 6-bit AD conversion inputs and a VFT (Vacuum Fluorescent Tube) driver on a chip.

Part No.	ROM	RAM	Package	OTP MCU
TMP87CM71F	32 K × 8-bit			
TMP87CN71F	40 K × 8-bit	1.5 K × 8-bit	P-QFP80-1420-0.80B	TMP87PP71F / TMP87PS71F
TMP87CP71F	48 K × 8-bit		F-QFF80-1420-0.80B	
TMP87CS71F	61184 × 8-bit	2.0 K × 8-bit		TMP87PS71F

Features

- ◆8-bit single chip microcomputer TLCS-870 Series
- lack Instruction execution time: 0.5 μ s (at 8 MHz), 122 μ s (at 32.768 kHz)
- 412 basic instructions
 - Multiplication and Division (8 bits x 8 bits, 16 bits ÷ 8 bits)
 - Bit manipulations (Set/Clear/Complement/Move/Test/Exclusive or)
 - 16-bit data operations
 - 1-byte jump/subroutine-call (Short relative jump/ Vector call)
- ◆ 14 interrupt sources (External: 5, Internal: 9)
 - All sources have independent latches each. and nested interrupt control is available.
 - 3 edge-selectable external interrupts with noise reject
 - High-speed task switching by register bank changeover
- ◆ 10 Input/Output ports (73 pins)
 - Output: 1 port (8 pins)
 - Input/Output: 9 ports (65 pins)
- Two 16-bit Timer/Counters
 - Timer, Event counter modes
- Two 8-bit Timer/Counters
 - Timer, Event counter, Capture (Pulse width/duty measurement), PWM output, Programmable divider
- ◆Time Base Timer (Interrupt frequency: 1 Hz to 16 kHz)
- Divider output function (frequency: 1 kHz to 8 kHz)
- ►Watchdog Timer
 - Interrupt source/reset output (programmable)



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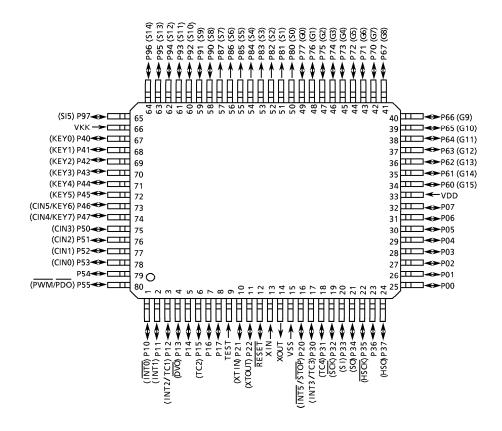
- ◆8-bit Serial Interface
 - With 8 bytes transmit/receive data buffer
 - Internal/external serial clock, and 4/8-bit mode
- igspace8-bit High Speed Serial Output (rate: max. 1 bit / μ s)
- ♦6-bit AD conversion input (6 channels)
- ◆ Vacuum Fluorescent Tube Driver (automatic display)
 - High breakdown voltage ports
- ◆Key scanning function
 - Key-matrix constructed by segment outputs (1 to 16) and key inputs (1 to 8)
- ◆ Dual clock operation
 - Single/Dual-clock mode (option)
- ◆ Five Power saving operating modes
 - STOP mode: Oscillation stops. Battery/Capacitor back-up. Port output hold/High-impedance.
 - SLOW mode: Low power consumption operation using low-frequency clock (32.768 kHz).
 - IDLE1 mode: CPU stops, and Peripherals operate using high-frequency clock. Release by interrupts.
 - IDLE2 mode: CPU stops, and Peripherals operate using high-and low-frequency clock. Release by interrupts.
 - SLEEP mode: CPU stops, and Peripherals operate using low-frequency clock. Release by interrupts.
- ◆ Wide operating voltage: 2.7 to 5.5 V at 4.19 MHz/32.768 kHz, 4.5 to 5.5 V at 8 MHz/32.768 kHz (TMP87CM71/N71/P71)

2.7 to 5.5 V at 32.768 kHz, 4.5 to 5.5 V at 8 MHz/32.768 kHz (TMP87CS71)

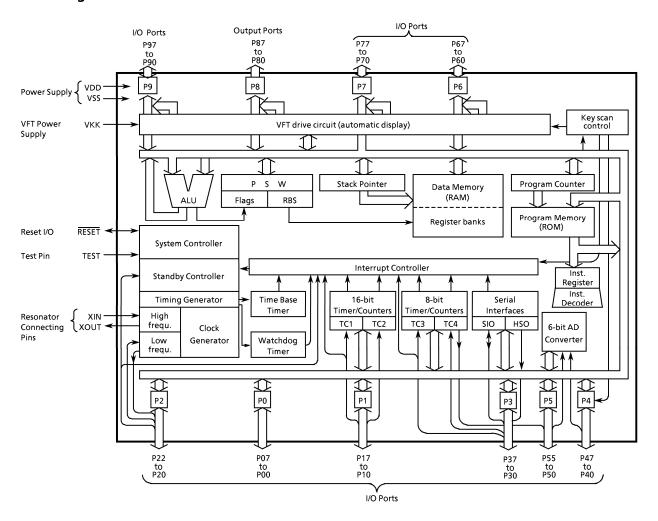
◆Emulation Pod: BM87CK70F0B

Pin Assignments (Top View)

P-QFP80-1420-0.80B



Block Diagram



Pin Function

Pin Name	Input / Output	Function						
P07 to P00	1/0							
P17, P16, P14	I/O	Two 8-bit programmable input/output ports (tri-state).						
P15 (TC2)	I/O (Input)	Each bit of these ports can be	Timer/Counter 2 input					
P13 (DVO)	I/O (Output)	individually configured as an input or an	Divider output					
P12 (INT2 / TC1)	•••••	output under software control. During reset, all bits are configured as	External interrupt input 2 or Timer/Counter 1 input					
P11 (INT1)	I/O (Input)	inputs. When used as a divider output, the latch	External interrupt input 1					
P10 (INT0)		must be set to "1".	External interrupt input 0					
P22 (XTOUT)	I/O (Output)	3-bit input/output port with latch.	Resonator connecting pins (32.768 kHz). For inputting external clock, XTIN is used					
P21 (XTIN)	I/O (Input)	When used as an input port, the latch	and XTOUT is opened.					
P20 (ĪNT5/STOP)		must be set to "1".	External interrupt input 5 or STOP mode release signal input					
P37 (HSO)	I/O (Output)		HSO serial data output					
P36	1/0							
P35 (HSCK)	I/O (Output)	8-bit input/output port with latch.	HSO serial clock output					
P34 (SO)	"O (Output)	When used as an input port, a HSO output, a SIO input/output, a	SIO serial data output					
P33 (SI)	I/O (Input)	timer/counter input, or an interrupt input, the latch must be set to "1".	SIO serial data input					
P32 (SCK)	I/O (I/O)	input, the later must be set to 1.	SIO serial clock input/output					
P31 (TC4)	I/O (Input)		Timer/Counter 4 input					
P30 (INT3 / TC3)	ii o (iiiput)		External interrupt input 3 or Timer/Counter 3 input					
P47 (CIN4 / KEY7), P46 (CIN5 / KEY6) P45 (KEY5)	I/O (Input)	8-bit input/output port with latch. When used as an input port, the latch	Comparator inputs or Key scan inputs					
to P40 (KEY0)		must be set to "1".	Key scan inputs 8-bit PWM output or					
P55 (PWM / PDO)	I/O (Output)	6-bit input/output port with latch. When used as an input port, a compa-	8-bit programmable divider output					
P54 P53 (CIN0)	1/0	rator input, or a PWM / PDO output, the						
to P50 (CIN3)	I/O (Input)	latch must be set to "1".	Comparator inputs					
P67 (G8) to P60 (G15)		Three 8-bit high breakdown voltage I/O	VFT digit driver outputs					
P77 (G0) to P70 (G7)	I/O (Output)	ports with the latch. When used as a VFT driver output, the latch must be cleared	- '					
P97 (S15) to P90 (S8)	Outout	to"0".	VFT segment driver outputs					
P87 (S7) to P80 (S0)	Output (Output)	8-bit high breakdown voltage output port with latch. When used as VFT driver output, the latch must be cleared to "0".	(Key strobe outputs)					
XIN, XOUT	Input, Output	Resonator connecting pins for high-frequency clock. For inputting external clock, XIN is used and XOUT is opened.						
RESET	I/O	Reset signal input or watchdog timer output/address-trap-reset output/system-clock-reset output.						
TEST	Input	Test pin for out-going test. Be tied to low.						
VDD, VSS	Power Supply	+5 V, 0 V (GND)						
VKK	i ower suppry	VFT driver power supply						

Operational Description

1. CPU Core Functions

The CPU core consists of a CPU, a system clock controller, an interrupt controller, and a watchdog timer. This section provides a description of the CPU core, the program memory (ROM), the data memory (RAM), and the reset circuit.

1.1 Memory Address Map

The TLCS-870 Series is capable of addressing 64K bytes of memory. Figure 1-1 shows the memory address maps of the TMP87CM71/N71/P71/S71. In the TLCS-870 Series, the memory is organized 4 address spaces (ROM, RAM, SFR, and DBR). It uses a memory mapped I/O system, and all I/O registers are mapped in the SFR/DBR address spaces. There are 16 banks of general-purpose registers. The register banks are also assigned to the first 128 bytes of the RAM address space.

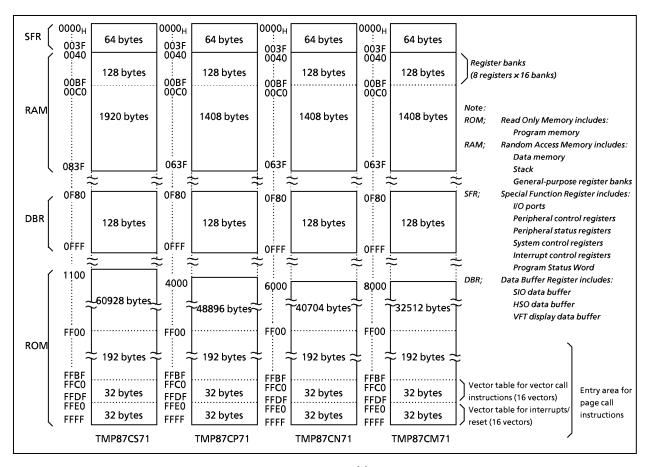


Figure 1-1. Memory Address Maps

Electrical Characteristics

Absolute Maximum Ratings

 $(V_{SS} = 0 V)$

Parameter	Symbol	Conditions	Ratings	Unit
Supply Voltage	V_{DD}		– 0.3 to 6.5	V
Input Voltage	V _{IN}		- 0.3 to V _{DD} + 0.3	٧
Output Valtage	V _{OUT1}	P2, P3, P4, P5, XOUT, RESET	- 0.3 to V _{DD} + 0.3	v
Output Voltage	V _{OUT2}	Source open drain ports	$V_{DD} - 40 \text{ to } V_{DD} + 0.3$]
	I _{OUT1}	P0, P1, P2, P3, P4, P5	3.2	
Output Current (Per 1 pin)	Іопт3	P8, P9 (segment outputs)	- 12	mA
	I _{OUT4}	P6, P7 (digit outputs)	- 25	
O to 15 word (Total)	Σ I _{OUT1}	P0, P1, P2, P3, P4, P5	120	
Output Current (Total)	Σ I _{OUT2}	P6, P7, P8, P9	- 120	mA
Power Dissipation [Topr = 70°C]	PD		350	mW
Soldering Temperature (time)	Tsld		260 (10 s)	°C
Storage Temperature	Tstg		– 55 to 125	°C
Operating Temperature	Topr		– 30 to 70	°C

Note: The absolute maximum ratings are rated values which must not be exceeded during operation, even for an instant. Any one of the ratings must not be exceeded. If any absolute maximum rating is exceeded, a device may break down or its performance may be degraded, causing it to catch fire or explode resulting in injury to the user. Thus, when designing products which include this device, ensure that no absolute maximum rating value will ever be exceeded.

(1) TMP87CM71/N71/P71

Recommended Operating Conditions

 $(V_{SS} = 0 \text{ V}, \text{ Topr} = -30 \text{ to } 70^{\circ}\text{C})$

Parameter	Symbol	Pins	C	Conditions	Min	Max	Unit
				NORMAL1, 2 modes	4.5		
			fc = 8 MHz	IDLE1, 2 modes	4.5		
			f- 4.2 NALL-	NORMAL1, 2 modes			
Supply Voltage	V_{DD}		fc = 4.2 MHz	IDLE1, 2 modes	2.7	5.5	V
			fs =	SLOW mode	2.7		
			32.768 kHz	SLEEP mode			
				STOP mode	2.0		
	V _{IH1}	Except hysteresis input	V _{DD} ≥ 4.5 V V _{DD} <4.5 V		$V_{DD} \times 0.70$	V _{DD}	v
Input High Voltage	V _{IH2}	Hysteresis input			$V_{DD} \times 0.75$		
	V _{IH3}				$V_{DD} \times 0.90$		
	V_{IL1}	Except hysteresis input	V >4.5.V			$V_{DD} \times 0.30$	
Input Low Voltage	V_{IL2}	Hysteresis input	\ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \	V _{DD} ≧ 4.5 V		$V_{DD} \times 0.25$	V
	V _{IL3}		V	_{DD} <4.5 V		$V_{DD} \times 0.10$	
	٤.	VIN YOUT	VDD = 4.5 to 5.5V		0.4	8.0	NALLE.
Clock Frequency	fc XIN, XOUT		VDD = 2.7 to 5.5V		0.4	4.2	MHz
	fs	XTIN, XTOUT			30.0	34.0	kHz

Note: The recommended operating conditions for a device are operating conditions under which it can be guaranteed that the device will operate as specified. If the device is used under operating conditions other than the recommended operating conditions (supply voltage, operating temperature range, specified AC/DC values etc.), malfunction may occur. Thus, when designing products which include this device, ensure that the recommended operating conditions for the device are always adhered to.

(2) TMP87CS71

Recommended Operating Conditions

 $(V_{SS} = 0 \text{ V}, \text{ Topr} = -30 \text{ to } 70^{\circ}\text{C})$

Parameter	Symbol	Pins	(Conditions	Min	Max	Unit
Supply Voltage			f- 0.0411-	NORMAL1, 2 modes	4.5		
			fc = 8 MHz	IDLE1, 2 modes	4.5		
	V_{DD}		fs = SLOW mode	SLOW mode	2.7	5.5	V
			32.768 kHz	SLEEP mode	2.7		
				STOP mode	2.0		
	V _{IH1}	Except hysteresis input	V _{DD} ≥ 4.5 V V _{DD} <4.5 V		V _{DD} × 0.70	V _{DD}	\ \
Input High Voltage	V _{IH2}	Hysteresis input			V _{DD} × 0.75		
	V _{IH3}				$V_{DD} \times 0.90$		
	V_{IL1}	Except hysteresis input	V >45V			$V_{DD} \times 0.30$	
Input Low Voltage	V_{IL2}	Hysteresis input]	V _{DD} ≧ 4.5 V		$V_{DD} \times 0.25$	V
	V_{IL3}		V _{DD} <4.5 V			V _{DD} × 0.10	
Clask Fraguency	fc	XIN, XOUT	VDD) = 4.5 to 5.5V	0.4	8.0	MHz
Clock Frequency	fs	XTIN, XTOUT			30.0	34.0	kHz

DC Characteristics

 $(V_{SS} = 0 \text{ V}, \text{ Topr} = -30 \text{ to } 70^{\circ}\text{C})$

Parameter	Symbol	Pins	Co	onditions	Min	Тур.	Max	Unit
Hysteresis Voltage	V_{HS}	Hysteresis input			-	0.9	-	٧
	I _{IN1}	TEST						
Input Current	I _{IN2}	Open drain ports, Tri-state ports	$V_{DD} = 5.5 V$ $V_{IN} = 5.5 V/0 V$		_	_	± 2	μΑ
	I _{IN3}	RESET, STOP						
Innut Basistanaa	R _{IN1}	Port P4 with pull-down		30	70	150		
Input Resistance	R _{IN2}	RESET				220	450	kΩ
Pull-down Resistance	R_{K}	Source open drain ports	$V_{DD} = 5.5 \text{ V}, V_{KK} = -33 \text{ V}$		_	80	ı	
	I _{LO1}	Sink open drain ports	$V_{DD} = 5.5 \text{ V}, V_{OUT} = 5.5 \text{ V}$ $V_{DD} = 5.5 \text{ V}, V_{OUT} = -33 \text{ V}$ $V_{DD} = 5.5 \text{ V}, V_{OUT} = 5.5 \text{ V} / 0 \text{ V}$		_	_	2	
Output Leakage Current	I _{LO2}	Source open drain ports			_	_	- 2	μΑ
	I _{LO3}	Tri-state ports			_	_	± 2	
Output High Voltage	V _{OH2}	Tri-state ports	$V_{DD} = 4.5 \text{ V}, I_{OH} = -0.7 \text{ mA}$		4.1	-	ı	٧
Output High Voltage	V _{OH3}	P8, P9	$V_{DD} = 4.5 \text{ V}, I_{OH} = -5 \text{ mA}$		2.4	-	ı	V
Output Low Voltage	V_{OL}	Except XOUT	$V_{DD} = 4.5 V, I_{OL} =$	= 1.6 mA	-	-	0.4	٧
Output High current	I _{OH}	P6, P7	$V_{DD} = 4.5 V, V_{OH}$	= 2.4 V	_	- 15	1	mA
Supply Current in			V _{DD} = 5.5 V	TMP87CM71/N71/P71	-	10.0	16.0	
NORMAL 1, 2 modes			fc = 8 MHz TMP87CS71		_	11.0	17.0	mA
Supply Current in IDLE 1, 2 modes			$V_{IN} = 5.3 \text{ V} / 0.2 \text{ V}$	= 32.768 kHz		4.5	6.0	
Supply Current in SLOW mode	I _{DD}		V _{DD} = 3.0 V fs = 32.768 kHz V _{IN} = 2.8 V / 0.2 V		-	30	60	^
Supply Current in SLEEP mode					_	15	30	μΑ
Supply Current in STOP mode			$V_{DD} = 5.5 \text{ V}$ $V_{IN} = 5.3 \text{ V} / 0.2 \text{ V}$,	-	0.5	10	μΑ

Note 1: Typical values show those at Topr = 25° C, $V_{DD} = 5 V$.

Note 2: Input Current I_{IN1}, I_{IN3}; The current through resistor is not included, when the input resistor (pull-up/pull-down) is contained.

Note 3: Typical current consumption during AD conversion is 1.2 mA.

AD Conversion Characteristics

 $(V_{SS} = 0 \text{ V}, V_{DD} = 2.7 / 4.5 \text{ to } 5.5 \text{ V}, Topr = -30 \text{ to } 70^{\circ}\text{C})$

Parameter	Symbol	Pins	Conditions	Min	Тур.	Max	Unit
Analog Input Voltage Range	V _{CIN}	CIN5 to CIN0		V _{SS}	-	V_{DD}	V
Conversion Error			$V_{DD} = 5.0 \text{ V}$	-	-	± 1.5	LSB

AC Characteristics

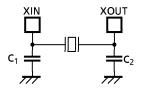
 $(V_{SS} = 0 \text{ V}, V_{DD} = 2.7/4.5 \text{ to } 5.5 \text{ V}, Topr = -30 \text{ to } 70^{\circ}\text{C})$

Parameter	Symbol	Conditions	Min	Тур.	Max	Unit
		In NORMAL1, 2 modes	0.5		10	
Marshina Guela Tina		In IDLE 1, 2 modes	0.5	_		μ\$
Machine Cycle Time	t _{cy}	In SLOW mode	117.6		422.2	
		In SLEEP mode	117.6	_	133.3	
High Level Clock Pulse Width	t _{WCH}	For external clock operation	F0			
Low Level Clock Pulse Width	t _{WCL}	(XIN input), fc = 8 MHz	50	_	_	ns
High Level Clock Pulse Width	t _{WSH}	For external clock operation				
Low Level Clock Pulse Width	t _{WSL}	(XTIN input), fs = 32.768 kHz	14.7	-	ı	μS

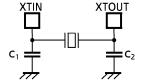
Recommended Oscillating Conditions

$$(V_{SS} = 0 \text{ V}, V_{DD} = 2.7 / 4.5 \text{ to } 5.5 \text{ V}, \text{ Topr} = -30 \text{ to } 70^{\circ}\text{C})$$

Danie na akan	0 111 1	Oscillation	Recommended Oscillator		Recommended Constant		
Parameter	Oscillator	Frequency			C ₁	C ₂	
High-frequency Oscillation		8 MHz	KYOCERA	KBR8.0M			
	Ceramic Resonator	4 MHz	KYOCERA	KBR4.0MS	30 pF	30 pF	
			MURATA	CSA 4.00MG			
	Crystal Oscillator	8 MHz	тоуосом	210B 8.0000			
		4 MHz	тоуосом	204B 4.0000	20 pF	20 pF	
Low-frequency Oscillation	Crystal Oscillator	32.768 kHz	NDK	MX-38T	15 pF	15 pF	



(1) High-frequency Oscillation



(2) Low-frequency Oscillation

Note: An electrical shield by metal shield plate on the surface of the IC package should be recommendable in order to prevent the device from the high electric fieldstress applied for continuous reliable operation.