CMOS 8-Bit Microcontroller

TMP87CM71F, TMP87CN71F, TMP87CP71F, TMP87CS71F

The TMP87CM71/N71/P71/S71 are the high speed and high performance 8-bit single chip microcomputers. These MCU contain 6-bit AD conversion inputs and a VFT (Vacuum Fluorescent Tube) driver on a chip.

Part No.	ROM	RAM	Package	OTP MCU
TMP87CM71F	32 K × 8-bit	1.5 K × 8-bit	P-QFP80-1420-0.80B	TMP87PP71F / TMP87PS71F
TMP87CN71F	40 K × 8-bit			
TMP87CP71F	48 K × 8-bit			
TMP87CS71F	61184 × 8-bit	2.0 K × 8-bit		TMP87PS71F

Features

◆8-bit single chip microcomputer TLCS-870 Series
◆Instruction execution time: 0.5 μs (at 8 MHz), 122 μs (at 32.768 kHz)
◆412 basic instructions
- Multiplication and Division (8 bits × 8 bits , 16 bits ÷ 8 bits)
- Bit manipulations (Set/Clear/Complement/Move/Test/Exclusive or)
- 16-bit data operations
- 1-byte jump/subroutine-call (Short relative jump/ Vector call)

◆14 interrupt sources (External: 5, Internal: 9)
- All sources have independent latches each, and nested interrupt control is available.
- 3 edge-selectable external interrupts with noise reject
- High-speed task switching by register bank changeover

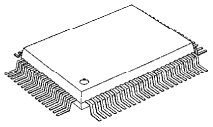
◆10 Input/Output ports (73 pins)
- Output: 1 port (8 pins)
- Input/Output: 9 ports (65 pins)

◆Two 16-bit Timer/Counters
- Timer, Event counter modes

◆Two 8-bit Timer/Counters
- Timer, Event counter, Capture (Pulse width/duty measurement), PWM output, Programmable divider output modes

◆Time Base Timer (Interrupt frequency: 1 Hz to 16 kHz)
◆Divider output function (frequency: 1 kHz to 8 kHz)
◆Watchdog Timer
- Interrupt source/reset output (programmable)

P-QFP80-1420-0.80B



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◆8-bit Serial Interface
- With 8 bytes transmit/receive data buffer
- Internal/external serial clock, and 4/8-bit mode

◆8-bit High Speed Serial Output (rate: max. 1 bit / μs)
◆6-bit AD conversion input (6 channels)
◆Vacuum Fluorescent Tube Driver (automatic display)
- High breakdown voltage ports

◆Key scanning function
- Key-matrix constructed by segment outputs (1 to 16) and key inputs (1 to 8)

◆Dual clock operation
- Single/Dual-clock mode (option)

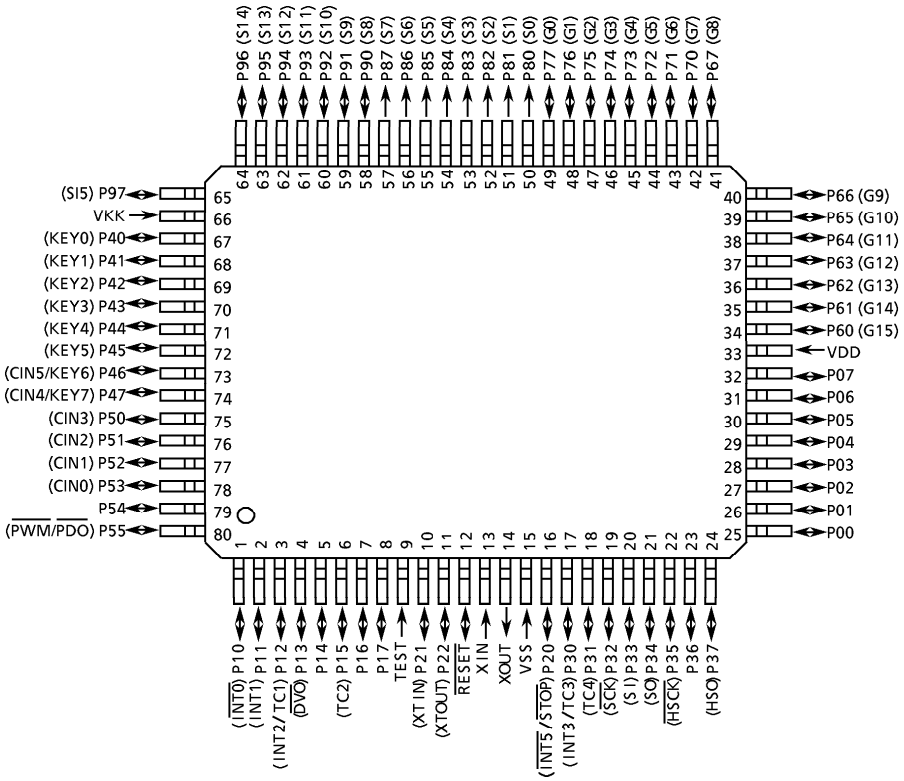
◆Five Power saving operating modes
- STOP mode: Oscillation stops. Battery/Capacitor back-up. Port output hold/High-impedance.
- SLOW mode: Low power consumption operation using low-frequency clock (32.768 kHz).
- IDLE1 mode: CPU stops, and Peripherals operate using high-frequency clock. Release by interrupts.
- IDLE2 mode: CPU stops, and Peripherals operate using high-and low-frequency clock. Release by interrupts.
- SLEEP mode: CPU stops, and Peripherals operate using low-frequency clock. Release by interrupts.

◆Wide operating voltage: 2.7 to 5.5 V at 4.19 MHz/32.768 kHz, 4.5 to 5.5 V at 8 MHz/32.768 kHz (TMP87CM71/N71/P71)
2.7 to 5.5 V at 32.768 kHz, 4.5 to 5.5 V at 8 MHz/32.768 kHz (TMP87CS71)

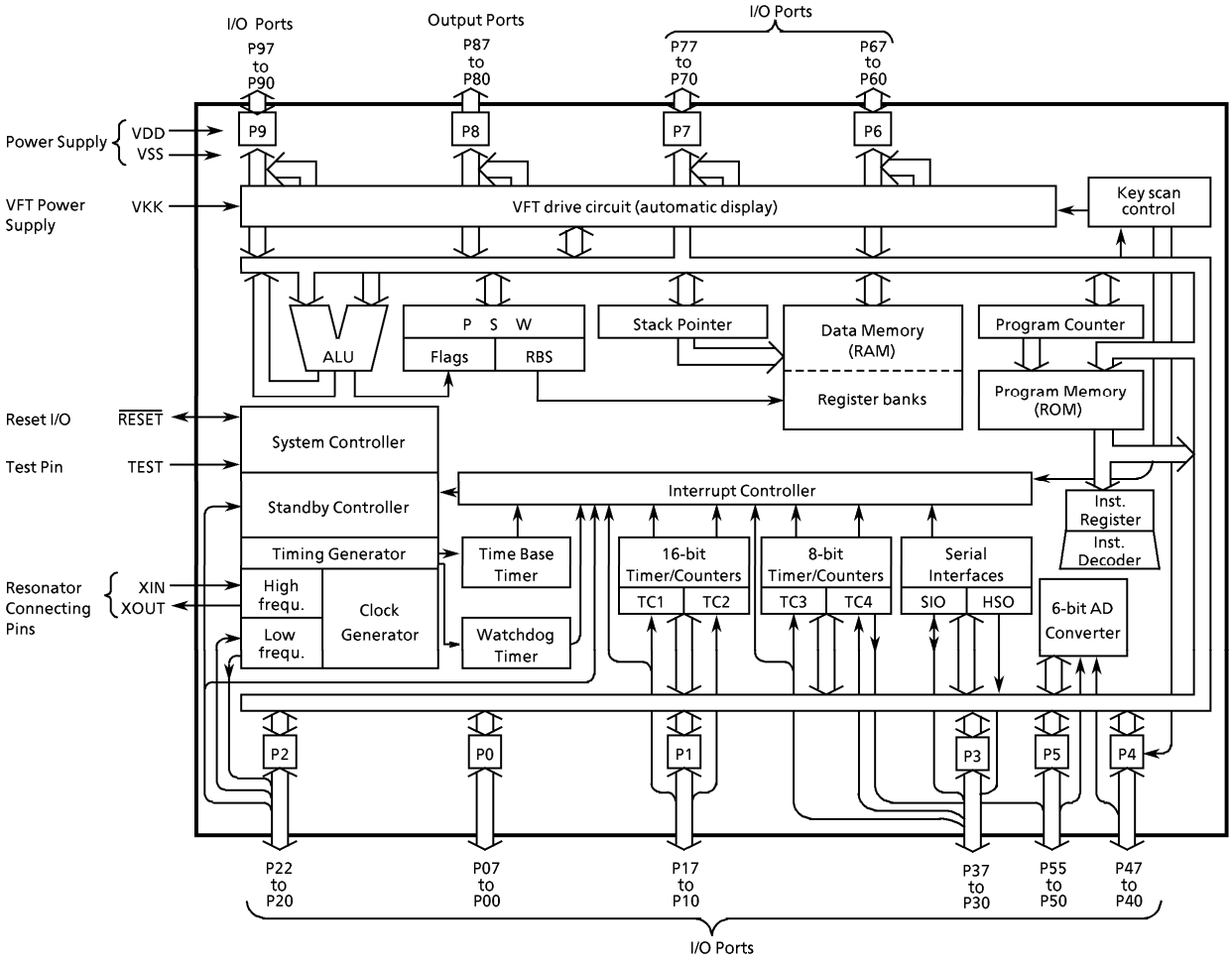
◆Emulation Pod: BM87CK70F0B

Pin Assignments (Top View)

P-QFP80-1420-0.80B



Block Diagram



Pin Function

Pin Name	Input / Output	Function	
P07 to P00	I/O	Two 8-bit programmable input/output ports (tri-state). Each bit of these ports can be individually configured as an input or an output under software control. During reset, all bits are configured as inputs. When used as a divider output, the latch must be set to "1".	
P17, P16, P14	I/O		
P15 (TC2)	I/O (Input)		Timer/Counter 2 input
P13 ($\overline{DVO}$)	I/O (Output)		Divider output
P12 (INT2 / TC1)	I/O (Input)		External interrupt input 2 or Timer/Counter 1 input
P11 (INT1)			External interrupt input 1
P10 ($\overline{INT0}$)			External interrupt input 0
P22 (XTOUT)	I/O (Output)	3-bit input/output port with latch. When used as an input port, the latch must be set to "1".	Resonator connecting pins (32.768 kHz). For inputting external clock, XTIN is used and XTOUT is opened.
P21 (XTIN)	I/O (Input)		
P20 ($\overline{INT5}$ / $\overline{STOP}$)			External interrupt input 5 or STOP mode release signal input
P37 (HSO)	I/O (Output)	8-bit input/output port with latch. When used as an input port, a HSO output, a SIO input/output, a timer/counter input, or an interrupt input, the latch must be set to "1".	HSO serial data output
P36	I/O		
P35 ($\overline{HSCK}$)	I/O (Output)		HSO serial clock output
P34 (SO)			SIO serial data output
P33 (SI)	I/O (Input)		SIO serial data input
P32 ($\overline{SCK}$)	I/O (I/O)		SIO serial clock input/output
P31 (TC4)	I/O (Input)		Timer/Counter 4 input
P30 (INT3 / TC3)			External interrupt input 3 or Timer/Counter 3 input
P47 (CIN4 / KEY7), P46 (CIN5 / KEY6)	I/O (Input)	8-bit input/output port with latch. When used as an input port, the latch must be set to "1".	Comparator inputs or Key scan inputs
P45 (KEY5) to P40 (KEY0)			Key scan inputs
P55 ($\overline{PWM}$ / $\overline{PDO}$)	I/O (Output)	6-bit input/output port with latch. When used as an input port, a comparator input, or a $\overline{PWM}$ / $\overline{PDO}$ output, the latch must be set to "1".	8-bit PWM output or 8-bit programmable divider output
P54	I/O		
P53 (CIN0) to P50 (CIN3)	I/O (Input)		Comparator inputs
P67 (G8) to P60 (G15)	I/O (Output)	Three 8-bit high breakdown voltage I/O ports with the latch. When used as a VFT driver output, the latch must be cleared to"0".	VFT digit driver outputs
P77 (G0) to P70 (G7)			
P97 (S15) to P90 (S8)			VFT segment driver outputs (Key strobe outputs)
P87 (S7) to P80 (S0)	Output (Output)	8-bit high breakdown voltage output port with latch. When used as VFT driver output, the latch must be cleared to"0".	
XIN, XOUT	Input, Output	Resonator connecting pins for high-frequency clock. For inputting external clock, XIN is used and XOUT is opened.	
$\overline{RESET}$	I/O	Reset signal input or watchdog timer output/address-trap-reset output/system-clock-reset output.	
TEST	Input	Test pin for out-going test. Be tied to low.	
VDD, VSS	Power Supply	+ 5 V, 0 V (GND)	
VKK		VFT driver power supply	

Operational Description

1. CPU Core Functions

The CPU core consists of a CPU, a system clock controller, an interrupt controller, and a watchdog timer. This section provides a description of the CPU core, the program memory (ROM), the data memory (RAM), and the reset circuit.

1.1 Memory Address Map

The TLCS-870 Series is capable of addressing 64K bytes of memory. Figure 1-1 shows the memory address maps of the TMP87CM71/N71/P71/S71. In the TLCS-870 Series, the memory is organized 4 address spaces (ROM, RAM, SFR, and DBR). It uses a memory mapped I/O system, and all I/O registers are mapped in the SFR/DBR address spaces. There are 16 banks of general-purpose registers. The register banks are also assigned to the first 128 bytes of the RAM address space.

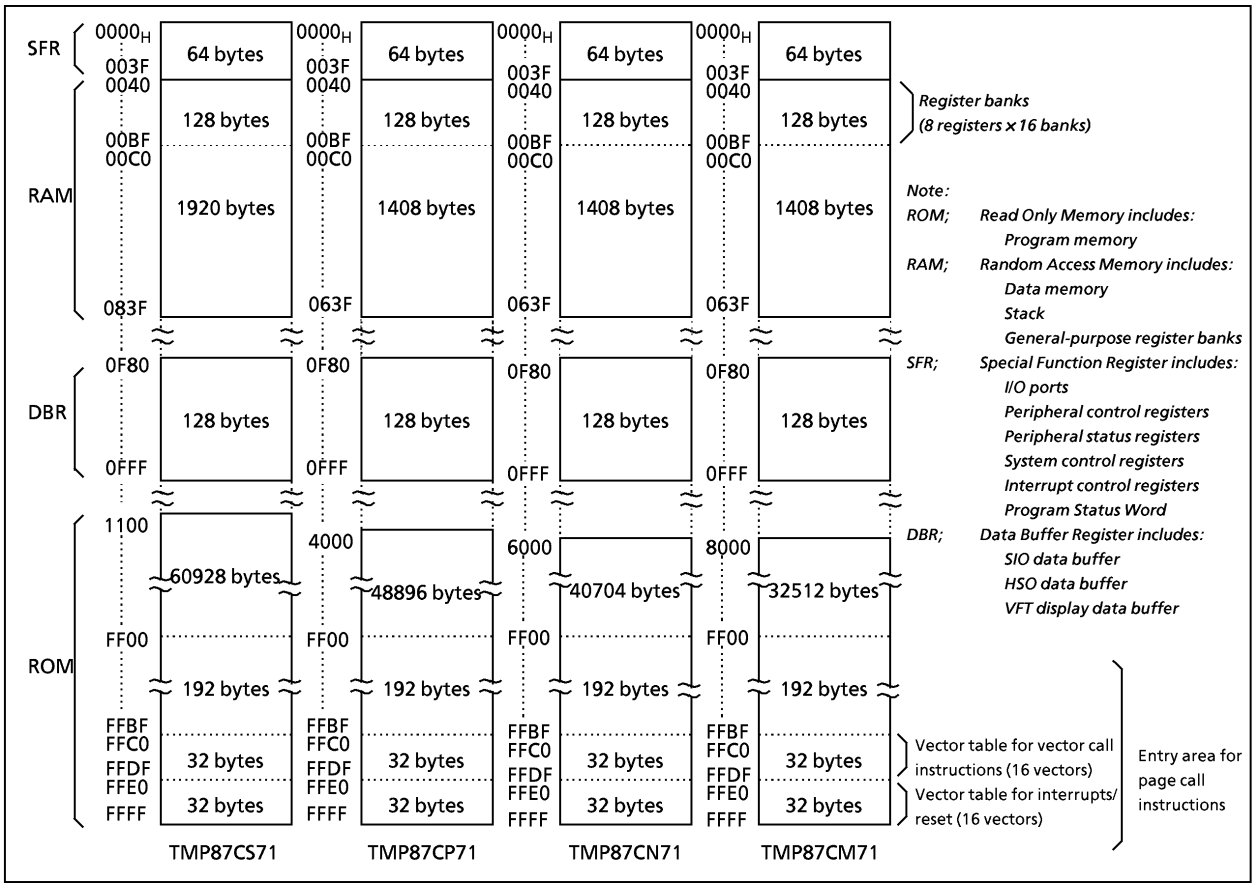


Figure 1-1. Memory Address Maps

Electrical Characteristics

Absolute Maximum Ratings (V_{SS} = 0 V)

Parameter	Symbol	Conditions	Ratings	Unit
Supply Voltage	V_{DD}		– 0.3 to 6.5	V
Input Voltage	V_{IN}		– 0.3 to V_{DD} + 0.3	V
Output Voltage	V_{OUT1}	P2, P3, P4, P5, XOUT, $\overline{RESET}$	– 0.3 to V_{DD} + 0.3	V
	V_{OUT2}	Source open drain ports	V_{DD} – 40 to V_{DD} + 0.3	
Output Current (Per 1 pin)	I_{OUT1}	P0, P1, P2, P3, P4, P5	3.2	mA
	I_{OUT3}	P8, P9 (segment outputs)	– 12	
	I_{OUT4}	P6, P7 (digit outputs)	– 25	
Output Current (Total)	ΣI_{OUT1}	P0, P1, P2, P3, P4, P5	120	mA
	ΣI_{OUT2}	P6, P7, P8, P9	– 120	
Power Dissipation [Topr = 70°C]	PD		350	mW
Soldering Temperature (time)	Tsld		260 (10 s)	°C
Storage Temperature	Tstg		– 55 to 125	°C
Operating Temperature	Topr		– 30 to 70	°C

Note: The absolute maximum ratings are rated values which must not be exceeded during operation, even for an instant. Any one of the ratings must not be exceeded. If any absolute maximum rating is exceeded, a device may break down or its performance may be degraded, causing it to catch fire or explode resulting in injury to the user. Thus, when designing products which include this device, ensure that no absolute maximum rating value will ever be exceeded.

(1) TMP87CM71/N71/P71

Recommended Operating Conditions (V_{SS} = 0 V, Topr = – 30 to 70°C)

Parameter	Symbol	Pins	Conditions		Min	Max	Unit
Supply Voltage	V_{DD}		fc = 8 MHz	NORMAL1, 2 modes	4.5	5.5	V
				IDLE1, 2 modes			
			fc = 4.2 MHz	NORMAL1, 2 modes	2.7		
				IDLE1, 2 modes			
			fs = 32.768 kHz	SLOW mode			
				SLEEP mode			
				STOP mode	2.0		
Input High Voltage	V_{IH1}	Except hysteresis input	$V_{DD} \geqq 4.5$ V		$V_{DD} \times 0.70$	V_{DD}	V
	V_{IH2}	Hysteresis input			$V_{DD} \times 0.75$		
	V_{IH3}		$V_{DD} < 4.5$ V		$V_{DD} \times 0.90$		
Input Low Voltage	V_{IL1}	Except hysteresis input	$V_{DD} \geqq 4.5$ V		0	$V_{DD} \times 0.30$	V
	V_{IL2}	Hysteresis input				$V_{DD} \times 0.25$	
	V_{IL3}		$V_{DD} < 4.5$ V			$V_{DD} \times 0.10$	
Clock Frequency	fc	XIN, XOUT	VDD = 4.5 to 5.5V		0.4	8.0	MHz
			VDD = 2.7 to 5.5V			4.2	
	fs	XTIN, XTOUT			30.0	34.0	kHz

Note: The recommended operating conditions for a device are operating conditions under which it can be guaranteed that the device will operate as specified. If the device is used under operating conditions other than the recommended operating conditions (supply voltage, operating temperature range, specified AC/DC values etc.), malfunction may occur. Thus, when designing products which include this device, ensure that the recommended operating conditions for the device are always adhered to.

(2) TMP87CS71

Recommended Operating Conditions (V_{SS} = 0 V, Topr = – 30 to 70°C)

Parameter	Symbol	Pins	Conditions		Min	Max	Unit
Supply Voltage	V_{DD}		fc = 8 MHz	NORMAL1, 2 modes	4.5	5.5	V
				IDLE1, 2 modes			
			fs = 32.768 kHz	SLOW mode	2.7		
				SLEEP mode			
				STOP mode	2.0		
Input High Voltage	V_{IH1}	Except hysteresis input	$V_{DD} \geqq 4.5$ V		$V_{DD} \times 0.70$	V_{DD}	V
	V_{IH2}	Hysteresis input			$V_{DD} \times 0.75$		
	V_{IH3}		$V_{DD} < 4.5$ V		$V_{DD} \times 0.90$		
Input Low Voltage	V_{IL1}	Except hysteresis input	$V_{DD} \geqq 4.5$ V		0	$V_{DD} \times 0.30$	V
	V_{IL2}	Hysteresis input				$V_{DD} \times 0.25$	
	V_{IL3}		$V_{DD} < 4.5$ V			$V_{DD} \times 0.10$	
Clock Frequency	fc	XIN, XOUT	VDD = 4.5 to 5.5V		0.4	8.0	MHz
	fs	XTIN, XTOUT			30.0	34.0	kHz

DC Characteristics

(V_{SS} = 0 V, Topr = – 30 to 70°C)

Parameter	Symbol	Pins	Conditions		Min	Typ.	Max	Unit
Hysteresis Voltage	V_{HS}	Hysteresis input			–	0.9	–	V
Input Current	I_{IN1}	TEST	V_{DD} = 5.5 V V_{IN} = 5.5 V/0 V		–	–	± 2	μA
	I_{IN2}	Open drain ports, Tri-state ports						
	I_{IN3}	$\overline{RESET}$, $\overline{STOP}$						
Input Resistance	R_{IN1}	Port P4 with pull-down			30	70	150	kΩ
	R_{IN2}	$\overline{RESET}$			100	220	450	
Pull-down Resistance	R_K	Source open drain ports	V_{DD} = 5.5 V, V_{KK} = – 33 V		–	80	–	
Output Leakage Current	I_{LO1}	Sink open drain ports	V_{DD} = 5.5 V, V_{OUT} = 5.5 V		–	–	2	μA
	I_{LO2}	Source open drain ports	V_{DD} = 5.5 V, V_{OUT} = – 33 V		–	–	– 2	
	I_{LO3}	Tri-state ports	V_{DD} = 5.5 V, V_{OUT} = 5.5 V / 0 V		–	–	± 2	
Output High Voltage	V_{OH2}	Tri-state ports	V_{DD} = 4.5 V, I_{OH} = – 0.7 mA		4.1	–	–	V
	V_{OH3}	P8, P9	V_{DD} = 4.5 V, I_{OH} = – 5 mA		2.4	–	–	
Output Low Voltage	V_{OL}	Except XOUT	V_{DD} = 4.5 V, I_{OL} = 1.6 mA		–	–	0.4	V
Output High current	I_{OH}	P6, P7	V_{DD} = 4.5 V, V_{OH} = 2.4 V		–	– 15	–	mA
Supply Current in NORMAL 1, 2 modes	I_{DD}		V_{DD} = 5.5 V fc = 8 MHz fs = 32.768 kHz V_{IN} = 5.3 V / 0.2 V	TMP87CM71/N71/P71	–	10.0	16.0	mA
				TMP87CS71	–	11.0	17.0	
Supply Current in IDLE 1, 2 modes					–	4.5	6.0	
Supply Current in SLOW mode			V_{DD} = 3.0 V fs = 32.768 kHz V_{IN} = 2.8 V / 0.2 V		–	30	60	μA
Supply Current in SLEEP mode					–	15	30	
Supply Current in STOP mode			V_{DD} = 5.5 V V_{IN} = 5.3 V / 0.2 V		–	0.5	10	μA

Note 1: Typical values show those at Topr = 25°C, V_{DD} = 5 V.

Note 2: Input Current I_{IN1}, I_{IN3}; The current through resistor is not included, when the input resistor (pull-up/pull-down) is contained.

Note 3: Typical current consumption during AD conversion is 1.2 mA.

AD Conversion Characteristics

(V_{SS} = 0 V, V_{DD} = 2.7 / 4.5 to 5.5 V, Topr = – 30 to 70°C)

Parameter	Symbol	Pins	Conditions	Min	Typ.	Max	Unit
Analog Input Voltage Range	V_{CIN}	CIN5 to CIN0		V_{SS}	–	V_{DD}	V
Conversion Error			V_{DD} = 5.0 V	–	–	± 1.5	LSB

AC Characteristics

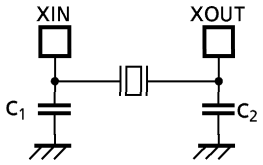
(V_{SS} = 0 V, V_{DD} = 2.7/4.5 to 5.5 V, Topr = – 30 to 70°C)

Parameter	Symbol	Conditions	Min	Typ.	Max	Unit
Machine Cycle Time	t_{cy}	In NORMAL1, 2 modes	0.5	–	10	μs
		In IDLE 1, 2 modes				
		In SLOW mode	117.6	–	133.3	
		In SLEEP mode				
High Level Clock Pulse Width	t_{WCH}	For external clock operation (XIN input), fc = 8 MHz	50	–	–	ns
Low Level Clock Pulse Width	t_{WCL}					
High Level Clock Pulse Width	t_{WSH}	For external clock operation (XTIN input), fs = 32.768 kHz	14.7	–	–	μs
Low Level Clock Pulse Width	t_{WSL}					

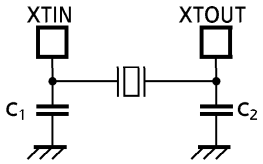
Recommended Oscillating Conditions

(V_{SS} = 0 V, V_{DD} = 2.7 / 4.5 to 5.5 V, Topr = – 30 to 70°C)

Parameter	Oscillator	Oscillation Frequency	Recommended Oscillator		Recommended Constant	
					C_1	C_2
High-frequency Oscillation	Ceramic Resonator	8 MHz	KYOCERA	KBR8.0M	30 pF	30 pF
		4 MHz	KYOCERA	KBR4.0MS		
			MURATA	CSA 4.00MG		
	Crystal Oscillator	8 MHz	TOYOCOM	210B 8.0000	20 pF	20 pF
		4 MHz	TOYOCOM	204B 4.0000		
Low-frequency Oscillation	Crystal Oscillator	32.768 kHz	NDK	MX-38T	15 pF	15 pF



(1) High-frequency Oscillation



(2) Low-frequency Oscillation

Note: An electrical shield by metal shield plate on the surface of the IC package should be recommendable in order to prevent the device from the high electric fieldstress applied for continuous reliable operation.