CMOS 8-Bit Microcontroller

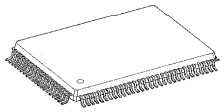
TMP86CS64F

The TMP86CS64 is the high-speed and high-performance 8-bit microcomputer, including a 10-bit AD converter, multi-function timer/counter, serial interface (UART/SIO) and two clock generators on chip.

Product No.	ROM	RAM	Package	OTP MCU
TMP86CS64F	60 K × 8 bits	2 K × 8 bits	P-QFP100-1420-0.65A	TMP86PS64F

Features

P-QFP100-1420-0.65A



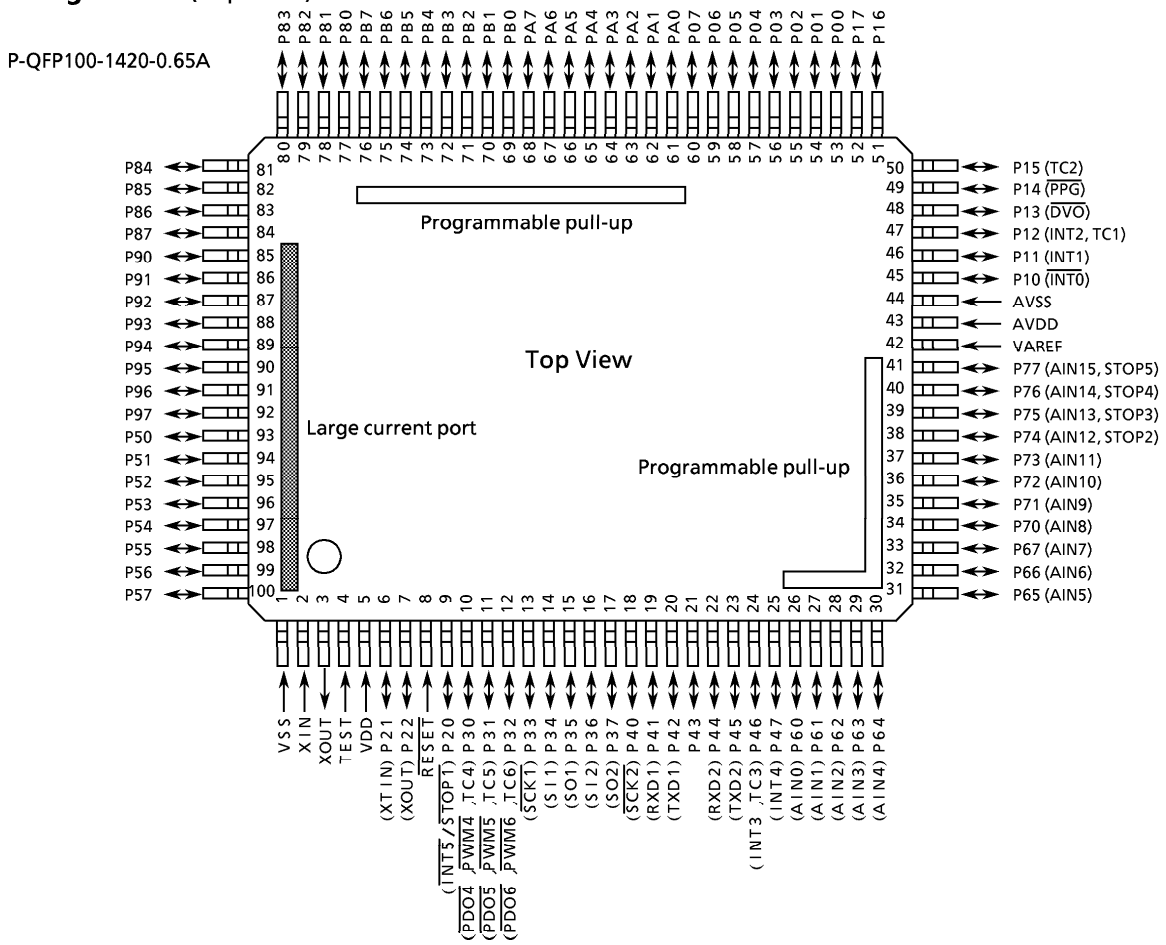
TMP86CS64

- 8-bit single-chip microcomputer TLCS-870/C series microcomputer
- Instruction execution time: 0.25 μs (at 16 MHz)
  122 μs (at 32.768 kHz)
- 132 types and 731 basic instructions
- 21 interrupt sources (External: 6, Internal: 15)
- Input/output ports (91 pins)
  - Large-current output: 16 pins (typ. 20 mA), LED direct drive
- Watchdog timer
- Time base timer
- 16-bit timer counter: 2 channels
  - Timer, event counter, programmable pulse generator (PPG) output, pulse width measurement, external trigger timer, window mode
- 8-bit timer counter: 4 channels
  - Timer, event counter, PWM, PPG output, programmable divider output (PDO)
- 10-bit successive approximation type AD converter with sample and hold
  - Analog input: 16 channel

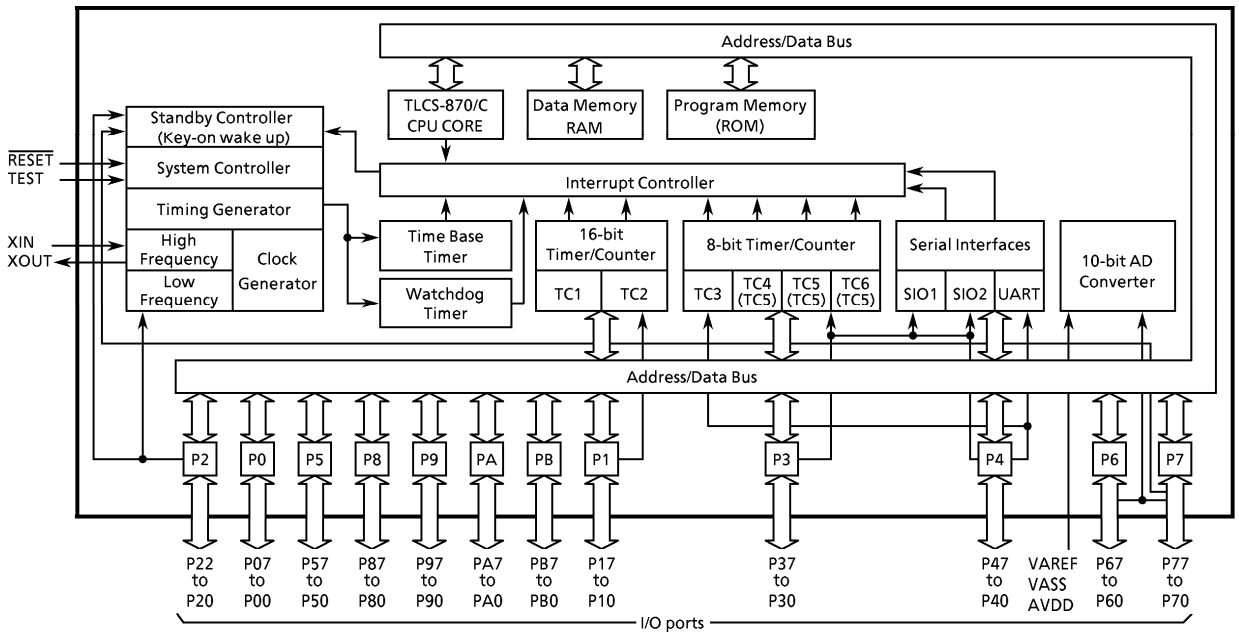
- Serial interface
  - 8-bit SIO: 2 channels
  - 8-bit UART: 1 channel (for IrDA, Selectable use terminal)
- Programmable pull-up: 4 ports
- Key-on-wake-up: 4 channels
- Clock oscillator circuit: 2 lines (Single/Dual-clock mode)
- Low power consumption voltage (9 modes)
  - STOP mode : Oscillation stops (Battery/Capacitor back-up).
  - SLOW1 mode : Low power consumption operation using low-frequency clock (high-frequency clock stop).
  - SLOW2 mode : Low power consumption operation using low-frequency clock (high-frequency clock oscillator).
  - IDLE0 mode : CPU stops, and only the Time Base Timer (TBT) on Peripherals operate using high-frequency clock. Release by falling edge of the source clock which is set by TBTCR<TBTCK>
  - IDLE1 mode : CPU stops, and Peripherals operate using high-frequency clock. Release by interrupts (CPU restarts).
  - IDLE2 mode : CPU stops, and Peripherals operate using high-and low-frequency clock. Release by interruput (CPU restarts).
  - SLEEP0 mode : CPU stops, and only the Time Base Timer (TBT) on Peripherals operate using low-frequency clock. Release by falling edge of the source clock which is set by TBTCR<TBTCK>
  - SLEEP1 mode : CPU stops, and Peripherals operate using low-frequency clock. Release by interrupts (CPU restarts).
  - SLEEP2 mode : CPU stops, and Peripherals operate using high-and low-frequency clock. Release by interrupt (CPU restarts).
- Operating voltage: 4.5 to 5.5 V at 16 MHz/32.768 kHz, 2.7 to 5.5 V at 8 MHz/32.768 kHz

Pin Assignments (Top View)

P-QFP100-1420-0.65A



Block Diagram



Pin Functions (1/3)

Pin Name	I/O	Functions	
P00	I/O	8-bit programmable input/output port. Input or output specified on bit basis.	—
P01			
P02			
P03			
P04			
P05			
P06			
P07			
P10 ($\overline{INT0}$)	I/O (Input)	8-bit programmable input/output port. Input or output specified on bit basis. When using pins for external interrupt input or timer/counter input, set them to input mode. When using pins for DVO output or PPG output, the output latches set to 1.	External interrupt input
P11 (INT1)			External interrupt input
P12 (INT2/TC1)			External interrupt input/ Timer counter input
P13 ($\overline{DVO}$)	I/O (Output)		DVO output
P14 ($\overline{PPG}$)			PPG output
P15 (TC2)	I/O (Input)		Timer counter input
P16	I/O		—
P17			—
P20 ($\overline{STOP1}$/$\overline{INT5}$)	I/O (Input)	3-bit input/output ports. When used as input port, external interrupt input, STOP mode release signal input, the input mode is configured.	STOP mode release input/ External interrupt input
P21 (XTIN)	I/O (Output)		Low-frequency oscillator connecting pin
P22 (XTOUT)			
P30 (TC4/$\overline{PWM4}$/$\overline{PDO4}$)	I/O (Input/Output/Output)	8-bit programmable input/output port. Input or output specified on bit basis. When using pins for timer/counter input or SI, set them to input mode. When using pins PWM output, PDO output or SO, set them to output mode.	Timer/Counter input PWM output/ PDO output
P31 (TC5/$\overline{PWM5}$/$\overline{PDO5}$)			
P32 (TC6/$\overline{PWM6}$/$\overline{PDO6}$)			
P33 ($\overline{SCK1}$)	I/O (Input/Output)		SIO clock input/output
P34 (SI1)	I/O (Input)		SIO input
P35 (SO1)	I/O (Output)		SIO output
P36 (SI2)	I/O (Input)		SIO input
P37 (SO2)	I/O (Output)		SIO output
P40 ($\overline{SCK2}$)	I/O (Input/Output)	8-bit programmable input/output port. Input or output specified on bit basis. When using pins for UART, set to output latches. When using pins for open-drain output, set to P4ODE and P4CR.	SIO clock input/output
P41 (RXD1)	I/O (Input)		UART data input
P42 (TXD1)	I/O (Output)		UART data output
P43	I/O		—
P44 (RXD2)	I/O (Input)		UART data input
P45 (TXD2)	I/O (Output)		UART data output
P46 (INT3/TC3)	I/O (Input)		External interrupt input/ Timer counter input
P47 (INT4)			External interrupt input

Pin Functions (2/3)

Pin Name	I/O	Functions	
P50	I/O	8-bit programmable input/output ports. Input or output specified on bit basis. With a Nch large current output, the direct operation of LED enable.	—
P51			
P52			
P53			
P54			
P55			
P56			
P57			
P60 (AIN0)	I/O (Input)	8-bit programmable input/output port. Input or output specified on bit basis. Programmable pull-up enable.	AD converter analog input
P61 (AIN1)			
P62 (AIN2)			
P63 (AIN3)			
P64 (AIN4)			
P65 (AIN5)			
P66 (AIN6)			
P67 (AIN7)			
P70 (AIN8)	I/O (Input)	8-bit programmable input/output port. Input or output specified on bit basis. Programmable pull-up enable.	AD converter analog input
P71 (AIN9)			
P72 (AIN10)			
P73 (AIN11)			
P74 (AIN12/STOP2)			AD converter analog input STOP mode release input
P75 (AIN13/STOP3)			
P76 (AIN14/STOP4)			
P77 (AIN15/STOP5)			
P80	I/O	8-bit programmable input/output port. Input or output specified on bit basis.	—
P81			
P82			
P83			
P84			
P85			
P86			
P87			
P90	I/O	8-bit programmable input/output port. Input or output specified on bit basis. With a Nch large current output, the direct operation of LED enable.	—
P91			
P92			
P93			
P94			
P95			
P96			
P97			

Pin Functions (3/3)

Pin Name	I/O	Functions	
PA0	I/O	8-bit programmable input/output ports. Input or output specified on bit basis. Programmable pull-up enable.	—
PA1			
PA2			
PA3			
PA4			
PA5			
PA6			
PA7			
PB0	I/O	8-bit programmable input/output port. Input or output specified on bit basis. Programmable pull-up enable.	—
PB1			
PB2			
PB3			
PB4			
PB5			
PB6			
PB7			
TEST	Input	Shipment test pin, fix to "L" level	
$\overline{\text{RESET}}$	Input	—	
XIN	Input	High-frequency oscillator connecting pins.For external clock input, input to XIN and leave XOUT open.	
XOUT	Output		
VSS	Power supply	GND	
VDD		VCC	
AVSS		Analog voltage for AD conversion.	
AVDD		Analog voltage for AD conversion.	
VAREF		Analog reference voltae for AD conversion.	

Operational Description

1. CPU Core Functions

The CPU core consists of a CPU, a system clock controller, and an interrupt controller.

This section provides a description of the CPU core, the program memory, the data memory, and the reset circuit.

1.1 Memory Address Map

The TMP86C8S64 memory consist of 4 blocks: ROM, RAM, DBR (Data Buffer Register) and SFR (Special Function Register). They are all mapped in 64 Kbyte address space. Figure 1-1 shows the TMP86CS64 memory address map. The general-purpose registers are not assigned to the RAM address space.

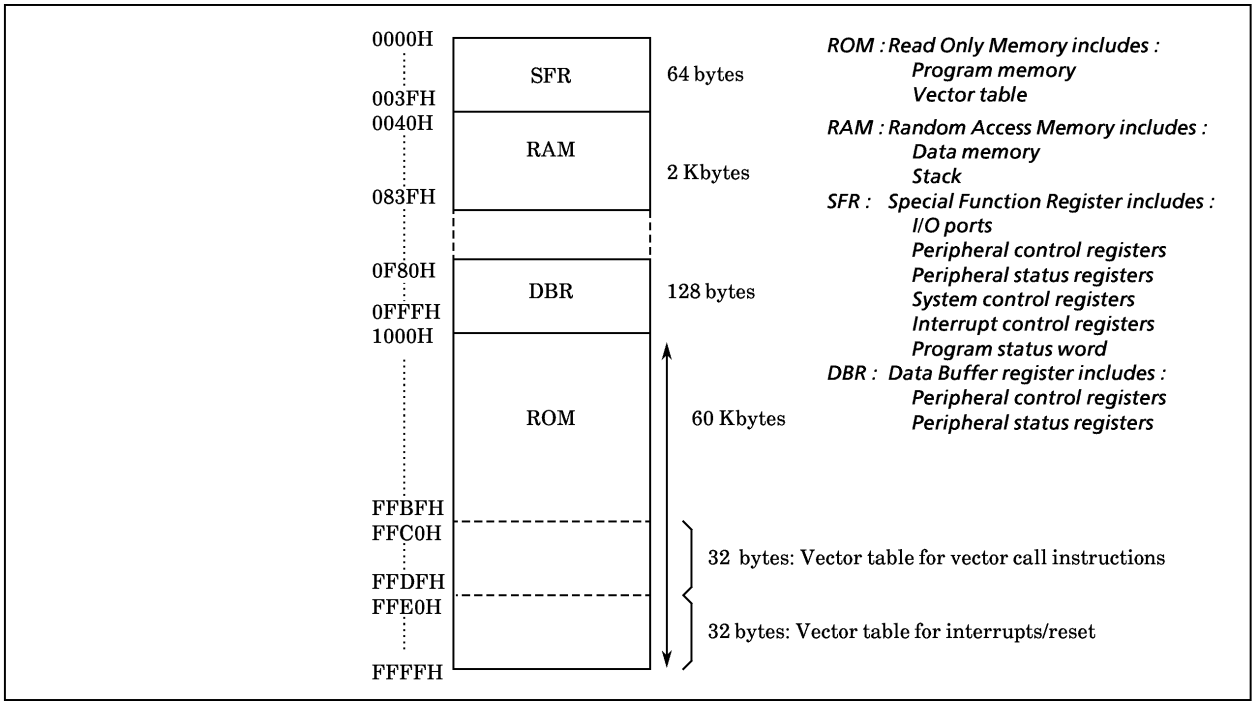


Figure 1-1. Memory Address Map

1.2 Program Memory (ROM)

The TMP86CS64 has a 60 K×8 bits (Address 1000H to FFFFH) of program memory (mask programmed ROM). However, placing program memory on the internal RAM is deregulated if a certain procedure is executed (See 2.4.5 Address trap).

Electrical Characteristics

Absolute Maximum Ratings (V_{SS} = 0 V)

Parameter	Symbol	Pins	Ratings	Unit
Supply Voltage	V_{DD}		– 0.3 to 6.5	V
Input Voltage	V_{IN}		– 0.3 to V_{DD} + 0.3	
Output Voltage	V_{OUT}		– 0.3 to V_{DD} + 0.3	
Output Current (Per 1 pin)	I_{OUTH}		– 3.2	mA
	I_{OUT1}	Except P5, P9	3.2	
	I_{OUT2}	P5	30	
	I_{OUT3}	P9		
Output Current (Total)	ΣI_{OUT1}	Except P5, P9	60	
	ΣI_{OUT2}	P5		
	ΣI_{OUT3}	P9		
Power Dissipation [T_{opr} = 85°C]	PD		250	mW
Soldering Temperature (time)	Tsld		260 (10 s)	°C
Storage Temperature	Tstg		– 55 to 125	
Operating Temperature	Topr		– 40 to 85	

Note: The absolute maximum ratings are rated values which must not be exceeded during operation, even for an instant. Any one of the ratings must not be exceeded. If any absolute maximum rating is exceeded, a device may break down or its performance may be degraded, causing it to catch fire or explode resulting in injury to the user. Thus, when designing products which include this device, ensure that no absolute maximum rating value will ever be exceeded.

Recommended Operating Condition (V_{SS} = 0 V, Topr = – 40 to 85°C)

Parameter	Symbol	Pins	Condition		Min	Max	Unit
Supply Voltage	V_{DD}		fc = 1 to 16 MHz	Each operation modes	4.5	5.5	V
			fc = 1 to 8 MHz	Each operation modes	2.7	5.5	
			fs = 32.768 kHz	Each operation modes	2.7	5.5	
			STOP mode		2.0	5.5	
Input high Level	V_{IH1}	Hysteresis	$V_{DD} \geqq 4.5$ V		V_{DD} × 0.70	V_{DD}	
	V_{IH2}	Hysteresis			V_{DD} × 0.75		
	V_{IH3}		$V_{DD} < 4.5$ V		V_{DD} × 0.90		
Input low Level	V_{IL1}	Hysteresis	$V_{DD} \geqq 4.5$ V		0	V_{DD} × 0.30	
	V_{IL2}	Hysteresis				V_{DD} × 0.25	
	V_{IL3}		$V_{DD} < 4.5$ V			V_{DD} × 0.10	
Clock Frequency	fc	XIN, XOUT	V_{DD} = 4.5 to 5.5 V		1.0	16.0	MHz
			V_{DD} = 2.7 to 5.5 V			8.0	
	fs	XTEN, XTOUT			30.0	34.0	kHz

Note: The recommended operating conditions for a device are operating conditions under which it can be guaranteed that the device will operate as specified. If the device is used under operating conditions other than the recommended operating conditions (supply voltage, operating temperature range, specified AC/DC values etc.), malfunction may occur. Thus, when designing products which include this device, ensure that the recommended operating conditions for the device are always adhered to.

DC Characteristics (V_{SS} = 0 V, Topr = – 40 to 85°C)

Parameter	Symbol	Pins	Condition	Min	Typ.	Max	Unit
Hysteresis Voltage	V_{HS}	Hysteresis input		–	0.9	–	V
Input Current	I_{IN1}	TEST	V_{DD} = 5.5 V, V_{IN} = 5.5 V/0 V	–	–	± 2	μA
	I_{IN2}	Sink Open Drain, Tri-state port					
	I_{IN3}	$\overline{STOP}$, $\overline{RESET}$					
Input Resistance	R_{IN1}	TEST		–	70	–	kΩ
	R_{IN2}	$\overline{RESET}$		100	220	450	
	R_{IN3}	Programmable pull up (P6, P7, PA, PB)	V_{DD} = 5.5 V	40	80	200	
OSC. Feedback resistance	Rfx	XIN-XOUT		–	1.2	–	MΩ
	Rfxt	XTIN-XTOUT		–	6	–	
Output Leakage Current	I_{LO1}	Sink Open Drain port	V_{DD} = 5.5 V, V_{OUT} = 5.5 V	–	–	2	μA
	I_{LO2}	Tri-state port	V_{DD} = 5.5 V, V_{OUT} = 5.5 V/0 V	–	–	± 2	
"H" output Voltage	V_{OH}	Tri-state port	V_{DD} = 4.5 V, I_{OH} = – 0.7 mA	4.1	–	–	V
"L" output Voltage	V_{OL3}	P5, P9	V_{DD} = 4.5 V, I_{OL} = 1.6 mA	–	–	0.4	
"L" output Current	I_{OL1}	Except P5, P9	V_{DD} = 4.5 V, V_{OL} = 0.4 V	–	1.6	–	mA
	I_{OL3}	High current port (P5, P9)	V_{DD} = 4.5 V, V_{OL} = 1.0 V	–	20	–	
Supply Current in Normal 1, 2 mode	I_{DD}		V_{DD} = 5.5 V V_{IN} = 5.3 V/0.2 V fc = 16 MHz fs = 32.768 kHz	–	7	8	
Supply Current in IDLE 1, 2 mode				–	4	5	
Supply Current in SLOW 1 mode			V_{DD} = 3.0 V V_{IN} = 2.8 V/0.2 V fs = 32.768 kHz	–	10	20	μA
Supply Current in SLEEP 0, 1 mode				–	6	12	
Supply Current in STOP mode			V_{DD} = 5.5 V V_{IN} = 5.3 V/0.2 V	–	0.5	10	

Note 1: Typical values show those at Topr = 25°C, V_{DD} = 5 V
Note 2: Input current (I_{IN1}, I_{IN3}); The current through pull-up or pull-down resistor is not included.
Note 3: I_{DD} does not include I_{REF} current.

AD Conversion Characteristics (V_{SS} = 0 V, 4.5 V ≦ V_{DD} ≦ 5.5 V, Topr = – 40 to 85°C)

Parameter	Symbol	Condition	Min	Typ.	Max	Unit
Analog Reference Voltage	V_{AREF}		A_{VDD} – 1.0	–	A_{VDD}	V
Power Supply Voltage of Analog Control Circuit	A_{VDD}		V_{DD}			
	A_{VSS}		V_{SS}			
Analog Reference of Voltage Range	$\triangle V_{AREF}$		3.5	–	V_{DD}	
Analog Input Voltage	V_{AIN}		V_{SS}	–	V_{AREF}	
Power Supply Current of Analog Reference Voltage	I_{REF}	$V_{DD} = A_{VDD} = V_{AREF}$ = 5.5 V $V_{SS} = A_{VSS}$ = 0.0 V	–	0.6	1.0	mA
Non linearity Error		$V_{DD} = A_{VDD}$ = 5.0 V $V_{SS} = A_{VSS}$ = 0.0 V V_{AREF} = 5.0 V	–	–	± 2	LSB
Zero Point Error			–	–	± 2	
Full Scale Error			–	–	± 2	
Total Error			–	–	± 4	

(V_{SS} = 0 V, 2.7 V ≦ V_{DD} < 4.5 V, Topr = – 40 to 85°C)

Parameter	Symbol	Condition	Min	Typ.	Max	Unit
Analog Reference Voltage	V_{AREF}		A_{VDD} – 1.0	–	A_{VDD}	V
Power Supply Voltage of Analog Control Circuit	A_{VDD}		V_{DD}			
	A_{VSS}		V_{SS}			
Analog Reference of Voltage Range	$\triangle V_{AREF}$		2.5	–	V_{DD}	
Analog Input Voltage	V_{AIN}		V_{SS}	–	V_{AREF}	
Power Supply Current of Analog Reference Voltage	I_{REF}	$V_{DD} = A_{VDD} = V_{AREF}$ = 4.5 V $V_{SS} = A_{VSS}$ = 0.0 V	–	0.5	0.8	mA
Non linearity Error		$V_{DD} = A_{VDD}$ = 2.7 V $V_{SS} = A_{VSS}$ = 0.0 V V_{AREF} = 2.7 V	–	–	± 2	LSB
Zero Point Error			–	–	± 2	
Full Scale Error			–	–	± 2	
Total Error			–	–	± 4	

Note 1: Total error includes all error except a quantization error, and is defined as a maximum deviation from the ideal conversion line.

Note 2: Conversion time is different in recommended value by power supply voltage.
About conversion time, please refer to "2.14.2 Register Framing".

Note 3: Please use input voltage to AIN input Pin in limit of V_{AREF} - V_{SS}.
When voltage of range outside is input, conversion value becomes unsettled and gives affect to other channel conversion value.

Note 4: Analog Reference Voltage Range: $\triangle V_{AREF} = V_{AREF} - A_{VSS}$

AC Characteristics (V_{SS} = 0 V, V_{DD} = 4.5 to 5.5 V, Topr = – 40 to 85°C)

Parameter	Symbol	Condition	Min	Typ.	Max	Unit
Machine Cycle Time	tcy	NORMAL 1, 2 mode	0.25	–	4	μs
		IDLE 0, 1, 2 mode				
		SLOW 1, 2 mode	117.6	–	133.3	
		SLEEP 0, 1, 2 mode				
High Level Clock Pulse Width	t_{WCH}	For external clock operation (XIN input) fc = 16 MHz	–	31.25	–	ns
Low Level Clock Pulse Width	t_{WCL}					
High Level Clock Pulse Width	t_{WSH}	For external clock operation (XTIN input) fs = 32.768 kHz	–	15.26	–	μs
Low Level Clock Pulse Width	t_{WSL}					

(V_{SS} = 0 V, V_{DD} = 2.7 to 4.5 V , Topr = – 40 to 85°C)

Parameter	Symbol	Condition	Min	Typ.	Max	Unit
Machine Cycle Time	tcy	NORMAL 1, 2 mode	0.5	–	4	μs
		IDLE 0, 1, 2 mode				
		SLOW 1, 2 mode	117.6	–	133.3	
		SLEEP 0, 1, 2 mode				
High Level Clock Pulse Width	t_{WCH}	For external clock operation (XIN input) fc = 8 MHz	–	62.5	–	ns
Low Level Clock Pulse Width	t_{WCL}					
High Level Clock Pulse Width	t_{WSH}	For external clock operation (XTIN input) fs = 32.768 kHz	–	15.26	–	μs
Low Level Clock Pulse Width	t_{WSL}					

Recommended Oscillating Conditions-1

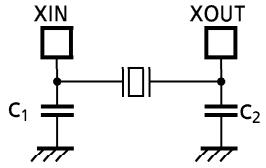
(V_{SS} = 0 V, V_{DD} = 4.5 to 5.5 V, Topr = – 40 to 85°C)

Parameter	Oscillator	Oscillation Frequency	Recommended Oscillator		Recommended Constant C_1	Recommended Constant C_2
High-frequency Oscillation	Ceramic Resonator	16 MHz	MURATA	CSA16.00MXZ040	10 pF	10 pF
		8 MHz	MURATA	CSA8.00MTZ	30 pF	30 pF
				CST8.00MTW	30 pF (built-in)	30 pF (built-in)
		4.19 MHz	MURATA	CSA4.19MG	30 pF	30 pF
				CST4.19MGW	30 pF (built-in)	30 pF (built-in)
Low-frequency Oscillation	Crystal Oscillator	32.768 kHz	SII	VT-200	6 pF	6 pF

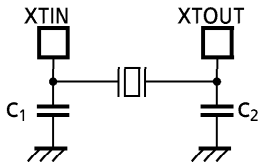
Recommended Oscillating Conditions-2

(V_{SS} = 0 V, V_{DD} = 2.7 to 5.5 V, Topr = – 40 to 85°C)

Parameter	Oscillator	Oscillation Frequency	Recommended Oscillator		Recommended Constant C_1	Recommended Constant C_2
High-frequency Oscillation	Ceramic Resonator	8 MHz	MURATA	CSA8.00MTZ	30 pF	30 pF
				CST8.00MTW	30 pF (built-in)	30 pF (built-in)
		4.19 MHz	MURATA	CSA4.19MG	30 pF	30 pF
				CST4.19MGW	30 pF (built-in)	30 pF (built-in)



(1) High-frequency Oscillation



(2) Low-frequency Oscillation

Note 1: An electrical shield by metal shield plate on the surface of IC package is recommended in order to protect the device from the high electric field stress applied from CRT (Cathodic Ray Tube) for continuous reliable operation.

Note 2: The product numbers and specifications of the resonators by Murata Manufacturing Co., Ltd. are subject to change. For up-to-date information, please refer to the following URL;
http://www.murata.co.jp/search/index.html