#### CMOS 8-Bit Microcontroller

### TMP86CS64F

The TMP86CS64 is the high-speed and high-performance 8-bit microcomputer, including a 10-bit AD converter, multi-function timer/counter, serial interface (UART/SIO) and two clock generators on chip.

Product No.	ROM	RAM	Package	OTP MCU
TMP86CS64F	60 K × 8 bits	2 K × 8 bits	P-QFP100-1420-0.65A	TMP86PS64F

#### **Features**

- ◆ 8-bit single-chip microcomputer TLCS-870/C series microcomputer
- Instruction execution time:  $0.25 \mu s$  (at 16 MHz)  $122 \mu s (at 32.768 \text{ kHz})$
- ◆ 132 types and 731 basic instructions
- 21 interrupt sources (External: 6, Internal: 15)
- Input/output ports (91 pins)
  - Large-current output: 16 pins (typ. 20 mA), LED direct drive
- Watchdog timer
- Time base timer
- 16-bit timer counter: 2 channels
  - Timer, event counter, programmable pulse generator (PPG) output, pulse width measurement, external trigger timer, window mode
- 8-bit timer counter: 4 channels
  - Timer, event counter, PWM, PPG output, programmable divider output (PDO)
- ◆ 10-bit successive approximation type AD converter with sample and hold
  - Analog input: 16 channel



For a discussion of how the reliability of microcontrollers can be predicted, please refer to Section 1.3 of the chapter entitled Quality and Reliability Assurance / Handling Precautions.

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- making a safe design for the entire system, and to avoid situations in which a malfunction or failure of such TOSHIBA products could cause loss of human life, bodily injury or damage to property.

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P-QFP100-1420-0.65A

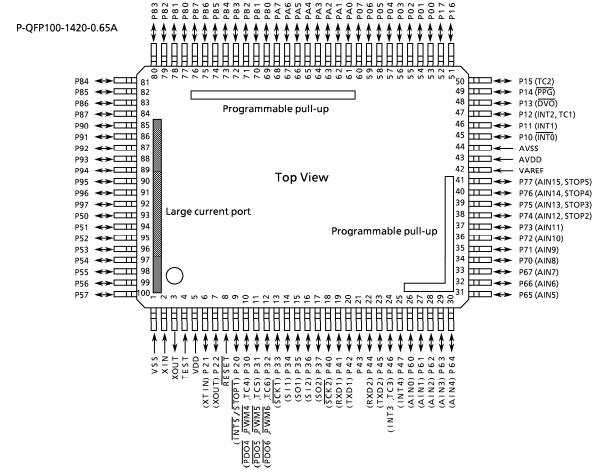
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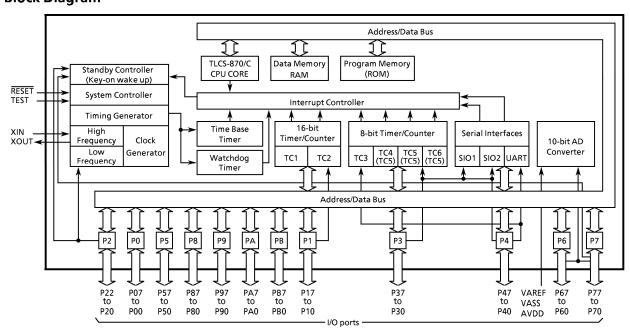
- ♦ Serial interface
  - 8-bit SIO: 2 channels
  - 8-bit UART: 1 channel (for IrDA, Selectable use terminal)
- ♦ Programmable pull-up: 4 ports
- ♦ Key-on-wake-up: 4 channels
- ♦ Clock oscillator circuit: 2 lines (Single/Dual-clock mode)
- ◆ Low power consumption voltage (9 modes)
  - STOP mode : Oscillation stops (Battery/Capacitor back-up).
  - SLOW1 mode: Low power consumption operation using low-frequency clock (high-frequency clock stop).
  - SLOW2 mode: Low power consumption operation using low-frequency clock (high-frequency clock oscillator).
  - IDLE0 mode : CPU stops, and only the Time Base Timer (TBT) on Peripherals operate using high-frequency clock. Release by falling edge of the source clock which is set by TBTCR<TBTCK>
  - IDLE1 mode : CPU stops, and Peripherals operate using high-frequency clock. Release by interrupts (CPU restarts).
  - IDLE2 mode : CPU stops, and Peripherals operate using high-and low-frequency clock. Release by interruput (CPU restarts).
  - SLEEP0 mode: CPU stops, and only the Time Base Timer (TBT) on Peripherals operate using low-frequency clock. Release by falling edge of the source clock which is set by TBTCR<TBTCK>
  - SLEEP1 mode: CPU stops, and Peripherals operate using low-frequency clock. Release by interrupts (CPU restarts).
  - SLEEP2 mode: CPU stops, and Peripherals operate using high-and low-frequency clock. Release by interrupt (CPU restarts).
- ◆ Operating voltage: 4.5 to 5.5 V at 16 MHz/32.768 kHz, 2.7 to 5.5 V at 8 MHz/32.768 kHz

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## Pin Assignments (Top View)



## **Block Diagram**



# Pin Functions (1/3)

Pin Name	1/0	Functions	
P00			
P01	1		
P02	1		
P03	1	8-bit programmable input/output port.	_
P04		Input or output specified on bit basis.	
P05			
P06	1		
P07	1		
P10 (INTO)			External interrupt input
P11 (INT1)	I/O (Input)		External interrupt input
P12 (INT2/TC1)	- "O (mpaty	8-bit programmable input/output port. Input or output specified on bit basis.	External interrupt input/ Timer counter input
P13 (DVO)	1/0 (0++)	When using pins for external interrupt input or	DVO output
P14 (PPG)	l/O (Output)	timer/counter input, set them to input mode. When using pins for DVO output or PPG	PPG output
P15 (TC2)	I/O (Input)	output, the output latches set to 1.	Timer counter input
P16	1/0		_
P17	1/0		_
P20 (STOP1/INT5)	I/O (Input)	3-bit input/output ports. When used as input port, external interrupt	STOP mode release input/ External interrupt input
P21 (XTIN)	I/O (Output)	input, STOP mode release signal input, the	Low-frequency oscillator
P22 (XTOUT)	70 (Output)	input mode is configured.	connecting pin
P30 (TC4/PWM4/PDO4)			
P31 (TC5/PWM5/PDO5) P32	I/O (Input/Output/Output)	8-bit programmable input/output port.	Timer/Counter input PWM output/ PDO output
(TC6/PWM6/PDO6)		Input or output specified on bit basis. When using pins for timer/counter input or SI,	
P33 (SCK1)	I/O (Input/Output)	set them to input mode. When using pins PWM output, PDO output or SO, set them to	SIO clock input/output
P34 (SI1)	I/O (Input)	output mode.	SIO input
P35 (SO1)	I/O (Output)		SIO output
P36 (SI2)	I/O (Input)		SIO input
P37 (SO2)	I/O (Output)		SIO output
P40 (SCK2)	I/O (Input/Output)		SIO clock input/output
P41 (RXD1)	I/O (Input)		UART data input
P42 (TXD1)	I/O (Output)	8-bit programmable input/output port.	UART data output
P43	1/0	Input or output specified on bit basis.	_
P44 (RXD2)	I/O (Input)	When using pins for UART, set to output latches. When using pins for open-drain	UART data input
P45 (TXD2)	I/O (Output)	output, set to P4ODE and P4CR.	UART data output
P46 (INT3/TC3)	] I/O (Input)		External interrupt input/ Timer counter input
P47 (INT4)			External interrupt input

# Pin Functions (2/3)

Pin Name	I/O	Functions			
P50					
P51					
P52		O hit was a second by its and to stand a second			
P53	1/0	8-bit programmable input/output ports. Input or output specified on bit basis.	_		
P54	1/0	With a Nch large current output, the direct			
P55		operation of LED enable.			
P56					
P57					
P60 (AIN0)					
P61 (AIN1)					
P62 (AIN2)					
P63 (AIN3)	1/0 (1000)	8-bit programmable input/output port.	AD annuarious analysis in must		
P64 (AIN4)	l/O (Input)	Input or output specified on bit basis. Programmable pull-up enable.	AD converter analog input		
P65 (AIN5)					
P66 (AIN6)					
P67 (AIN7)					
P70 (AIN8)					
P71 (AIN9)					
P72 (AIN10)		8-bit programmable input/output port. Input or output specified on bit basis.	AD converter analog input		
P73 (AIN11)	1/0 (1000)				
P74 (AIN12/STOP2)	I/O (Input)	Programmable pull-up enable.			
P75 (AIN13/STOP3)			AD converter analog input		
P76 (AIN14/STOP4)			STOP mode release input		
P77 (AIN15/STOP5)					
P80					
P81					
P82					
P83		8-bit programmable input/output port.			
P84	1/0	Input or output specified on bit basis.	_		
P85					
P86					
P87					
P90					
P91					
P92		9 hit programmable input/output part			
P93	1/0	8-bit programmable input/output port. Input or output specified on bit basis.	_		
P94	] 1/0	With a Nch large current output, the direct operation of LED enable.			
P95		operation of LED enable.			
P96					
P97					

# Pin Functions (3/3)

Pin Name	I/O	Functions					
PA0							
PA1	1						
PA2							
PA3	]	8-bit programmable input/output ports.					
PA4	1/0	Input or output specified on bit basis. Programmable pull-up enable.	_				
PA5							
PA6							
PA7							
PB0							
PB1							
PB2							
PB3		8-bit programmable input/output port.					
PB4	1/0	Input or output specified on bit basis. — Programmable pull-up enable.	_				
PB5							
PB6							
PB7							
TEST	Input	Shipment test pin, fix to "L" level					
RESET	Input	_					
XIN	Input	High-frequency oscillator connecting pins.For ex	ternal clock input, input to XIN				
хоит	Output	and leave XOUT open.					
VSS		GND					
VDD		vcc					
AVSS	Power supply	Analog voltage for AD conversion.					
AVDD		Analog voltage for AD conversion.					
VAREF		Analog reference voltae for AD conversion.					

### **Operational Description**

#### 1. CPU Core Functions

The CPU core consists of a CPU, a system clock controller, and an interrupt controller.

This section provides a description of the CPU core, the program memory, the data memory, and the reset circuit.

#### 1.1 Memory Address Map

The TMP86C8S64 memory consist of 4 blocks: ROM, RAM, DBR (Data Buffer Register) and SFR (Special Function Register). They are all mapped in 64 Kbyte address space. Figure 1-1 shows the TMP86CS64 memory address map. The general-purpose registers are not assigned to the RAM address space.

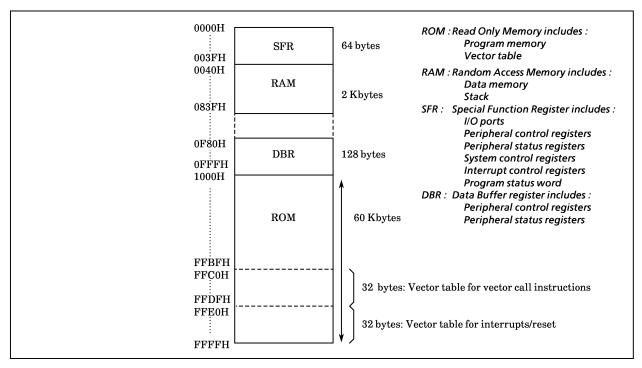


Figure 1-1. Memory Address Map

#### 1.2 Program Memory (ROM)

The TMP86CS64 has a 60 K×8 bits (Address 1000H to FFFFH) of program memory (mask programmed ROM). However, placing program memory on the internal RAM is deregulated if a certain procedure is executed (See 2.4.5 Address trap).

#### **Electrical Characteristics**

Absolute Maximum Ratings  $(V_{SS} = 0 V)$ 

Parameter	Symbol	Pins	Ratings	Unit
Supply Voltage	V <sub>DD</sub>		- 0.3 to 6.5	
Input Voltage	V <sub>IN</sub>		- 0.3 to V <sub>DD</sub> + 0.3	v
Output Voltage	V <sub>OUT</sub>		- 0.3 to V <sub>DD</sub> + 0.3	
	I <sub>OUTH</sub>		- 3.2	
Output Compant (Ban 1 min)	I <sub>OUT1</sub>	Except P5, P9	3.2	
Output Current (Per 1 pin)	I <sub>OUT2</sub>	P5	20	mA
	I <sub>OUT3</sub>	P9	- 30	'''
	Σl <sub>OUT1</sub>	Except P5, P9		
Output Current (Total)	ΣI <sub>OUT2</sub>	P5	60	
	ΣI <sub>OUT3</sub>	P9		
Power Dissipation [T <sub>opr</sub> = 85℃]	PD		250	mW
Soldering Temperature (time)	Tsld		260 (10 s)	
Storage Temperature	Tstg		– 55 to 125	¹ ∘c
Operating Temperature	Topr		- 40 to 85	

Note: The absolute maximum ratings are rated values which must not be exceeded during operation, even for an instant.

Any one of the ratings must not be exceeded. If any absolute maximum rating is exceeded, a device may break down or its performance may be degraded, causing it to catch fire or explode resulting in injury to the user. Thus, when designing products which include this device, ensure that no absolute maximum rating value will ever be exceeded.

Recommended Operating Condition

 $(V_{SS} = 0 \text{ V, Topr} = -40 \text{ to } 85^{\circ}\text{C})$ 

Parameter	Symbol	Pins	c	Condition		Max	Unit	
Supply Voltage			fc = 1 to 16 MHz	Each operation modes	4.5	5.5		
	V <sub>DD</sub>		fc = 1 to 8 MHz	Each operation modes	2.7	5.5		
			fs = 32.768 kHz	Each operation modes	2.7	5.5		
			ST	STOP mode		5.5	] ,	
	V <sub>IH1</sub>	Hysteresis	$V_{DD} \ge 4.5 V$		$V_{DD} \times 0.70$			Ţ
Input high Level	V <sub>IH2</sub>	Hysteresis			V <sub>DD</sub> × 0.75	$V_{DD}$		
	V <sub>IH3</sub>		V <sub>C</sub>	V <sub>DD</sub> < 4.5 V				
	V <sub>IL1</sub>	Hysteresis	V > 4.5.V			$V_{DD} \times 0.30$	]	
Input low Level	V <sub>IL2</sub>	Hysteresis		$V_{DD} \ge 4.5 V$		$V_{DD} \times 0.25$	1	
	V <sub>IL3</sub>		V <sub>C</sub>	<sub>DD</sub> < 4.5 V		V <sub>DD</sub> × 0.10	]	
	f.	VIN VOUT	V <sub>DD</sub> :	= 4.5 to 5.5 V	1.0	16.0	MHz	
Clock Frequency	fc	XIN, XOUT	$V_{DD} = 2.7 \text{ to } 5.5 \text{ V}$		1.0	8.0	1 101112	
	fs	XTEN, XTOUT			30.0	34.0	kHz	

Note: The recommended operating conditions for a device are operating conditions under which it can be guaranteed that the device will operate as specified. If the device is used under operating conditions other than the recommended operating conditions (supply voltage, operating temperature range, specified AC/DC values etc.), malfunction may occur. Thus, when designing products which include this device, ensure that the recommended operating conditions for the device are always adhered to.

DC Characteristics  $(V_{SS} = 0 \text{ V}, \text{Topr} = -40 \text{ to } 85^{\circ}\text{C})$ 

Parameter	Symbol	Pins	Condition	Min	Тур.	Max	Unit	
Hysteresis Voltage	V <sub>HS</sub>	Hysteresis input		_	0.9	_	V	
	I <sub>IN1</sub>	TEST						
Input Current	I <sub>IN2</sub>	Sink Open Drain, Tri-state port	$V_{DD} = 5.5 \text{ V}, V_{IN} = 5.5 \text{ V/0 V}$	-	_	± 2	μΑ	
	I <sub>IN3</sub>	STOP, RESET						
	R <sub>IN1</sub>	TEST		_	70	-		
Input Resistance	R <sub>IN2</sub>	RESET		100	220	450	$\left[\begin{array}{c} \mathbf{k}_{\Omega} \end{array}\right]$	
mput Nesistance	R <sub>IN3</sub>	Programmable pull up (P6, P7, PA, PB)	V <sub>DD</sub> = 5.5 V	40	80	200		
OSC. Feedback	Rfx	XIN-XOUT		_	1.2	_		
resistance	Rfxt	XTIN-XTOUT		_	6	MΩ		
Output Leakage	I <sub>LO1</sub>	Sink Open Drain port	V <sub>DD</sub> = 5.5 V, V <sub>OUT</sub> = 5.5 V	_	-	2		
Current	I <sub>LO2</sub>	Tri-state port	V <sub>DD</sub> = 5.5 V, V <sub>OUT</sub> = 5.5 V/0 V	_	-	± 2	μΑ	
"H" output Voltage	V <sub>OH</sub>	Tri-state port	$V_{DD} = 4.5 \text{ V}, I_{OH} = -0.7 \text{ mA}$	4.1	_	_		
"L" output Voltage	V <sub>OL3</sub>	P5, P9	$V_{DD} = 4.5 \text{ V}, I_{OL} = 1.6 \text{ mA}$	_	-	0.4	\ \	
W. W	I <sub>OL1</sub>	Except P5, P9	V <sub>DD</sub> = 4.5 V, V <sub>OL</sub> = 0.4 V	_	1.6	_		
"L" output Current	I <sub>OL3</sub>	High current port (P5, P9)	V <sub>DD</sub> = 4.5 V, V <sub>OL</sub> = 1.0 V	_	20	_		
Supply Current in			V <sub>DD</sub> = 5.5 V		7	8		
Normal 1, 2 mode			V <sub>IN</sub> = 5.3 V/0.2 V	_		٥	mA	
Supply Current in			fc = 16 MHz		4	5		
IDLE 1, 2 mode			fs = 32.768 kHz					
Supply Current in	I <sub>DD</sub>		V <sub>DD</sub> = 3.0 V	_	10	20		
SLOW 1 mode			$V_{IN} = 2.8 \text{ V}/0.2 \text{ V}$					
Supply Current in			fs = 32.768 kHz	_	6	12	μA	
SLEEP 0, 1 mode						. <u>-</u>		
Supply Current in STOP mode			$V_{DD} = 5.5 \text{ V}$ $V_{IN} = 5.3 \text{ V}/0.2 \text{ V}$	-	0.5	10		

Note 1: Typical values show those at Topr =  $25^{\circ}$ C,  $V_{DD} = 5 \text{ V}$ 

Note 2: Input current ( $I_{IN1}$ ,  $I_{IN3}$ ); The current through pull-up or pull-down resistor is not included.

Note 3: IDD does not include IREF current.

**AD Conversion Characteristics** 

(V<sub>SS</sub> = 0 V, 4.5 V  $\leq$  V<sub>DD</sub>  $\leq$  5.5 V, Topr = -40 to 85°C)

Parameter	Symbol	Condition	Min	Тур.	Max	Unit
Analog Reference Voltage	V <sub>AREF</sub>		A <sub>VDD</sub> – 1.0	_	A <sub>VDD</sub>	
Power Supply Voltage of	A <sub>VDD</sub>			$V_{DD}$		
Analog Control Circuit	A <sub>VSS</sub>			$V_{SS}$		] ,,
Analog Reference of Voltage Range	$\triangle V_{AREF}$		3.5	-	V <sub>DD</sub>	V
Analog Input Voltage	V <sub>AIN</sub>		V <sub>SS</sub>	_	V <sub>AREF</sub>	
Power Supply Current of Analog Reference Voltage	I <sub>REF</sub>	$V_{DD} = A_{VDD} = V_{AREF} = 5.5 \text{ V}$ $V_{SS} = A_{VSS} = 0.0 \text{ V}$	-	0.6	1.0	mA
Non linearity Error			-	-	± 2	
Zero Point Error		$V_{DD} = A_{VDD} = 5.0 \text{ V}$	_	-	± 2	]
Full Scale Error		$V_{SS} = A_{VSS} = 0.0 \text{ V}$ $V_{AREF} = 5.0 \text{ V}$	-	_	± 2	LSB
Total Error		7.1	_	ı	± 4	<u> </u>

$$(V_{SS} = 0 \text{ V}, 2.7 \text{ V} \le V_{DD} < 4.5 \text{ V}, Topr = -40 \text{ to } 85^{\circ}\text{C})$$

Parameter	Symbol	Condition	Min	Тур.	Max	Unit
Analog Reference Voltage	V <sub>AREF</sub>		A <sub>VDD</sub> – 1.0	_	A <sub>VDD</sub>	
Power Supply Voltage of	A <sub>VDD</sub>			$V_{DD}$		]
Analog Control Circuit	A <sub>VSS</sub>			V <sub>SS</sub>		] ,
Analog Reference of Voltage Range	$\triangle V_{AREF}$		2.5	-	V <sub>DD</sub>	\ \ \
Analog Input Voltage	V <sub>AIN</sub>		V <sub>SS</sub>	_	V <sub>AREF</sub>	]
Power Supply Current of Analog Reference Voltage	I <sub>REF</sub>	$V_{DD} = A_{VDD} = V_{AREF} = 4.5 \text{ V}$ $V_{SS} = A_{VSS} = 0.0 \text{ V}$	-	0.5	0.8	mA
Non linearity Error			_	_	± 2	
Zero Point Error		$V_{DD} = A_{VDD} = 2.7 \text{ V}$	_	_	± 2	]
Full Scale Error		$V_{SS} = A_{VSS} = 0.0 \text{ V}$ $V_{ARFF} = 2.7 \text{ V}$	_	_	± 2	LSB
Total Error		73361	_	_	± 4	1

- Note 1: Total error includes all error except a quantization error, and is defined as a maximum deviation from the ideal conversion line.
- Note 2: Conversion time is different in recommended value by power supply voltage.

  About conversion time, please refer to "2.14.2 Register Framing".
- Note 3: Please use input voltage to AIN input Pin in limit of V<sub>AREF</sub>- V<sub>SS</sub>.

  When voltage of range outside is input, conversion value becomes unsettled and gives affect to other channel conversion value.
- Note 4: Analog Reference Voltage Range:  $\triangle V_{AREF} = V_{AREF} A_{VSS}$

**AC Characteristics** 

 $(V_{SS} = 0 \text{ V}, V_{DD} = 4.5 \text{ to } 5.5 \text{ V}, Topr = -40 \text{ to } 85^{\circ}\text{C})$ 

Parameter	Symbol	Condition	Min	Тур.	Max	Unit
		NORMAL 1, 2 mode	0.25	_	4	
Machine Cycle Time		IDLE 0, 1, 2 mode	0.25			
	tcy	SLOW 1, 2 mode SLEEP 0, 1, 2 mode		_	133.3	μS
High Level Clock Pulse Width	t <sub>WCH</sub>	For external clock operation (XIN input)		24.25		
Low Level Clock Pulse Width	t <sub>WCL</sub>	fc = 16 MHz	_	31.25	_	ns
High Level Clock Pulse Width	t <sub>WSH</sub>	For external clock operation (XTIN input)		45.26		
Low Level Clock Pulse Width	t <sub>WSL</sub>	fs = 32.768 kHz	_	15.26	-	μS

# (V<sub>SS</sub> = 0 V, V<sub>DD</sub> = 2.7 to 4.5 V , Topr = -40 to 85°C)

Parameter	Symbol	Condition	Min	Тур.	Max	Unit
		NORMAL 1, 2 mode			4	
Machine Cycle Time		IDLE 0, 1, 2 mode	0.5	_		
	tcy	SLOW 1, 2 mode	117.6		100.0	$\mu$ S
		SLEEP 0, 1, 2 mode		-	133.3	
High Level Clock Pulse Width	t <sub>WCH</sub>	For external clock operation (XIN input)		60.5		
Low Level Clock Pulse Width	t <sub>WCL</sub>	fc = 8 MHz		62.5	_	ns
High Level Clock Pulse Width	t <sub>WSH</sub>	For external clock operation (XTIN input)				
Low Level Clock Pulse Width	t <sub>WSL</sub>	fs = 32.768 kHz	-	15.26	-	μS

## **Recommended Oscillating Conditions-1**

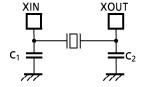
 $(V_{SS} = 0 \text{ V}, V_{DD} = 4.5 \text{ to } 5.5 \text{ V}, \text{ Topr} = -40 \text{ to } 85^{\circ}\text{C})$ 

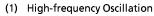
Davamatar	0 311 4	Oscillation			Recommended Constant		
Parameter Oscillato	Oscillator	Frequency	Recom	mended Oscillator	C <sub>1</sub>	C <sub>2</sub>	
	16 MHz	MURATA	CSA16.00MXZ040	10 pF	10 pF		
⊔iah fraguansy		8 MHz	MURATA	CSA8.00MTZ	30 pF	30 pF	
High-frequency Oscillation	Ceramic Resonator	8 IVITZ		CST8.00MTW	30 pF (built-in)	30 pF (built-in)	
Oscillation		4.40.0411	MURATA	CSA4.19MG	30 pF	30 pF	
		4.19 MHz		CST4.19MGW	30 pF (built-in)	30 pF (built-in)	
Low-frequency Oscillation	Crystal Oscillator	32.768 kHz	SII	VT-200	6 pF	6 pF	

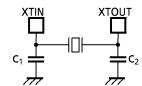
## **Recommended Oscillating Conditions-2**

$$(V_{SS} = 0 \text{ V}, V_{DD} = 2.7 \text{ to } 5.5 \text{ V}, Topr = -40 \text{ to } 85^{\circ}\text{C})$$

Parameter	Oscillator	Oscillation	Recommended Oscillator		Recommended Constant	
		Frequency			C <sub>1</sub>	C <sub>2</sub>
High-frequency Oscillation	Ceramic Resonator	8 MHz	MURATA	CSA8.00MTZ	30 pF	30 pF
				CST8.00MTW	30 pF (built-in)	30 pF (built-in)
		4.19 MHz	MURATA	CSA4.19MG	30 pF	30 pF
				CST4.19MGW	30 pF (built-in)	30 pF (built-in)







(2) Low-frequency Oscillation

- Note 1: An electrical shield by metal shield plate on the surface of IC package is recommended in order to protect the device from the high electric field stress applied from CRT (Cathodic Ray Tube) for continuous reliable operation.
- Note 2: The product numbers and specifications of the resonators by Murata Manufacturing Co., Ltd. are subject to change. For up-to-date information, please refer to the following URL; http://www.murata.co.jp/search/index.html