CMOS 4-Bit Microcontroller

TMP47C103N, TMP47C203N
TMP47C103M, TMP47C203M

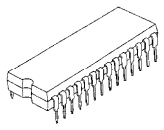
The TMP47C103/203 are high speed and high performance 4-bit single chip micro computers, integrating ROM, RAM, input/output ports and timer/counters on a ship.
The TMP47C103/203 are srandard LSI in the TLCS-47E series.
In addition, they have 8 bit SIO, watchdog timer and the output port with LED direct drive capabilty.

Part No.	ROM	RAM	Package	OTP Version
TMP47C103N	1024 × 8-bit	64 × 4-bit	P-SDIP28-400-1.78	TMP47P403VN
TMP47C103M			P-SOP28-450-1.27	TMP47P403VM
TMP47C203N	2048 × 8-bit	128 × 4-bit	P-SDIP28-400-1.78	TMP47P403VN
TMP47C203M			P-SOP28-450-1.27	TMP47P403VM

Features

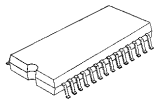
- ◆4-bit single chip microcomputer
- ◆Instruction execution time: 1.3 μs (at 6 MHz)
- ◆Low voltage operation: 2.2 V (at 2 MHz RC)
- ◆90 basic instructions
  - ROM table look-up instructions
  - 5-bit to 8-bit data conversion instruction
- ◆Subroutine nesting: 15 levels max
- ◆6 interrupt sources (External: 2, Internal: 4)
  All sources have independent latches each, and multiple interrupt control is available
- ◆I/O port (23 pins)
- ◆Two 12-bit Timer / Counters
  Timer, event counter, and pulse width measurement mode
- ◆Interval Timer
- ◆Watchdog Timer
- ◆Serial Interface with 8-bit buffer
  - Simultaneous transmission and reception capability
  - 4/8-bit transfer, external / internal clock, and leading/trailing edge shift mode

P-SDIP28-400-1.78



TMP47C103N
TMP47C203N
TMP47P403VN

P-SOP28-450-1.27



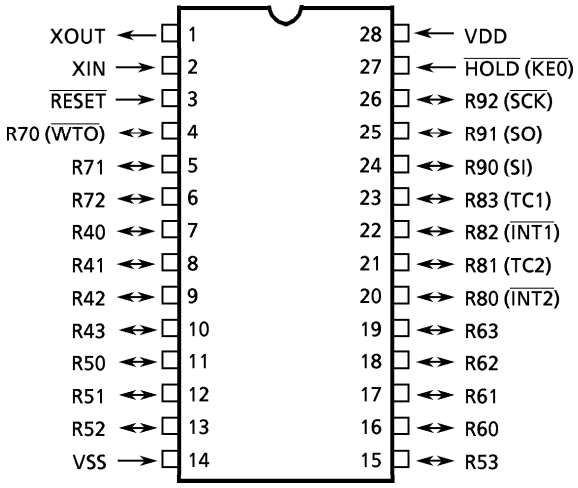
TMP47C103M
TMP47C203M
TMP47P403VM

000707EBA1

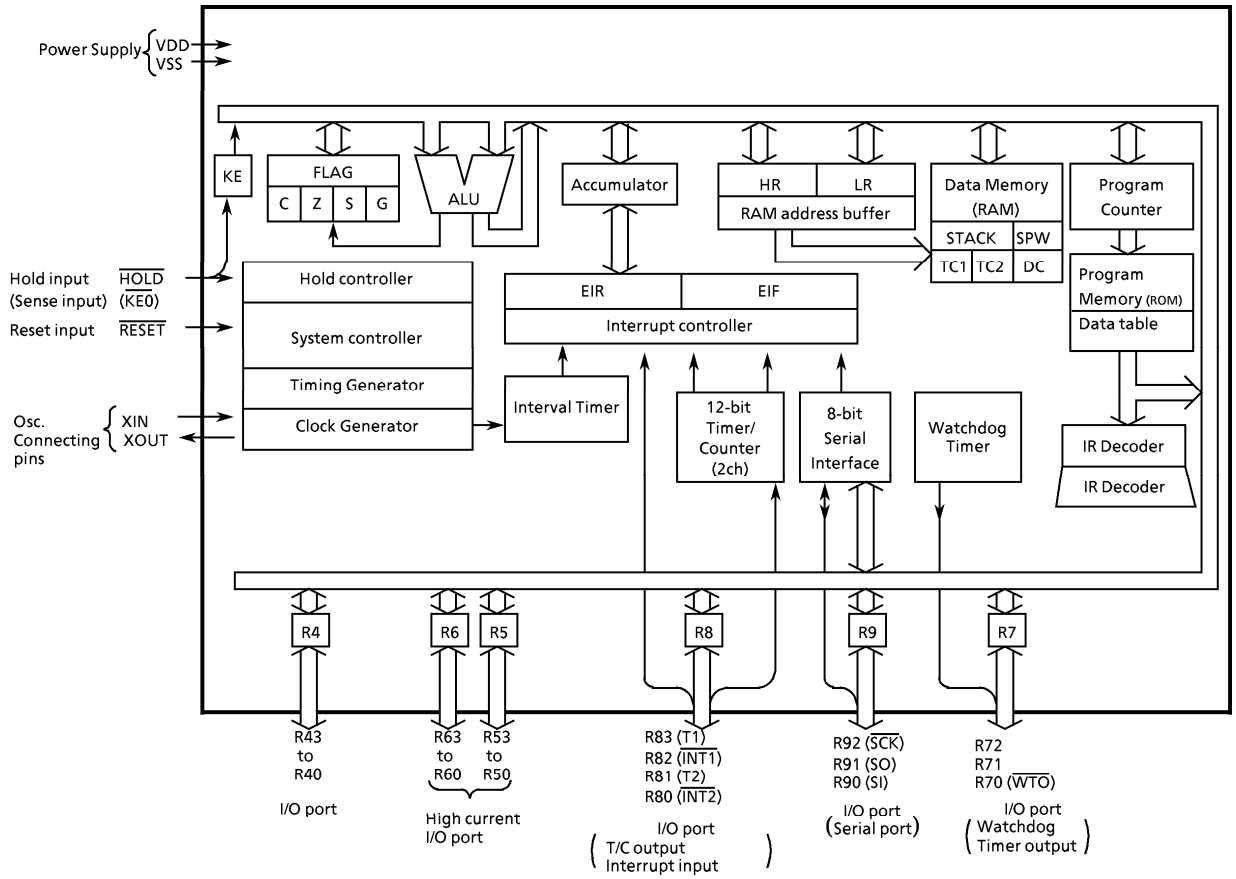
◆High current outputs
LED direct drive capability: typ. 20 mA × 8 bits (port R5, R6)
typ. 7 mA × 4 bits (port R4)
◆Hold function
Battery / Capacitor back-up
◆Real Time Emulator: BM47C203

Pin Assignment (Top View)

P-SDIP28-400-1.78 / P-SOP28-450-1.27



Block Diagram



Pin Function

Pin Name	Input / Output	Functions	
R43 to R40	I/O	4-bit I/O port with latch (R7 port has only 3-bit). When used as input port, the latch must be set to "1". Every bit data is possible to be set, cleared and tested by the bit manipulation instruction of the L-register indirect addressing.	
R53 to R50			8-bit data are output by the 5-bit to 8-bit data conversion instruction [OUTB @HL] .
R63 to R60			
R72 to R71	I/O		
R70 ($\overline{WTO}$)	I/O(Output)		Watchdog timer output
R83 (T1)	I/O(Input)	4-bit I/O port with latch. When used as input port, external interrupt input pin, or timer/counter external input pin, the latch must be set to "1".	Timer / C ounter 1 external input
R82 ($\overline{INT1}$)			External interrupt 1 input
R81 (T2)			Timer / Counter 2 external input
R80 ($\overline{INT2}$)			External interrupt 2 input
R92 ($\overline{SCK}$)	I/O(I/O)	3-bit I/O port with latch. When used as input port or serial port, the latch must be set to "1".	Serial clock I/O
R91 (SO)	I/O(Output)		Serial data output
R90 (SI)	I/O(Input)		Serial data input
XIN	Input	Resonator connecting pins.	
XOUT	Output	For inputting external clock, XIN is used and XOUT is opened.	
$\overline{RESET}$	Input	Reset signal input	
$\overline{HOLD}$ ($\overline{KE0}$)	Input(Input)	Hold request / release signal input	Sense input
VDD	Power Supply	+ 5 V	
VSS		0 V (GND)	

Operational Description

Concerning the TMP47C103/203 the configuration and functions of hardwares are described. The basic instruction of configuration in the TMP47C103/203 is the same those of TLCS-47 serise.

1. System Configuration

◆Internal CPU Function

- 2.1 Program Counter (PC)
- 2.2 Program Memory (ROM)
- 2.3 H Register, L Register
- 2.4 Data Memory (RAM)
  - a. Stack
  - b. Stack Pointer Word (SPW)
  - c. Data Counter (DC)
- 2.5 ALU, Accumulator
- 2.6 Flags
- 2.7 Clock Generator and Timing Generator
- 2.8 INTERRUPT FUNCTION
- 2.9 RESET FUNCTION

◆Peripheral Hardware Function

- 3.1 I/O Ports
- 3.2 Interval Timer
- 3.3 Timer / Counters (TC1, TC2)
- 3.4 Watchdog Timer
- 3.5 Serial Interface

2. Internal CPU Function

2.1 Program Counter (PC)

The program counter is a 11-bit binary counter which indicates the address of the program memory storing the next instruction to be executed. Normally, the PC is incremented by the number of bytes of the instruction every time it is fetched. When a branch instruction or a subroutine instruction has been executed or an interrupt has been accepted, the specified values listed in Table 2-1 are set to the PC. The PC is initialized to "0" during reset.

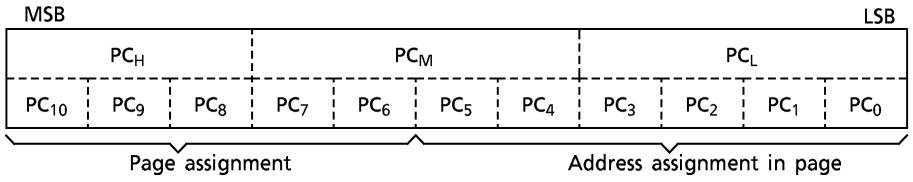


Figure 2-1. Configuration of Program Counter

The PC can directly address a 2048-byte address space. However, with the short branch and subroutine call instructions, the following points must be considered.

(1) Short branch instruction [BSS a]

In [BSS a] instruction execution, when the branch condition is satisfied, the value specified in the instruction is set to the lower 6 bits of the PC. That is, [BSS a] becomes the in-page branch instruction. When [BSS a] is stored at the last address of the page, the upper 6 bits of the PC point the next page, so that branch is made to the next page.

Table 2-1. Status Change of Program Counter

Instruction or Operation		Condition		Program Counter (PC)										
				PC_{10}	PC_9	PC_8	PC_7	PC_6	PC_5	PC_4	PC3	PC_2	PC_1	PC_0
Execution of Instruction	BS a	SF = 1 (Branch condition is satisfied)		Immediate data specified by the instruction										
		SF = 0 (Branch condition is not satisfied)		+ 2										
	BSS a	SF = 1	Lower 6-bit address ≠ 111111	Hold							Immediate data specified by the instruction			
			Lower 6-bit address = 111111 (last address in page)	+ 1							Immediate data specified by the instruction			
		SF = 0		+ 1										
	CALL a			Immediate data specified by the instruction										
	CALLS a			0	0	0	The data generated by the immediate data specified by the instruction					1	1	0
	RET			The return address restored from stack										
	RETI			The return address restored from stack										
	Others			Incremented by the number of bytes in the instruction										
Interrupt acceptance				0	0	0	0	0	0	0	Interrupt vector			0
Reset				0	0	0	0	0	0	0	0	0	0	0

2.2 Program Memory (ROM)

Programs and fixed data are stored in the program memory. The instruction to be executed next is read from the address indicated by the contents of the PC.

The fixed data can be need by using the table look-up instructions on 5-bit to 8-bit data conversion instruction.

(1) Table look-up instructions

[LDL A, @DC], [LDH A, @DC+]

The table look-up instructions read the lower and upper 4 bits of the fixed data stored at the address specified in the data counter (DC) to place them into the accumulator. [LDL A, @DC] instruction reads the lower 4 bits of fixed data, and [LDH A, @DC+] instruction reads the upper 4 bits.

The DC is a 12-bit register, allowing it to address the entire program memory space.

In this case, the upper bit of the DC (MSB) is ignared.

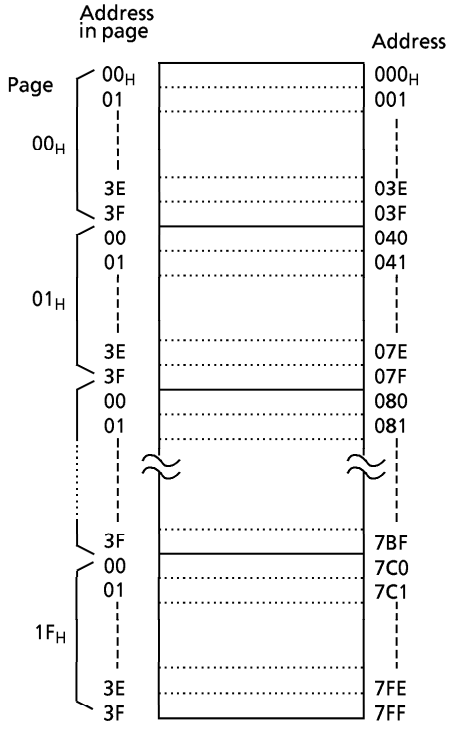


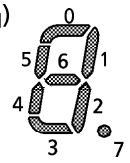
Figure 2-2. Configuration of Program Memory

(2) 5-bit to 8-bit data conversion instruction [OUTB @HL]

The 5-bit to 8-bit data conversion instruction reads the fixed data (8 bits) from the data conversion table in the program memory to output the upper 4 bits to port P6 and the lower 4 bits to port P5. The table is located in the last 32-byte space (addresses,$7E0_H$ through $7FF_H$ for the TMP47C203, $3E0_H$ through $3FF_H$ for the TMP47C103) in the program memory with the lower address consisting of the 5 bits obtained by concatenating the contents of the data memory specified by the HL register pair and the content of the carry flag. This instruction is usable for such applications as converting BCD data into an output code to the 7-segment display elements.

Example: The following shows that the BCD data at address $2F_H$ in the data memory is converted into the 7-segment code (e.g., anode common LED) to be output to ports P6 and P5.

```
LD      HL, #2FH ;  HL←2FH (Data memory address is set)
TEST    CF       ;  CF←0 (The table is specified at addresses 7E0H - 7EFH)
OUTB    @HL      ;  Ports P6, P5←fixed data
  :
ORG     07E0H    ;  Data conversion table
DATA    0C0H, 0F9H, 0A4H, 0B0H, 99H, 92H, 82H, 0D8H, 80H, 98H
```



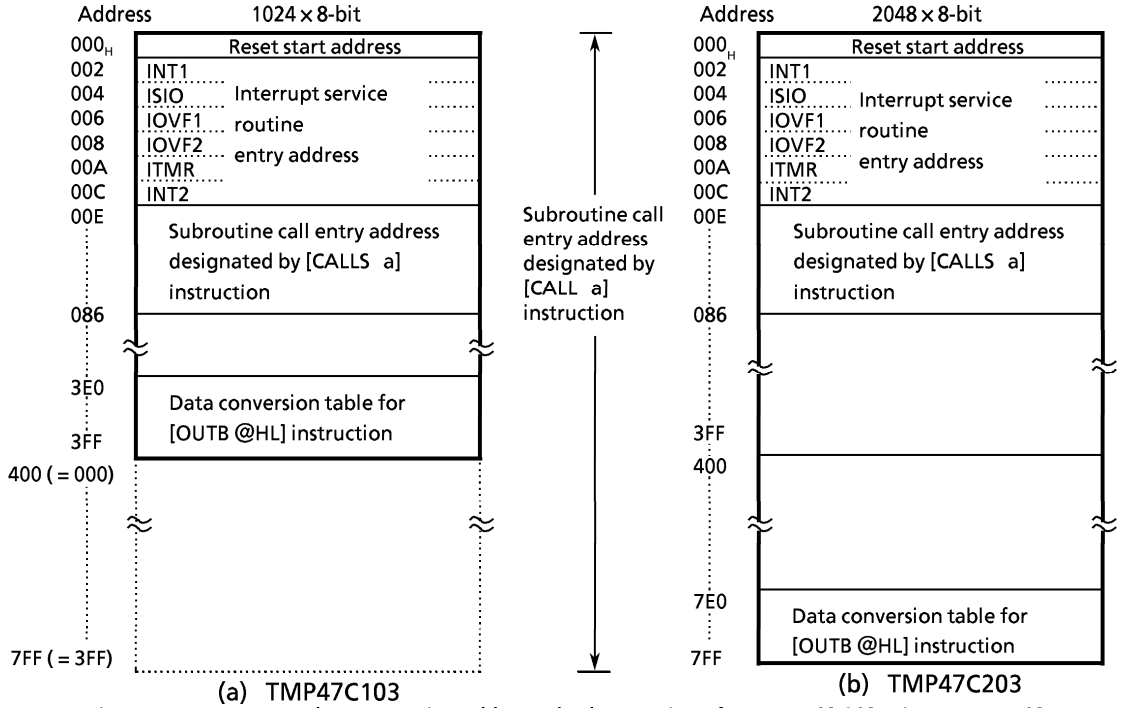
2.2.1 Program Memory Map

The TMP47C103 has 1024 × 8 bits (addresses 000_H through $3FF_H$) of program memory (mask ROM), the TMP47C203 has 2048 × 8 bits (addresses 000_H through $7FF_H$).

Figure 2-3 shows the program memory map. Address 000_H to 086_H and $7E0_H$ to $7FF_H$ ($3E0_H$ to $3FF_H$ for the TMP47C103) of the program memory are also used for special purposes.

2.2.2 Program Memory Capacity

On the TMP47C103, no physical program memory exists in the address range 400_H through $7FF_H$. However, if this space is accessed by program, the most significant bit of each address is always regarded as "0" and the contents of the program memory corresponding to the address 000_H through $3FF_H$ are read.



Note: It is necessary to set two data conversion tables to check operation of TMP47C103/203 using TMP47P403V.
For details, see the technical documents of TMP47P403V.

Figure 2-3. Program Memory Map

Electrical Characteristics

Absolute Maximum Ratings (V_{SS} = 0 V)

Parameter	Symbol	Pins		Ratings	Unit
Supply Voltage	V_{DD}			– 0.3 to 6.5	V
Input Voltage	V_{IN}			– 0.3 to V_{DD} + 0.3	V
Output Voltage	V_{OUT}			– 0.3 to V_{DD} + 0.3	V
Output Current (Per 1 pin)	I_{OUT1}	Port R5, R6		30	mA
	I_{OUT2}	Port R4		15	
	I_{OUT3}	Ports R7, R8, R9		3.2	
Output Current (Total)	ΣI_{OUT}	Port R4, R5, R6		120	mA
Power Dissipation [Topr = 70°C]	PD		DIP	300	mW
			SOP	180	
Soldering Temperature (time)	Tsld			260 (10 s)	°C
Storage Temperature	Tstg			– 55 to 125	°C
Operating Temperature	Topr			– 30 to 70	°C

Note: The absolute maximum ratings are rated values which must not be exceeded during operation, even for an instant. Any one of the ratings must not be exceeded. If any absolute maximum rating is exceeded, a device may break down or its performance may be degraded, causing it to catch fire or explode resulting in injury to the user. Thus, when designing products which include this device, ensure that no absolute maximum rating value will ever be exceeded.

Recommended Operating Conditions (V_{SS} = 0 V, Topr = – 30 to 70°C)

Parameter	Symbol	Pins		Conditions		Min	Max	Unit
Supply Voltage	V_{DD}		Normal mode	Crystar or ceramic	fc = 6.0 MHz	4.5	5.5	V
					fc = 4.2 MHz	2.7		
				RC	fc = 2.5 MHz	2.2		
			HOLD mode	–	–	2.0		
Input High Voltage	V_{IH1}	Except Hysteresis Input		In the normal operating area		V_{DD} × 0.7	V_{DD}	V
	V_{IH2}	Hysteresis Input				V_{DD} × 0.75		
	V_{IH3}			In the HOLD mode		V_{DD} × 0.9		
Input Low Voltage	V_{IL1}	Except Hysteresis Input		In the normal operating area		0	V_{DD} × 0.3	V
	V_{IL2}	Hysteresis Input					V_{DD} × 0.25	
	V_{IL3}			In the HOLD mode			V_{DD} × 0.1	
Clock Frequency	fc	XIN, XOUT		V_{DD} = 4.5 to 5.5 V		0.4	6.0	MHz
				V_{DD} = 2.7 to 5.5 V			4.2	
				V_{DD} = 2.2 to 5.5 V (RC)			2.5	

Note: The recommended operating conditions for a device are operating conditions under which it can be guaranteed that the device will operate as specified. If the device is used under operating conditions other than the recommended operating conditions (supply voltage, operating temperature range, specified AC/DC values etc.), malfunction may occur. Thus, when designing products which include this device, ensure that the recommended operating conditions for the device are always adhered to.

DC Characteristics

(V_{SS} = 0 V, Topr = – 30 to 70°C)

Parameter	Symbol	Pins	Conditions	Min	Typ.	Max	Unit
Hysteresis Voltage	V_{HS}	Hysteresis Input		–	0.7	–	V
Input Current	I_{IN1}	$\overline{RESET}$, $\overline{HOLD}$	V_{DD} = 5.5 V, V_{IN} = 5.5 V / 0 V	–	–	± 2	μA
	I_{IN2}	Open drain output ports					
Input Resistance	R_{IN}	$\overline{RESET}$		100	220	450	kΩ
Input Low Current	I_{IL}	Push-pull output ports	V_{DD} = 5.5 V, V_{IN} = 0.4 V	–	–	– 2	mA
Output Leakage Current	I_{LO}	Open drain output ports	V_{DD} = 5.5 V, V_{OUT} = 5.5 V	–	–	2	μA
Output High Voltage	V_{OH}	Push-pull output ports	V_{DD} = 4.5 V, I_{OH} = – 200 μA	2.4	–	–	V
			V_{DD} = 2.2 V, I_{OH} = – 5 μA	2.0	–	–	
Output Low Voltage	V_{OL}	Port R7, R8, R9	V_{DD} = 4.5 V, I_{OL} = 1.6 mA	–	–	0.4	V
			V_{DD} = 2.2 V, I_{OL} = 20 mA	–	–	0.1	
Output Low Current	I_{OL1}	Port R5, R6	V_{DD} = 4.5 V, V_{OL} = 1.0 V	–	20	–	mA
	I_{OL2}	Port R4		–	7	–	
Supply Current (in the Normal operating mode)	I_{DD}		V_{DD} = 5.5 V, fc = 4 MHz	–	2	4	mA
			V_{DD} = 3.0 V, fc = 4 MHz	–	1	2	
			V_{DD} = 3.0 V, fc = 400 kHz	–	0.5	1	
Supply Current (in the HOLD operating mode)	I_{DDH}		V_{DD} = 5.5 V	–	0.5	10	μA

Note 1: Typ. values show those at T_{opr} = 25°C, V_{DD} = 5 V.

Note 2: Input Current I_{IN1}: The current through resistor is not included.

Note 3: Supply Current: V_{IN} = 5.3 V / 0.2 V (V_{DD} = 5.5 V), 2.8 V / 0.2 V (V_{DD} = 3.0 V)

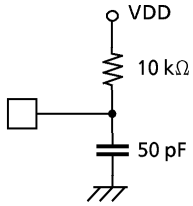
AC Characteristics

(V_{SS} = 0 V, Topr = – 30 to 70°C)

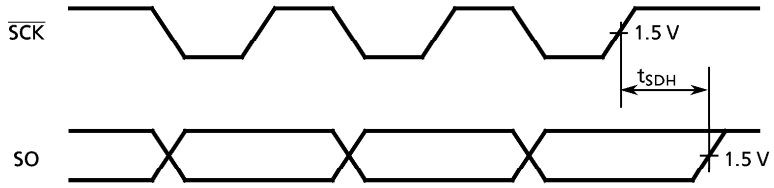
Parameter	Symbol	Conditions		Min	Typ.	Max	Unit
Instruction Cycle Time	tcy		V_{DD} = 4.5 to 5.5 V	1.3	–	20	μs
			V_{DD} = 2.7 to 5.5 V	1.9			
			V_{DD} = 2.2 to 5.5 V	3.2			
High level Clock pulse Width	t_{WCH}	For external clock operation	$V_{DD} \geqq 2.7$ V	80	–	–	ns
			$V_{DD} < 2.7$ V	160			
Low level Clock pulse Width	t_{WCL}		$V_{DD} \geqq 2.7$ V	80			
			$V_{DD} < 2.7$ V	160			
Shift data Hold Time	t_{SDH}			0.5 t_{cy} – 0.3	–	–	μs

Note: Shift data Hold Time:

External circuit for pins $\overline{SCK}$ and SO



Serial port (completed of transmission)



Recommended Oscillating Conditions

(V_{SS} = 0 V, V_{DD} = 4.5 to 5.5 V, Topr = – 30 to 70°C)

(1) 6 MHz

Ceramic Resonator

CSA6.00MGU (MURATA) $C_{XIN} = C_{XOUT}$ = 30 pF

KBR-6.00MS (KYOCERA) $C_{XIN} = C_{XOUT}$ = 30 pF

(2) 4 MHz

Ceramic Resonator

CSA4.00MG (MURATA) $C_{XIN} = C_{XOUT}$ = 30 pF

KBR-4.00MS (KYOCERA) $C_{XIN} = C_{XOUT}$ = 30 pF

Crystal Oscillator

204B-6F 4.0000 (TOYOCOM) $C_{XIN} = C_{XOUT}$ = 20 pF

(3) 400 kHz

Ceramic Resonator

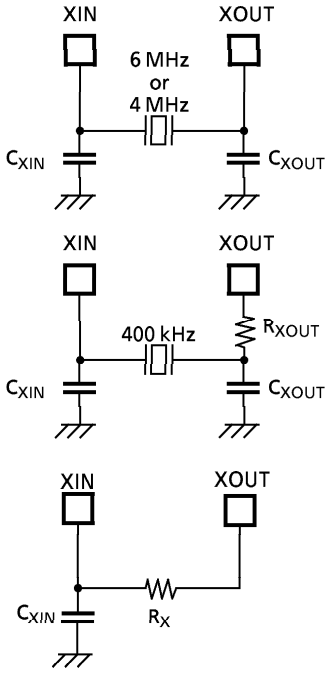
CSB400B (MURATA) $C_{XIN} = C_{XOUT}$ = 220 pF, R_{XOUT} = 6.8 kΩ

KBR-400B (KYOCERA) $C_{XIN} = C_{XOUT}$ = 100 pF, R_{XOUT} = 10 kΩ

(4) RC Oscillation (VSS = 0 V, VDD = 5.0 V, T_{opr} = 25°C)

2 MHz (Typ.) C_{XIN} = 33 pF, R_X = 10 kΩ

400 kHz (Typ.) C_{XIN} = 100 pF, R_X = 28 kΩ



Typical Characteristics