

4.5-ns Rail-to-Rail, High-Speed Comparator in Microsize Packages

Check for Samples: [TLV3501-Q1](#)

FEATURES

- Qualified for Automotive Applications
- High Speed: 4.5 ns
- Rail-To-Rail I/O
- Supply Voltage: +2.7 V to +5.5 V
- Push-Pull CMOS Output Stage
- Shutdown (TLV3501 Only)
- Micro Package:
SOT23-6
- Low Supply Current: 3.2 mA

APPLICATIONS

- Automatic Test Equipment
- Wireless Base Stations
- Threshold Detector
- Zero-Crossing Detector
- Window Comparator

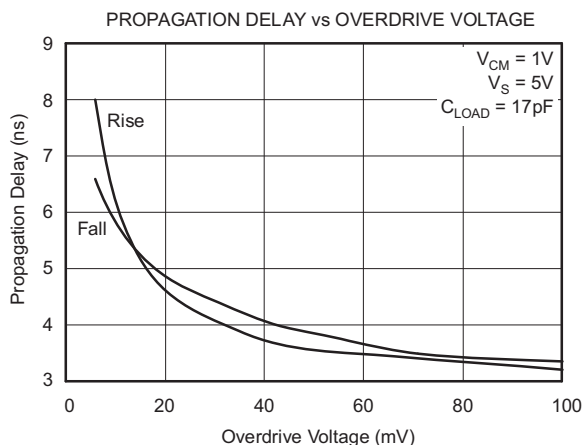
DESCRIPTION

The TLV3501 family of push-pull output comparators feature a fast 4.5-ns propagation delay and operation from +2.7 V to +5.5 V. Beyond-the-rails input common-mode range makes it an ideal choice for low-voltage applications. The rail-to-rail output directly drives either CMOS or TTL logic.

Microsize packages provide options for portable and space-restricted applications. The TLV3501-Q1 is available in a SOT23-6 package.

TLV3501-Q1 RELATED PRODUCTS

FEATURES	PRODUCT
Precision, Ultra-Fast, Low-Power Comparator	TLC3016
Differential Output Comparator	TL712
High-Speed Op Amp, 16-Bit Accurate, 150 MHz	OPA300
High-Speed Op Amp, Rail-to-Rail, 38 MHz	OPA350
High-Speed Op Amp with Shutdown, 250 MHz	OPA357



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION⁽¹⁾

PRODUCT	PACKAGE-LEAD	PACKAGE DESIGNATOR ⁽²⁾	PACKAGE MARKING
TLV3501AQDBVRQ1	SOT23-6	DBV	VCBQ

- (1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the device product folder at www.ti.com.
 (2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

Over operating free-air temperature range (unless otherwise noted).

	TLV3501-Q1	UNIT
Supply voltage	5.5	V
Signal input terminal voltage ⁽²⁾	(V-) - 0.3 to (V+) + 0.3	V
Signal input terminal current ⁽²⁾	10	mA
Output short-circuit current ⁽³⁾	74	mA
Thermal impedance, junction to free air	200	°C/W
Operating temperature	-40 to +125	°C
Storage temperature	-65 to +150	°C
Junction temperature	150	°C

- (1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not supported.
 (2) Input terminals are diode-clamped to the power-supply rails. Input signals that can swing more than 0.3V beyond the supply rails should be current limited to 10mA or less.
 (3) Short circuit to ground, one comparator per package

ELECTRICAL CHARACTERISTICS

$T_A = +25^\circ\text{C}$ and $V_S = +2.7\text{ V}$ to $+5.5\text{ V}$ (unless otherwise noted).

Boldface limits apply over the specified temperature range, $T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$.

PARAMETER	CONDITIONS	TLV3501-Q1			UNIT	
		MIN	TYP	MAX		
OFFSET VOLTAGE						
Input offset voltage ⁽¹⁾	V_{OS}	$V_{CM} = 0\text{ V}, I_O = 0\text{ mA}$		± 1	± 6.5	mV
vs Temperature	dV_{OS}/dT	$T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$		± 5		$\mu\text{V}/^\circ\text{C}$
vs Power supply	PSRR	$V_S = 2.7\text{ V}$ to 5.5 V		100	400	$\mu\text{V}/\text{V}$
Input hysteresis				6		mV
INPUT BIAS CURRENT						
Input bias current ⁽²⁾	I_B	$V_{CM} = V_{CC}/2, \Delta V_{IN} = \pm 5.5\text{ V}$		± 2	± 10	pA
Input offset current ⁽²⁾⁽³⁾	I_{OS}	$V_{CM} = V_{CC}/2, \Delta V_{IN} = \pm 5.5\text{ V}$		± 2	± 10	pA
INPUT VOLTAGE RANGE						
Common-mode voltage range	V_{CM}		$(V_-) - 0.2\text{ V}$		$(V_+) + 0.2\text{ V}$	V
Common-mode rejection	CMRR	$V_{CM} = -0.2\text{ V}$ to $(V_+) + 0.2\text{ V}$	57	70		dB
		$V_{CM} = -0.2\text{ V}$ to $(V_+) + 0.2\text{ V}$	55			dB
INPUT IMPEDANCE						
Common-mode				$10^{13} \parallel 2$		$\Omega \parallel \text{pF}$
Differential				$10^{13} \parallel 4$		$\Omega \parallel \text{pF}$
SWITCHING CHARACTERISTICS						
Propagation delay time ⁽²⁾⁽⁴⁾	T_{pd}	$\Delta V_{IN} = 100\text{ mV}$, Overdrive = 20 mV		4.5	6.4	ns
		$\Delta V_{IN} = 100\text{ mV}$, Overdrive = 20 mV			7	ns
		$\Delta V_{IN} = 100\text{ mV}$, Overdrive = 5 mV		7.5	10	ns
		$\Delta V_{IN} = 100\text{ mV}$, Overdrive = 20 mV			12	ns
Propagation delay skew ⁽⁵⁾	$\Delta t_{(SKEW)}$	$\Delta V_{IN} = 100\text{ mV}$, Overdrive = 20 mV		0.5		ns
Maximum toggle frequency	f_{MAX}	Overdrive = 50 mV, $V_S = 5\text{ V}$		80		MHz
Rise time ⁽⁶⁾	t_R			1.5		ns
Fall time ⁽⁶⁾	t_F			1.5		ns
OUTPUT						
Voltage output swing from rail	V_{OH}, V_{OL}	$I_{OUT} = \pm 1\text{ mA}$		30	50	mV
SHUTDOWN						
t_{OFF}				30		ns
t_{ON}				100		ns
V_H (comparator is enabled) ⁽⁷⁾					$(V_+) - 1.7\text{ V}$	V
V_L (comparator is disabled) ⁽⁷⁾			$(V_+) - 0.9\text{ V}$			V
Input bias current of Shutdown pin				2		pA
I_{QSD} (quiescent current in shutdown)				2		μA

(1) V_{OS} is defined as the average of the positive and the negative switching thresholds.

(2) Not production tested.

(3) The difference between I_{B+} and I_{B-} .

(4) Propagation delay cannot be accurately measured with low overdrive on automatic test equipment. This parameter is ensured by characterization at 100-mV overdrive.

(5) The difference between the propagation delay going high and the propagation delay going low.

(6) Measured between 10% of V_S and 90% of V_S .

(7) When the shutdown pin is within 0.9 V of the most positive supply, the part is disabled. When it is more than 1.7 V below the most positive supply, the part is enabled.

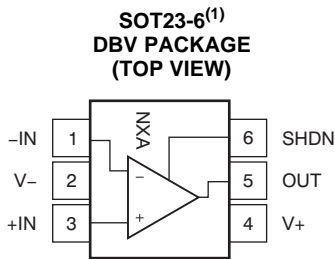
ELECTRICAL CHARACTERISTICS (continued)

$T_A = +25^\circ\text{C}$ and $V_S = +2.7\text{ V}$ to $+5.5\text{ V}$ (unless otherwise noted).

Boldface limits apply over the specified temperature range, $T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$.

PARAMETER	CONDITIONS	TLV3501-Q1			UNIT
		MIN	TYP	MAX	
POWER SUPPLY					
Specified voltage	V_S	+2.7		+5.5	V
Operating voltage range			2.2 to 5.5		V
Quiescent current	I_Q $V_S = 5\text{ V}, V_O = \text{High}$		3.2	5	mA
TEMPERATURE RANGE					
Specified range		-40		+125	$^\circ\text{C}$
Operating range		-40		+125	$^\circ\text{C}$
Storage range		-65		+150	$^\circ\text{C}$
Thermal resistance	θ_{JA}				
SOT23-6			200		$^\circ\text{C}/\text{W}$

PIN CONFIGURATIONS



(1) Pin 1 is determined by orienting the package marking as indicated on the diagram.

TYPICAL CHARACTERISTICS

At $T_A = +25^\circ\text{C}$, $V_S = 5\text{ V}$, and Input Overdrive = 100 mV (unless otherwise noted).

OUTPUT RESPONSE FOR VARIOUS OVERDRIVE VOLTAGES (Rising)

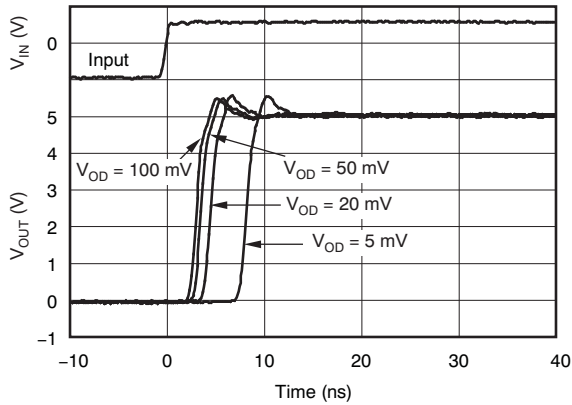


Figure 1.

OUTPUT RESPONSE FOR VARIOUS OVERDRIVE VOLTAGES (Falling)

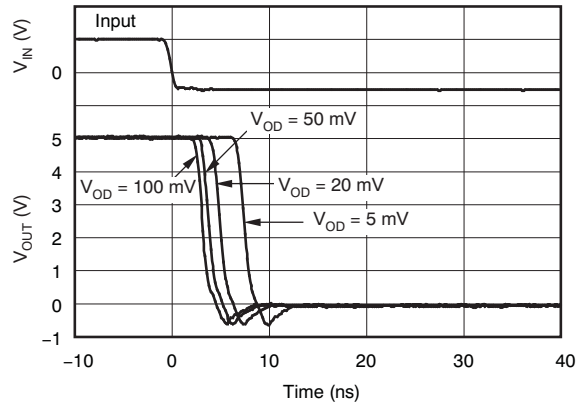


Figure 2.

PROPAGATION DELAY vs TEMPERATURE ($V_{OD} = 20\text{ mV}$)

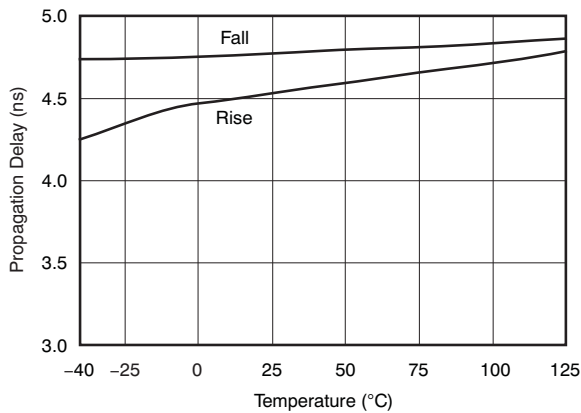


Figure 3.

PROPAGATION DELAY vs TEMPERATURE ($V_{OD} = 50\text{ mV}$)

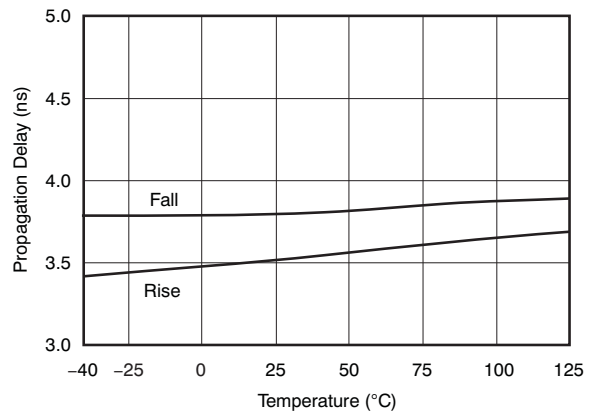


Figure 4.

PROPAGATION DELAY vs CAPACITIVE LOAD ($V_{OD} = 20\text{ mV}$)

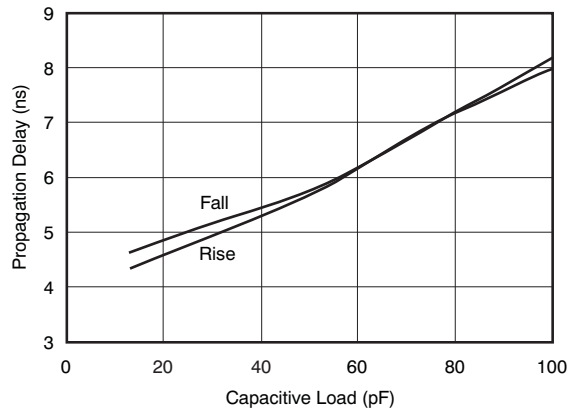


Figure 5.

PROPAGATION DELAY vs CAPACITIVE LOAD ($V_{OD} = 50\text{ mV}$)

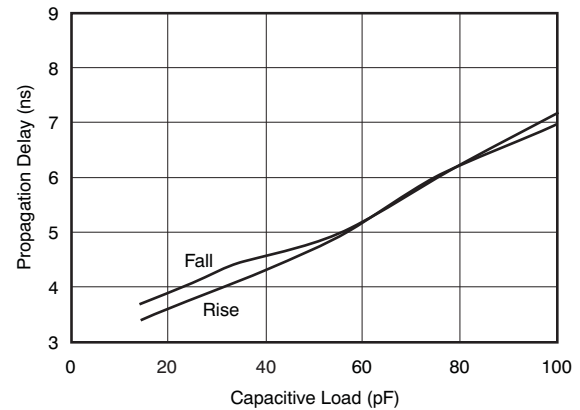


Figure 6.

TYPICAL CHARACTERISTICS (continued)

At $T_A = +25^\circ\text{C}$, $V_S = 5\text{ V}$, and Input Overdrive = 100 mV (unless otherwise noted).

PROPAGATION DELAY vs SUPPLY VOLTAGE
($V_{CM} = 1\text{ V}$, $V_{OD} = 20\text{ mV}$)

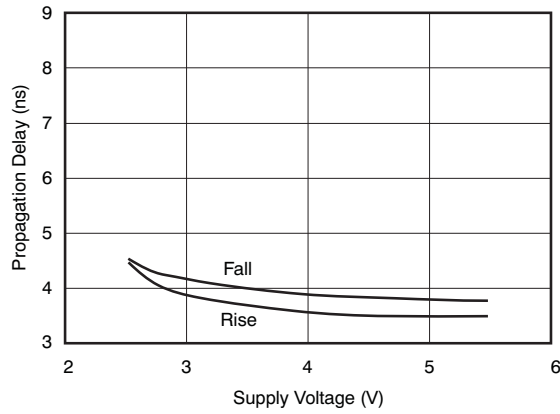


Figure 7.

WAKE-UP DELAY vs TEMPERATURE

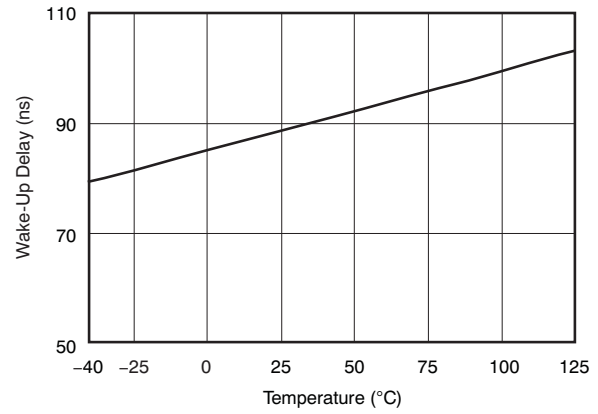


Figure 8.

RESPONSE TO 50-MHz SINE WAVE
($V_{DD} = 5\text{ V}$, $V_{IN} = 20\text{ mV}_{PP}$)

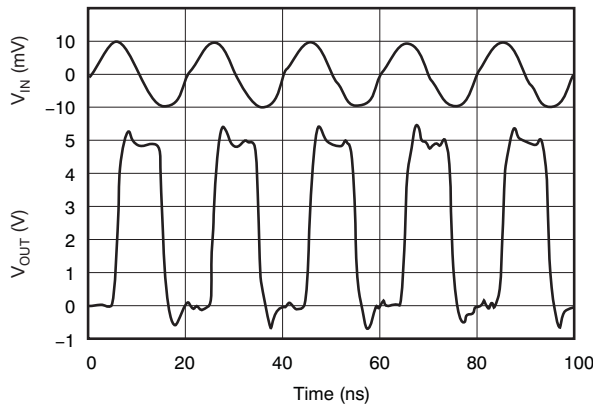


Figure 9.

RESPONSE TO 100-MHz SINE WAVE
($\pm 2.5\text{-V}$ Dual Supply into 50- Ω Oscilloscope Input)

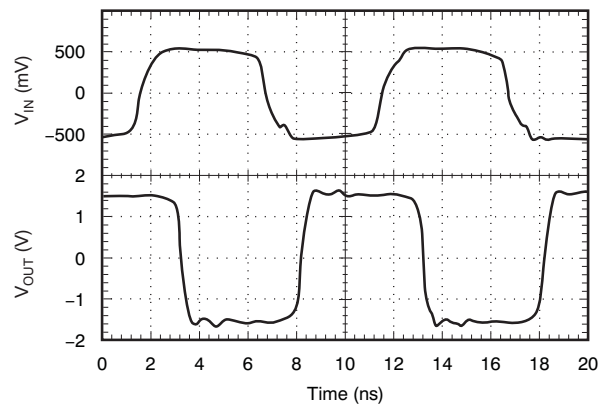


Figure 10.

QUIESCENT CURRENT vs SUPPLY VOLTAGE

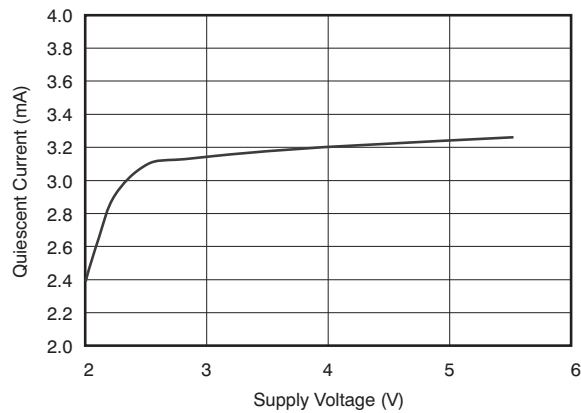


Figure 11.

QUIESCENT CURRENT vs TEMPERATURE

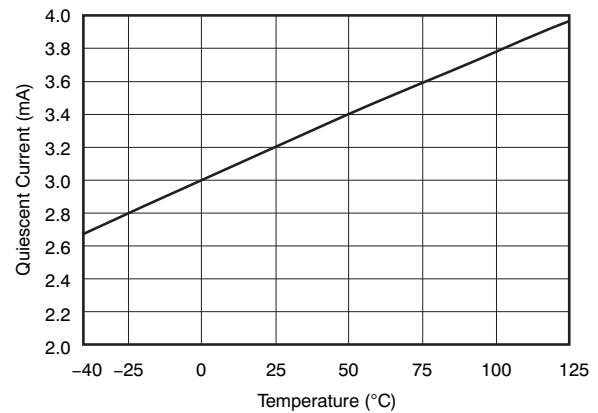


Figure 12.

TYPICAL CHARACTERISTICS (continued)

At $T_A = +25^\circ\text{C}$, $V_S = 5\text{ V}$, and Input Overdrive = 100 mV (unless otherwise noted).

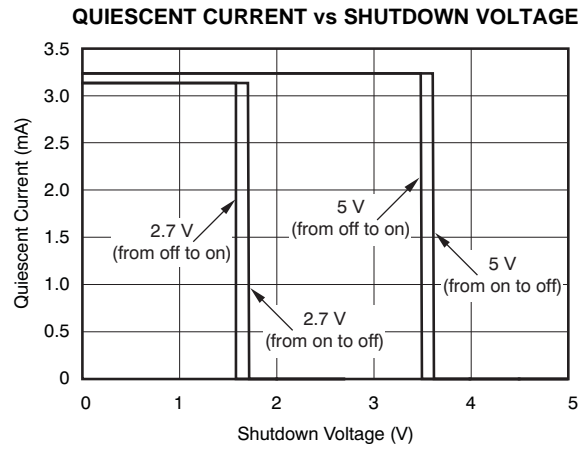


Figure 13.

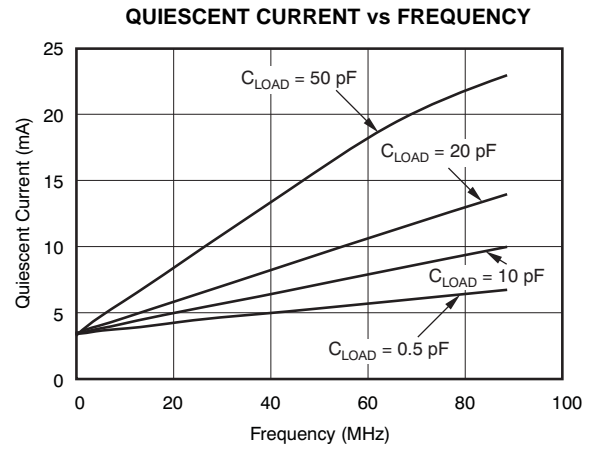


Figure 14.

APPLICATION INFORMATION

The TLV3501-Q1 features high-speed response and includes 6 mV of internal hysteresis for improved noise immunity with an input common-mode range that extends 0.2 V beyond the power-supply rails.

Shutdown

A shutdown pin allows the device to go into idle when it is not in use. When the shutdown pin is high, the device draws about 2 μA and the output goes to high impedance. When the shutdown pin is low, the TLV3501-Q1 is active. When the TLV3501-Q1 shutdown feature is not used, connect the shutdown pin to the most negative supply, as shown in [Figure 15](#). It takes about 100 ns to come out of shutdown mode.

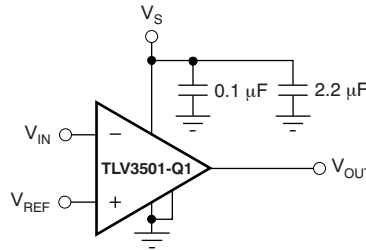


Figure 15. Basic Connections for the TLV3501-Q1

Operating Voltage

TLV3501-Q1 comparators are specified for use on a single supply from +2.7 V to +5.5 V (or a dual supply from ± 1.35 V to ± 2.75 V) over a temperature range of -40°C to $+125^\circ\text{C}$. The device continues to function below this range, but performance is not specified.

Adding External Hysteresis

The TLV3501-Q1 has a robust performance when used with a good layout. However, comparator inputs have little noise immunity within the range of specified offset voltage (± 5 mV). For slow moving or noisy input signals, the comparator output may display multiple switching as input signals move through the switching threshold. In such applications, the 6 mV of internal hysteresis of the TLV3501-Q1 might not be sufficient. In cases where greater noise immunity is desired, external hysteresis may be added by connecting a small amount of feedback to the positive. [Figure 16](#) shows a typical topology used to introduce 25 mV of additional hysteresis, for a total of 31-mV hysteresis when operating from a single 5-V supply. Total hysteresis is approximated by [Equation 1](#):

$$V_{\text{HYST}} = \frac{(V+) \times R_1}{R_1 + R_2} + 6\text{mV} \quad (1)$$

V_{HYST} sets the value of the transition voltage required to switch the comparator output by enlarging the threshold region, thereby reducing sensitivity to noise.

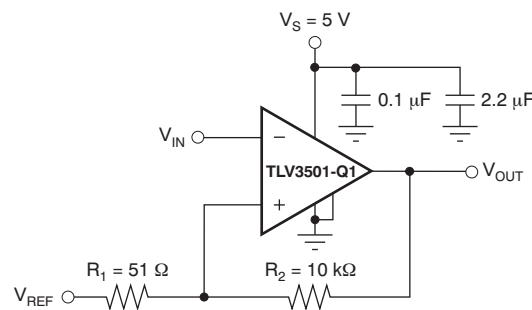


Figure 16. Adding Hysteresis to the TLV3501-Q1

Input Over-Voltage Protection

Device inputs are protected by electrostatic discharge (ESD) diodes that conduct if the input voltages exceed the power supplies by more than approximately 300 mV. Momentary voltages greater than 300 mV beyond the power supply can be tolerated if the input current is limited to 10 mA. This limiting is easily accomplished with a small input resistor in series with the comparator, as shown in Figure 17.

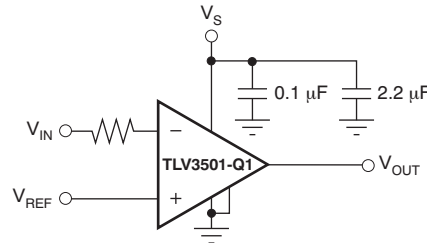


Figure 17. Input Current Protection for Voltages Exceeding the Supply Voltage

Relaxation Oscillator

The TLV3501-Q1 can easily be configured as a simple and inexpensive relaxation oscillator. In Figure 18, the R_2 network sets the trip threshold at $1/3$ and $2/3$ of the supply. Because this is a high-speed circuit, the resistor values are rather low to minimize the effect of parasitic capacitance. The positive input alternates between $1/3$ of V_+ and $2/3$ of V_+ depending on whether the output is low or high. The time to charge (or discharge) is $0.69R_1C$. Therefore, the period is $1.38R_1C$. For 62 pF and 1 kΩ as shown in Figure 18, the output is calculated to be 10.9 MHz. An implementation of this circuit oscillated at 9.6 MHz. Parasitic capacitance and component tolerances explain the difference between theory and actual performance.

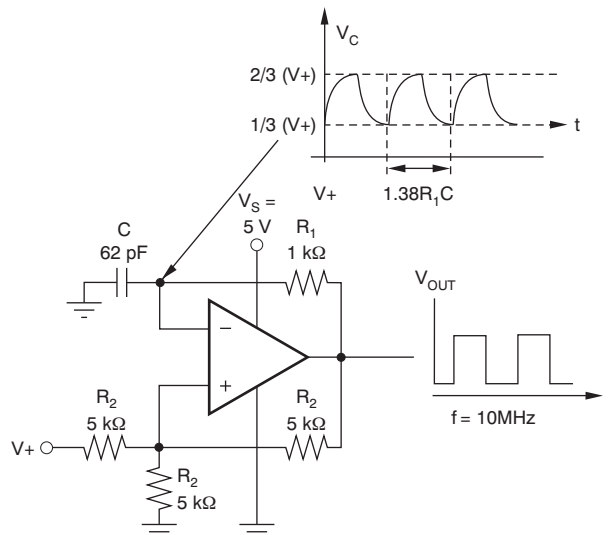


Figure 18. Relaxation Oscillator

High-Speed Window Comparator

A window comparator circuit is used to determine when a signal is between two voltages. The TLV3501-Q1 can readily be used to create a high-speed window comparator. V_{HI} is the upper voltage threshold, and V_{LO} is the lower voltage threshold. When V_{IN} is between these two thresholds, the output in Figure 19 is high. Figure 20 shows a simple means of obtaining an active low output. Note that the reference levels are connected differently between Figure 19 and Figure 20. The operating voltage range of either circuit is 2.7 V to 5.5 V.

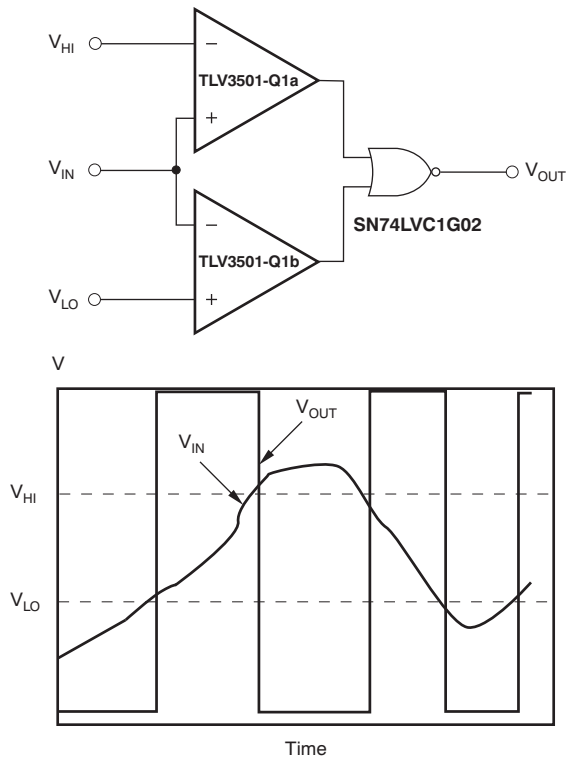


Figure 19. Window Comparator: Active High

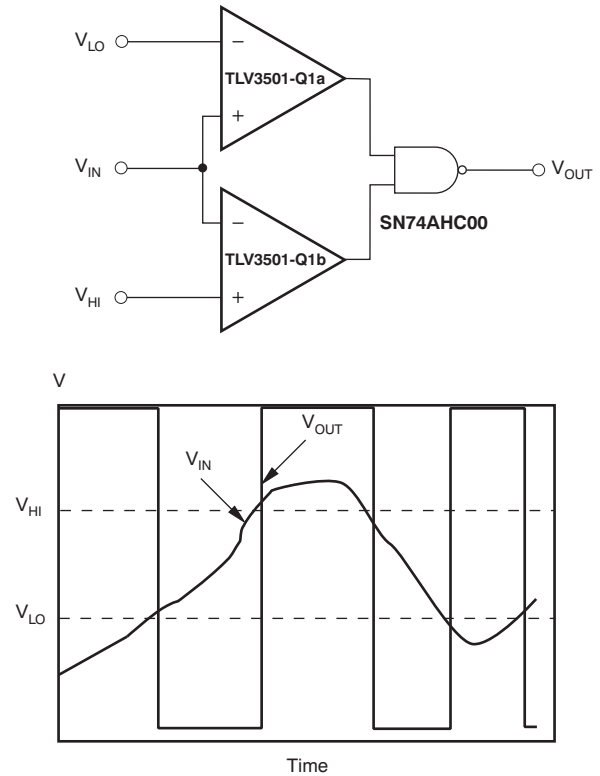


Figure 20. Window Comparator: Active Low

PCB Layout

For any high-speed comparator or amplifier, proper design and printed circuit board (PCB) layout are necessary for optimal performance. Excess stray capacitance on the active input, or improper grounding, can limit the maximum performance of high-speed circuitry.

Minimizing resistance from the signal source to the comparator input is necessary in order to minimize the propagation delay of the complete circuit. The source resistance along with input and stray capacitance creates an RC filter that delays voltage transitions at the input, and reduces the amplitude of high-frequency signals. The input capacitance of the TLV350x along with stray capacitance from an input pin to ground results in several picofarads of capacitance.

The location and type of capacitors used for power-supply bypassing are critical to high-speed comparators. The suggested 2.2- μ F tantalum capacitor do not need to be as close to the device as the 0.1- μ F capacitor, and may be shared with other devices. The 2.2- μ F capacitor buffers the power-supply line against ripple, and the 0.1- μ F capacitor provides a charge for the comparator during high-frequency switching.

In a high-speed circuit, fast rising and falling switching transients create voltage differences across lines that would be at the same potential at DC. To reduce this effect, a ground plane is often used to reduce difference in voltage potential within the circuit board. A ground plane has the advantage of minimizing the effect of stray capacitances on the circuit board by providing a more desirable path for the current to flow. With a signal trace over a ground plane, at high-frequency the return current (in the ground plane) tends to flow right under the signal trace. Breaks in the ground plane (as simple as through-hole leads and vias) increase the inductance of the plane, making it less effective at higher frequencies. Breaks in the ground plane for necessary vias should be spaced randomly.

Figure 21 shows an evaluation layout for the TLV3501-Q1 SOT23-6 package. Both are shown with SMA connectors bringing signals on and off the board. RT1 and RT2 are termination resistors for $+V_{IN}$ and $-V_{IN}$, respectively. C1 and C2 are power-supply bypass capacitors. Place the 0.1- μ F capacitor closest to the comparator. The ground plane is not shown, but the pads that the resistors and capacitors connect to are shown. Figure 22 shows a schematic of this circuit.

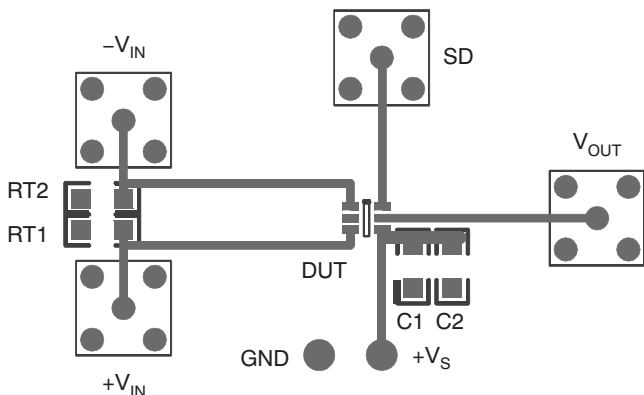


Figure 21. TLV3501DBV (SOT23) Sample Layout

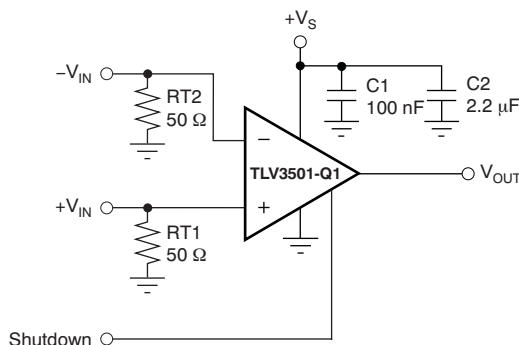


Figure 22. Schematic for Figure 21

REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (September, 2010) to Revision A	Page
• Added new feature bullet regarding automotive application qualification	1

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/ Ball Finish	MSL Peak Temp ⁽³⁾	Samples (Requires Login)
TLV3501AQDBVRQ1	ACTIVE	SOT-23	DBV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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TAPE AND REEL INFORMATION
REEL DIMENSIONS

TAPE DIMENSIONS


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV3501AQDBVRQ1	SOT-23	DBV	6	3000	180.0	8.4	3.2	3.1	1.39	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS

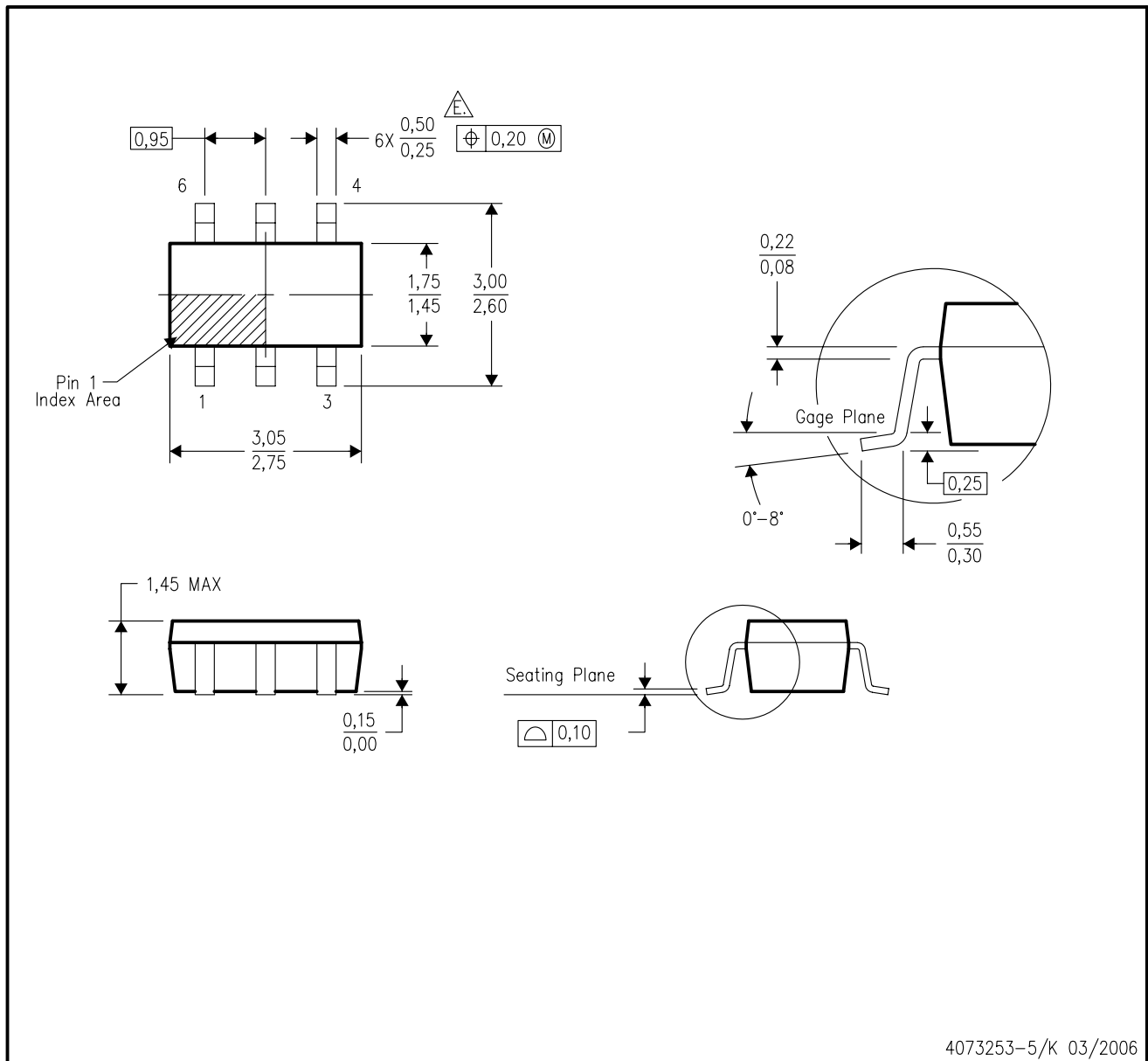


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLV3501AQDBVRQ1	SOT-23	DBV	6	3000	210.0	185.0	35.0

DBV (R-PDSO-G6)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
 - D. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
- $\triangle E$ Falls within JEDEC MO-178 Variation AB, except minimum lead width.

DBV (R-PDSO-G6)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
 - D. Publication IPC-7351 is recommended for alternate designs.
 - E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.

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