4.25 Gbps Cable and PC Board Equalizer

FEATURES

- **Multi-Rate Operation Up To 4.25 Gbps**
- **Compensates Up To 12 dB Loss At 2.1 GHz**
- **Suitable To Receive 4.25-Gbps Data Over Up To 30 Inches (0,76 Meters) Of FR4 PC Boards**
- **Suitable To Receive 4.25-Gbps Data Over Up To 30 Feet (9,1 Meters) Of CX4 Cable**
- **Ultra-Low Power Consumption**
- **Input Offset Cancellation**
- **High Input Dynamic Range**
- **Output Disable**
- **Output Polarity Select**
- **CML Data Outputs**
- **Single 3.3-V Supply**
- **Surface Mount Small Footprint 3 mm × 3 mm 16-Pin QFN Package**

APPLICATIONS

- **1.0625 Gbps, 2.125 Gbps, and 4.25 Gbps Fibre Channel Systems**
- **High Speed Links In Communication and Data Systems**
- **Backplane Interconnect**
- **Rack-to-Rack Interconnect**

DESCRIPTION

The TLK4211EA is a versatile high-speed limiting equalizer for applications in digital high-speed links with data rates up to 4.25 Gbps.

This device provides a high frequency boost of 12 dB at 2.1 GHz as well as sufficient gain to ensure a fully differential output swing for input signals as low as 200 mVp-p (at the input of the interconnect line).

The high input signal dynamic range ensures low jitter output signals even when overdriven with input signal swings as high as 2000 mVp-p.

The TLK4211EA is available in a small footprint 3 mm × 3 mm 16-pin QFN package. It requires a single 3.3-V supply.

This power efficient equalizer is characterized for operation from –40°C to 85°C.

BLOCK DIAGRAM

A simplified block diagram of the TLK4211EA is shown in Figure 1.

This compact, low-power 4.25-Gbps equalizer consists of a high-speed data path with offset cancellation circuitry, a bandgap voltage reference, and bias current generation block.

The equalizer requires a single 3.3-V supply voltage. All circuit parts are described in detail in below.

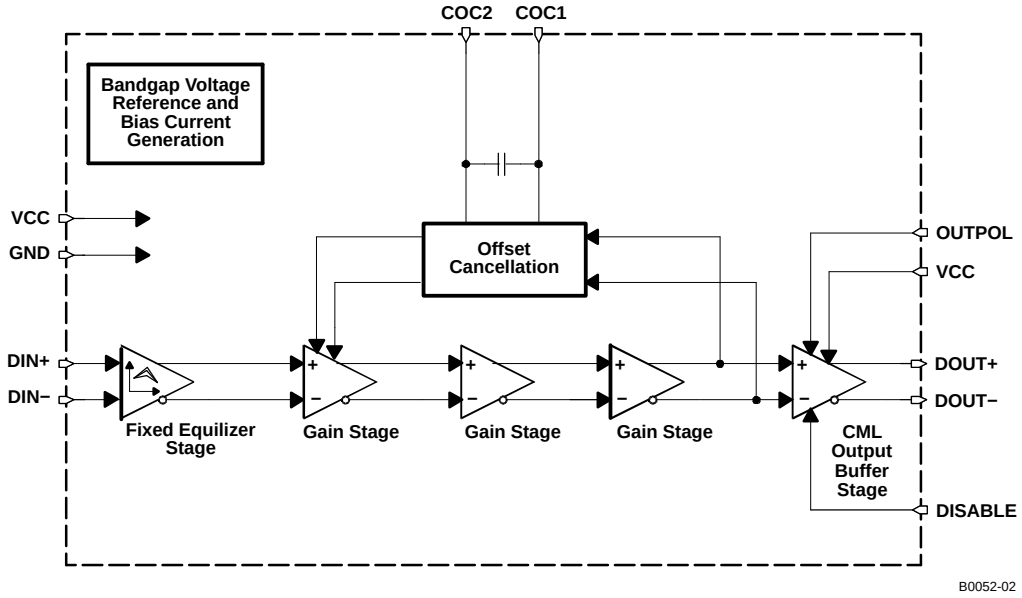


Figure 1. Simplified Block Diagram of the TLK4211EA

HIGH-SPEED DATA PATH

The high-speed data signal with frequency dependent loss is applied to the data path by means of the input signal pins DIN+/DIN–. The data path consists of the fixed equalizer input stage with 100-Ω differential on-chip line termination, three gain stages, which provide the required gain to ensure a limited output signal, and a CML output stage. The equalized and amplified data output signal is available at the output pins DOUT+/DOUT–, which provide 2 × 50-Ω back-termination to VCC. The output stage also includes a data polarity switching function, which is controlled by the OUTPOL input, and a disable function controlled by the signal applied to the DISABLE input pin.

An offset cancellation compensates inevitable internal offset voltages and thus ensures proper operation even for small input data signals.

The low frequency cutoff is as low as 10 kHz with the built-in filter capacitor.

For applications which require even lower cutoff frequencies, an additional external filter capacitor may be connected to the COC1/COC2 pins.

BANDGAP VOLTAGE AND BIAS GENERATION

The TLK4211EA equalizer is supplied by a single 3.3-V ±10% supply voltage connected to the VCC pins. This voltage is referred to ground (GND).

An on-chip bandgap voltage circuitry generates a supply voltage independent reference from which all other internally required voltages and bias currents are derived.

PACKAGE

The TLK4211EA is available in a small footprint 3 mm × 3 mm, 16-pin QFN package with a lead pitch of 0,5 mm. The pin out is shown below in Figure 2.

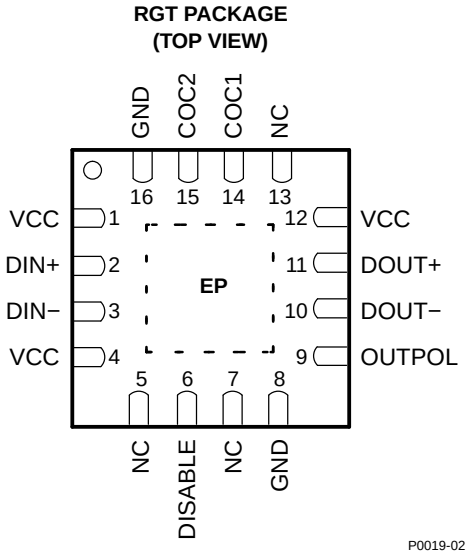


Figure 2. Pin Out of TLK4211EA in a 3 mm × 3 mm 16-Pin QFN Package

TERMINAL FUNCTIONS

TERMINAL		TYPE	DESCRIPTION
NAME	NO.		
VCC	1, 4 , 12	Supply	3.3-V ±10% supply voltage
DIN+	2	Analog in	Non-inverted data input. On-chip 100-Ω terminated to DIN–
DIN–	3	Analog in	Inverted data input. On-chip 100-Ω terminated to DIN+
NC	5, 7, 13		Not connected
DISABLE	6	CMOS in	Disables CML output stage when set to high level
GND	8, 16	Supply	Circuit ground.
OUTPOL	9	CMOS in	Output data signal polarity select (internally pulled up): Setting to high-level or leaving pin open selects normal polarity. Low-level selects inverted polarity.
DOUT–	10	CML out	Inverted data output. On-chip 50-Ω back-terminated to VCC.
DOUT+	11	CML out	Non-inverted data output. On-chip 50-Ω back-terminated to VCC.
COC1	14	Analog	Offset cancellation filter capacitor terminal 1. Connect an additional filter capacitor between this pin and COC2 (pin 15). To disable the offset cancellation loop connect COC1 and COC2 (pins 14 and 15).
COC2	15	Analog	Offset cancellation filter capacitor terminal 2. Connect an additional filter capacitor between this pin and COC1 (pin 14). To disable the offset cancellation loop connect COC1 and COC2 (pins 14 and 15).
EP	EP		Exposed die pad (EP) must be grounded.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)(1)

		VALUE / UNIT
V_{CC}	Supply voltage(2)	–0.3 V to 4 V
V_{DIN+}, $V_{DIN–}$	Voltage at DIN+, DIN–(2)	0.5 V to 4 V
$V_{DISABLE}$, V_{OUTPOL}, V_{DOUT+}, $V_{DOUT–}$, V_{COC1}, V_{COC2}	Voltage at DISABLE, OUTPOL, DOUT+, DOUT–, COC1, COC2(2)	–0.3 V to 4 V
$V_{COC,DIFF}$	Differential voltage between COC1 and COC2	±1 V
$V_{DIN,DIFF}$	Differential voltage between DIN+ and DIN–	±2.5 V
I_{DIN+}, $I_{DIN–}$, I_{DOUT+}, $I_{DOUT–}$	Continuous current at inputs and outputs	– 25 mA to 25 mA
ESD	ESD rating at all pins	2.5 kV (HBM)
$T_{J(max)}$	Maximum junction temperature	125°C
T_{STG}	Storage temperature range	–65°C to 85°C
T_A	Characterized free-air operating temperature range	–40°C to 85°C
T_L	Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute–maximum–rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network ground terminal.

RECOMMENDED OPERATING CONDITIONS

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	3	3.3	3.6	V
T_A	Operating free-air temperature	–40		85	°C
	CMOS input high voltage	2.1			V
	CMOS input low voltage			0.6	V

DC ELECTRICAL CHARACTERISTICS

over recommended operating conditions, typical operating condition is at V_{CC} = 3.3 V and T_A = 25°C(unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{CC}	Supply voltage		3	3.3	3.6	V
I_{CC}	Supply current	DISABLE = low, including CML output current		30	38	mA
R_{IN}	Data input resistance	Differential		100		Ω
R_{OUT}	Data output resistance	Single-ended to VCC		50		Ω

AC ELECTRICAL CHARACTERISTICS

over recommended operating conditions, typical operating condition is at V_{CC} = 3.3 V and T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Low frequency –3 dB bandwidth	C_{OC} = open		10	50	kHz
		C_{OC} = 0.22 µF		0.8		
	Data rate		4.25			Gbps
$V_{IN,MIN}$	Data input sensitivity(1)	BER < $10^{–12}$, voltage at the input of the interconnect line		200	250	mV_{p-p}
$V_{IN,MAX}$	Data input overload	Voltage at the input of the interconnect line	2000			mV_{p-p}
	High frequency boost	f = 2.1 GHz		12		dB
V_{OD}	Differential data output voltage swing	DISABLE = high		0.25	10	mV_{p-p}
		DISABLE = low	580	780	1200	

(1) The given differential input signal swing is measured at the input of the interconnect line. The high frequency components of the signal at the output of the interconnect line (which is connected the input pins DIN+/DIN– of the TLK4211EA) may be attenuated by 0 dB up to 12 dB at 2.1 GHz dependent of the interconnect line length.

AC ELECTRICAL CHARACTERISTICS (continued)

over recommended operating conditions, typical operating condition is at V_{CC} = 3.3 V and T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DJ	Deterministic jitter, 4.25 Gbps, K28.5 pattern, V_{IN} = 200 mVpp (differential voltage at the cable input)	No board or cable		20		ps_{p-p}
		12 inches of 7 mils wide microstrip interconnect line on standard FR4		30		
		24 inches of 7 mils wide microstrip interconnect line on standard FR4		30		
		36 inches of 7 mils wide microstrip interconnect line on standard FR4		30		
		30 feet CX4 cable		20		
	Deterministic jitter, 3.3 Gbps, K28.5 pattern, V_{IN} = 200 mVpp (differential voltage at the cable input)	No board or cable		20		ps_{p-p}
		48 inches of 7 mils wide microstrip interconnect line on standard FR4		25		
		30 feet CX4 cable		20		
RJ	Random jitter	Input = 200 mV_{p-p}, 36 inches of 7 mils wide stripline interconnect line on standard FR4 (voltage at the input of the interconnect line)		4.5		ps_{RMS}
	Latency	From DIN± to DOUT±		250		ps
t_r	Output rise time	20% to 80%, without microstrip line loss at input		55	85	ps
t_f	Output fall time	20% to 80%, without microstrip line loss at input		55	85	ps
T_{DIS}	Disable response time			20		ns

APPLICATION INFORMATION

Figure 3 shows the TLK4211EA connected with an ac-coupled interface to the data signal source via a microstrip interconnect line. The output load is ac-coupled as well.

The ac coupling capacitors C_1 through C_4 in the input and output data signal lines are the only required external components. In addition, if a low cutoff frequency is required, as an option, an external filter capacitor C_{OC} may be used.

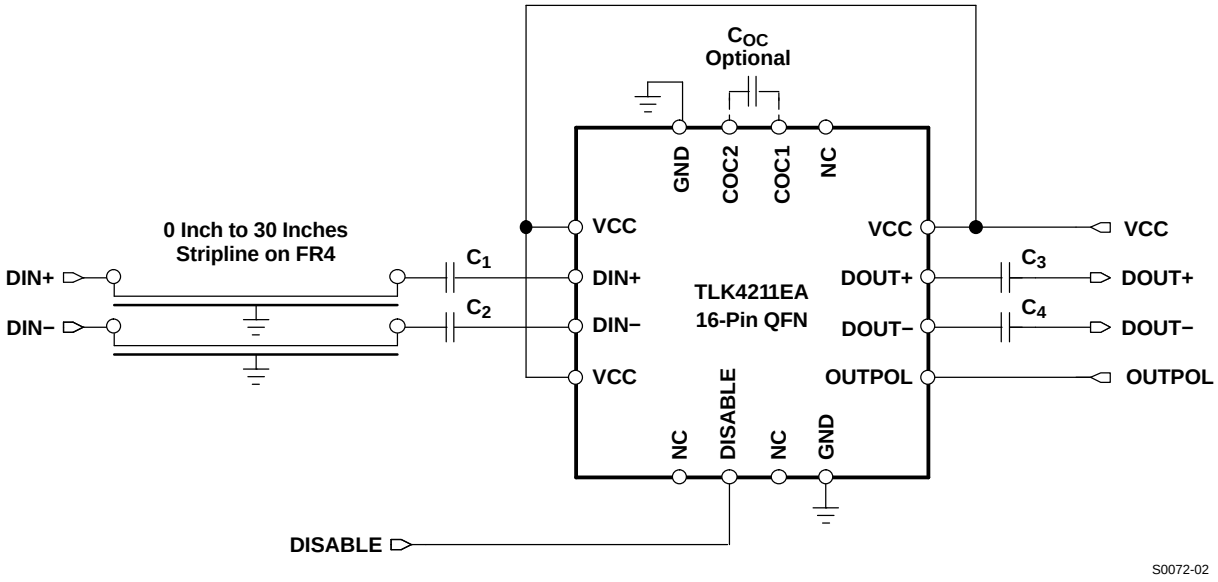


Figure 3. Basic Application Circuit With AC Coupled I/Os

TYPICAL CHARACTERISTICS

Typical operating condition is at V_{CC} = 3.3 V and T_A = 25°C (unless otherwise noted).

DIFFERENTIAL EQUALIZER INPUT SIGNAL (TOP) AND OUTPUT SIGNAL (BOTTOM) AT 4.25 GBPS USING A K28.5 PATTERN

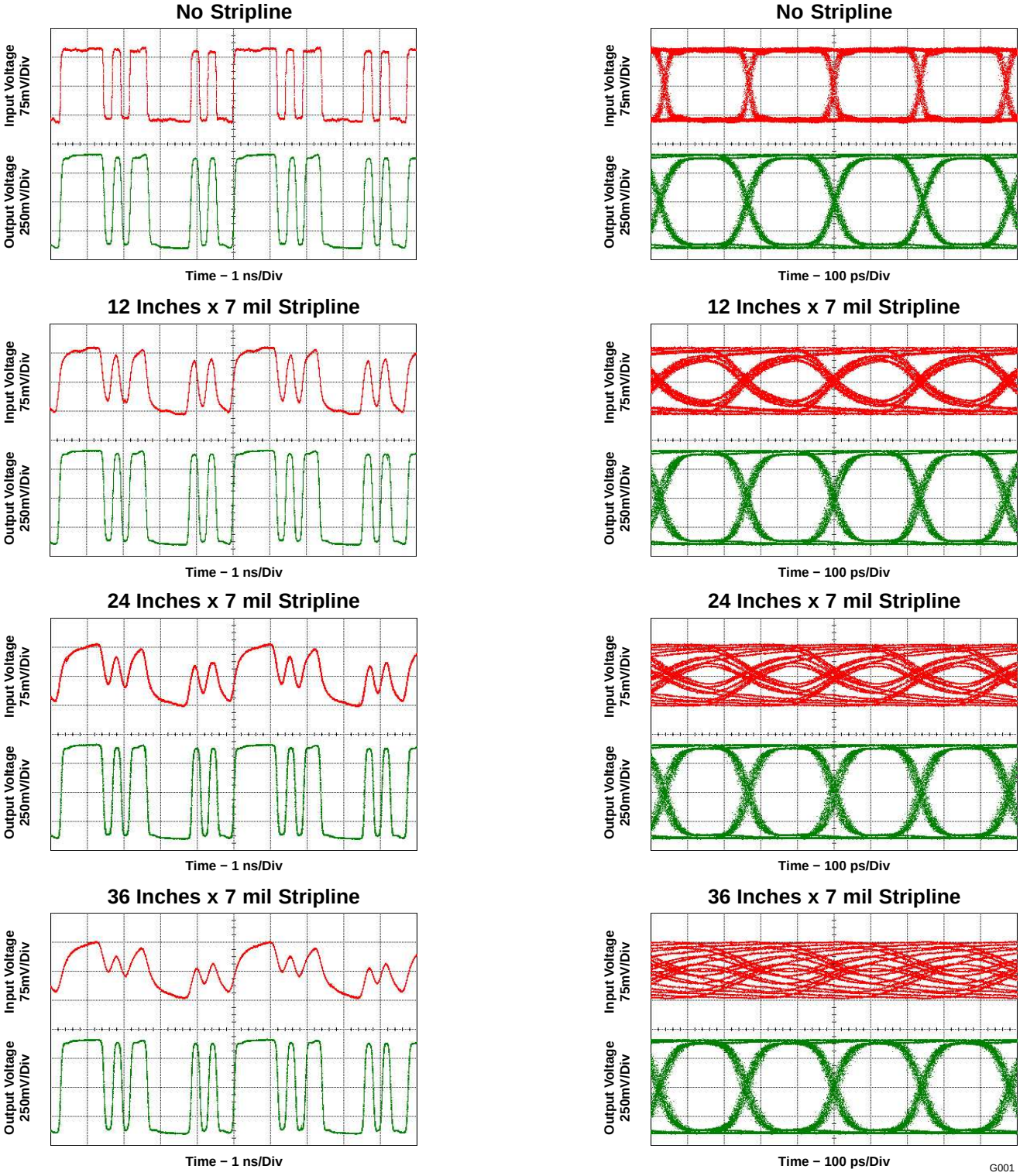


Figure 4. Equalizer Input and Output Signals With Different Interconnect Lines Patterns

TYPICAL CHARACTERISTICS (continued)

Typical operating condition is at V_{CC} = 3.3 V and T_A = 25°C (unless otherwise noted).

DIFFERENTIAL EQUALIZER INPUT SIGNAL (TOP) AND OUTPUT SIGNAL (BOTTOM) AT 3.3 GBPS USING A K28.5 PATTERN

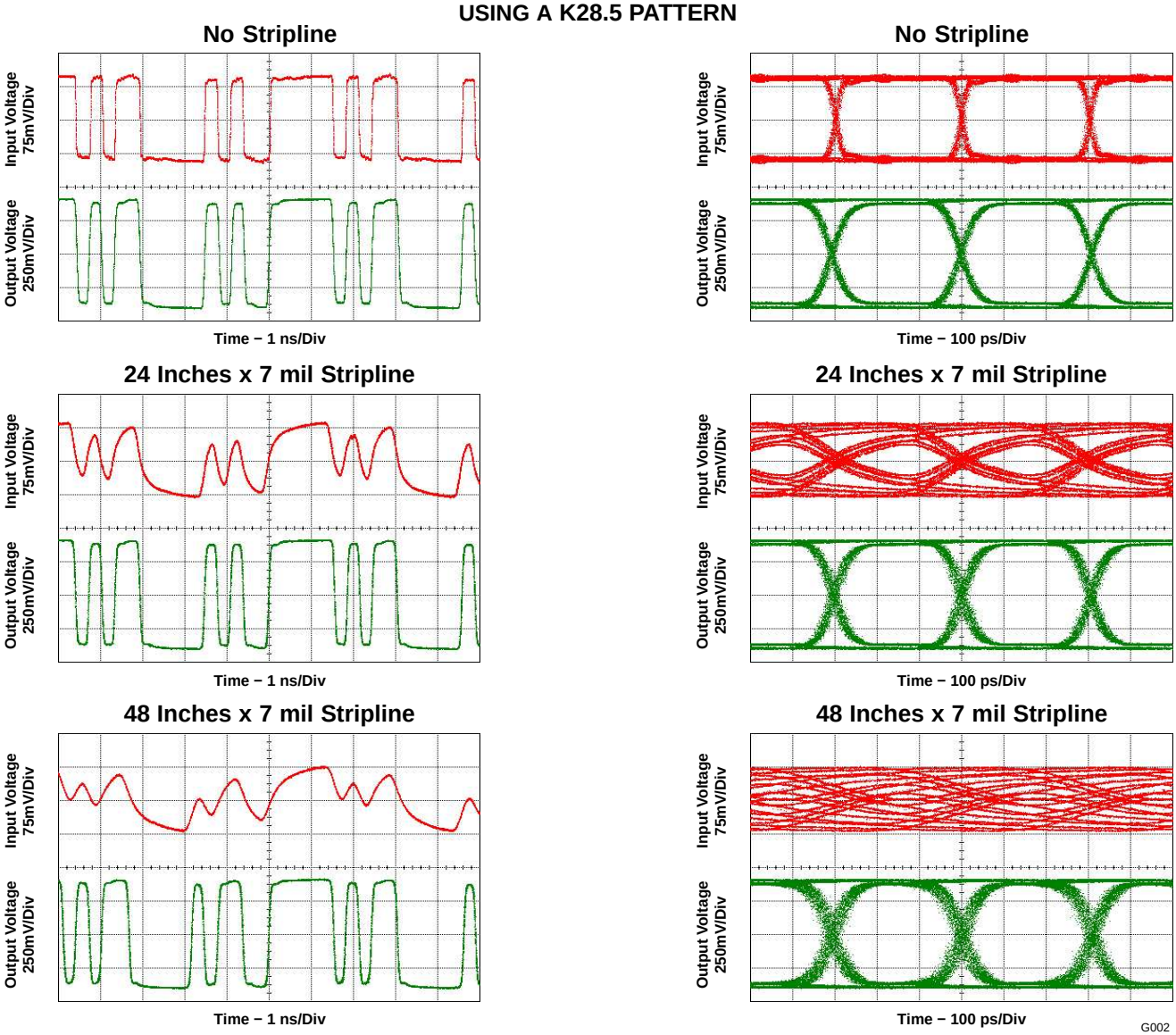


Figure 5. Equalizer Input and Output Signals With Different Interconnect Lines and Data

TYPICAL CHARACTERISTICS (continued)

Typical operating condition is at V_{CC} = 3.3 V and T_A = 25°C (unless otherwise noted).

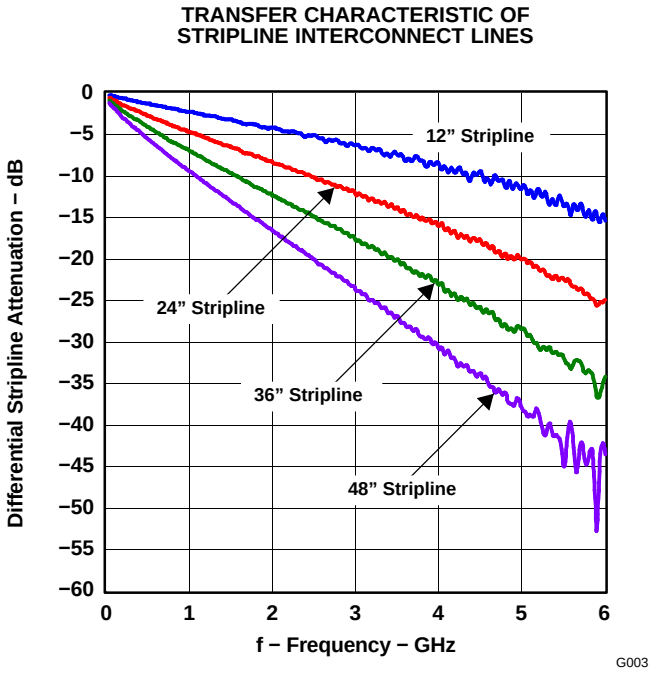


Figure 6.

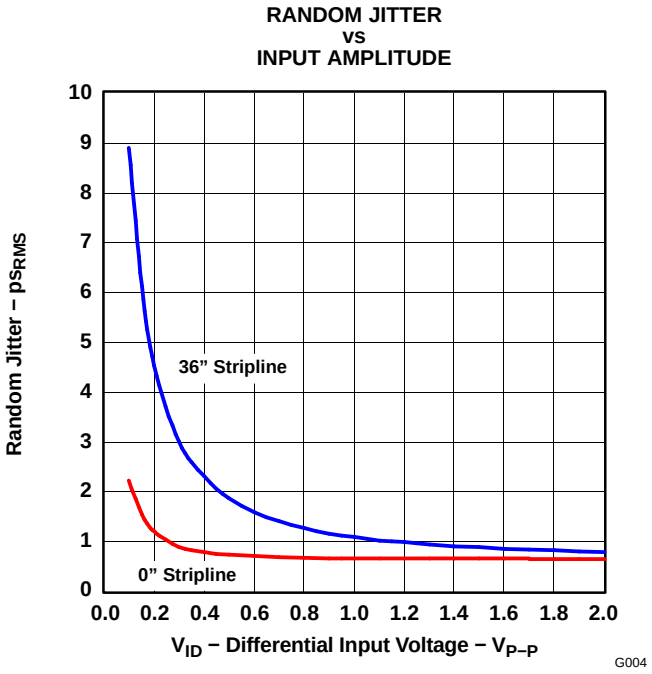


Figure 7.

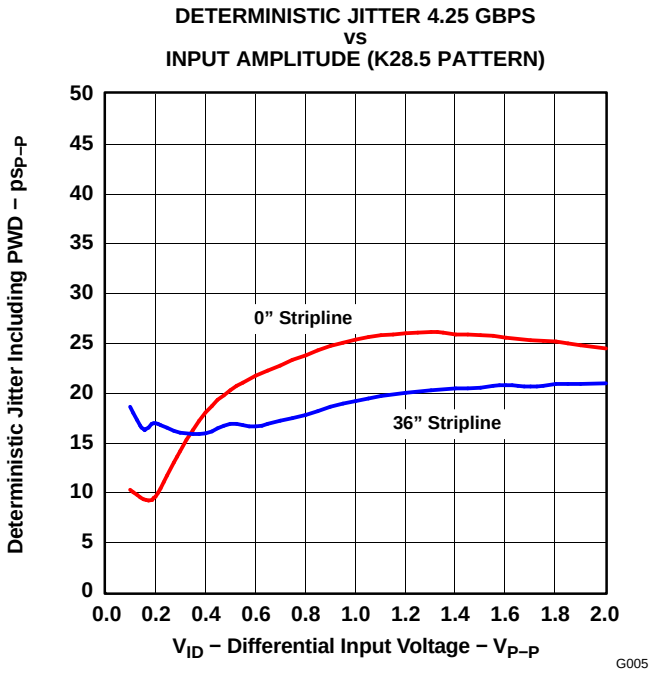


Figure 8.

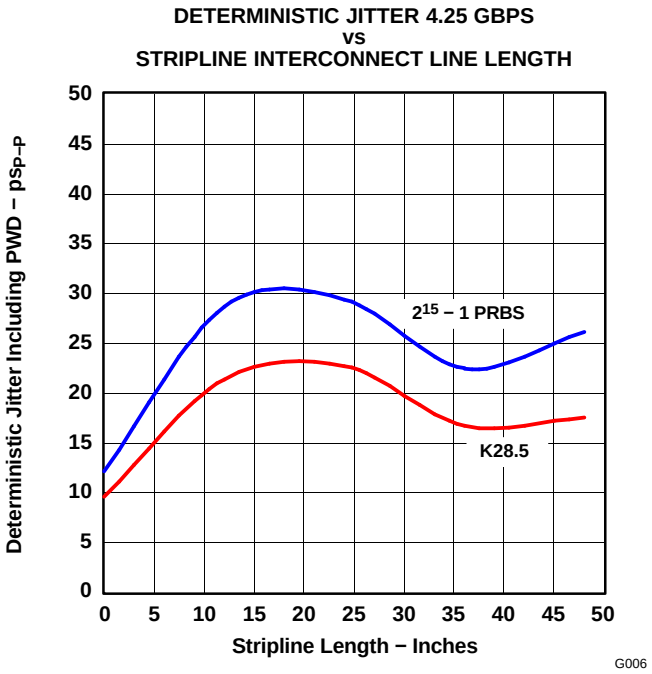


Figure 9.

TYPICAL CHARACTERISTICS (continued)

Typical operating condition is at V_{CC} = 3.3 V and T_A = 25°C (unless otherwise noted).

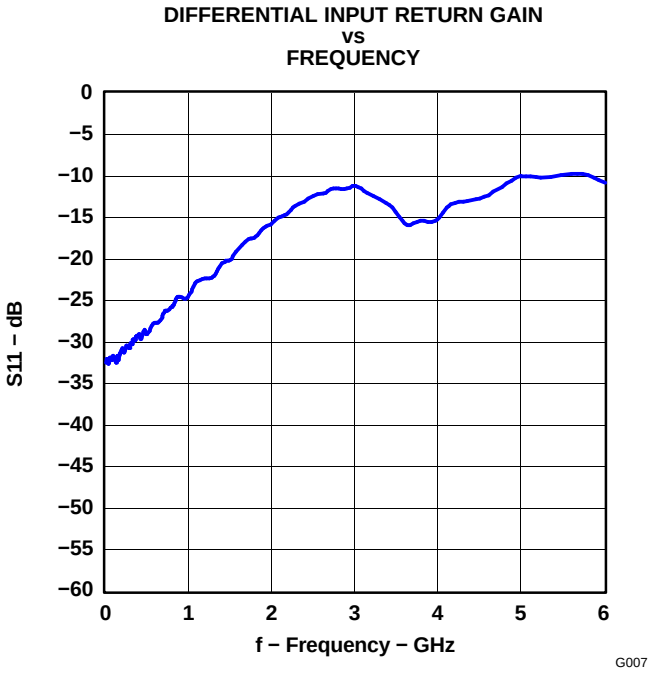


Figure 10.

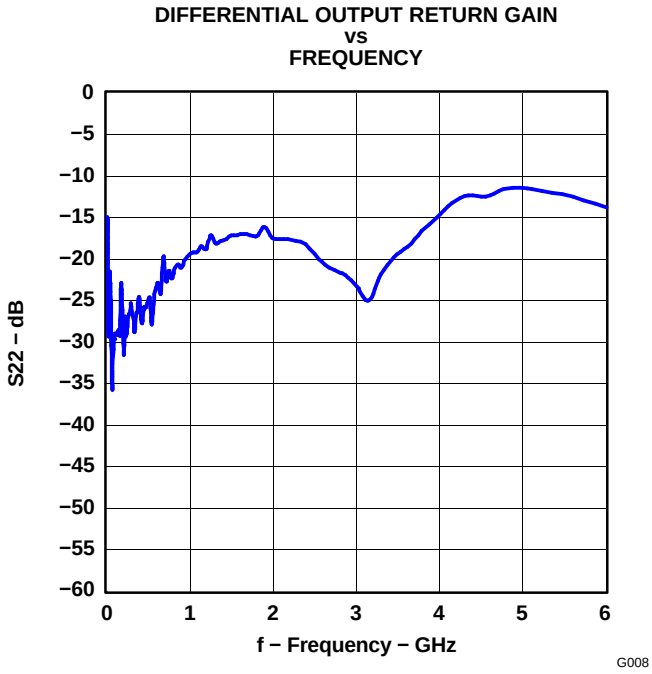


Figure 11.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
TLK4211EARGTR	OBSOLETE	QFN	RGT	16		TBD	Call TI	Call TI	-40 to 85	421E	
TLK4211EARGTRG4	OBSOLETE	QFN	RGT	16		TBD	Call TI	Call TI	-40 to 85		
TLK4211EARGTT	NRND	QFN	RGT	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	421E	
TLK4211EARGTTG4	NRND	QFN	RGT	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	421E	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

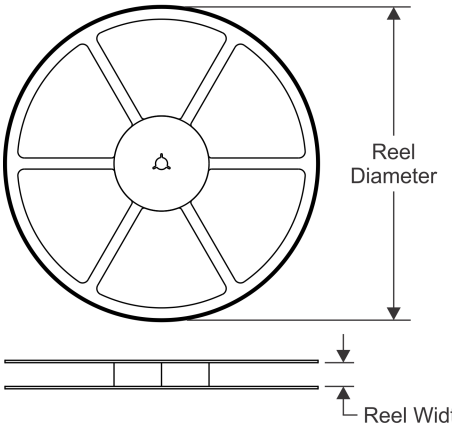
(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

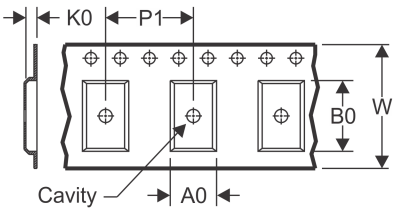
(4) Only one of markings shown within the brackets will appear on the physical device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

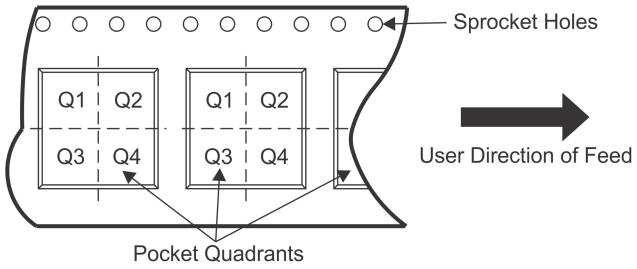


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

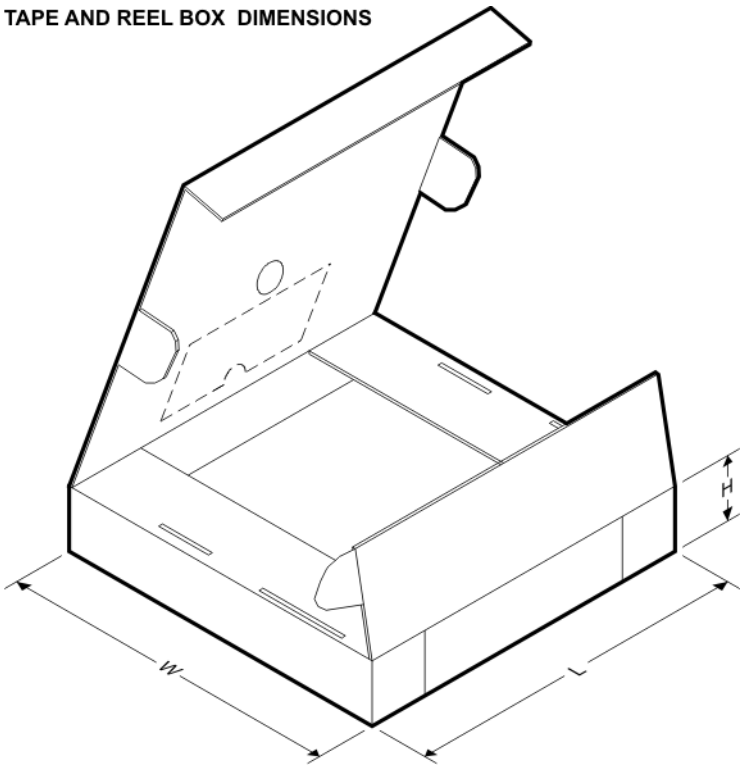
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLK4211EARGTT	QFN	RGT	16	250	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

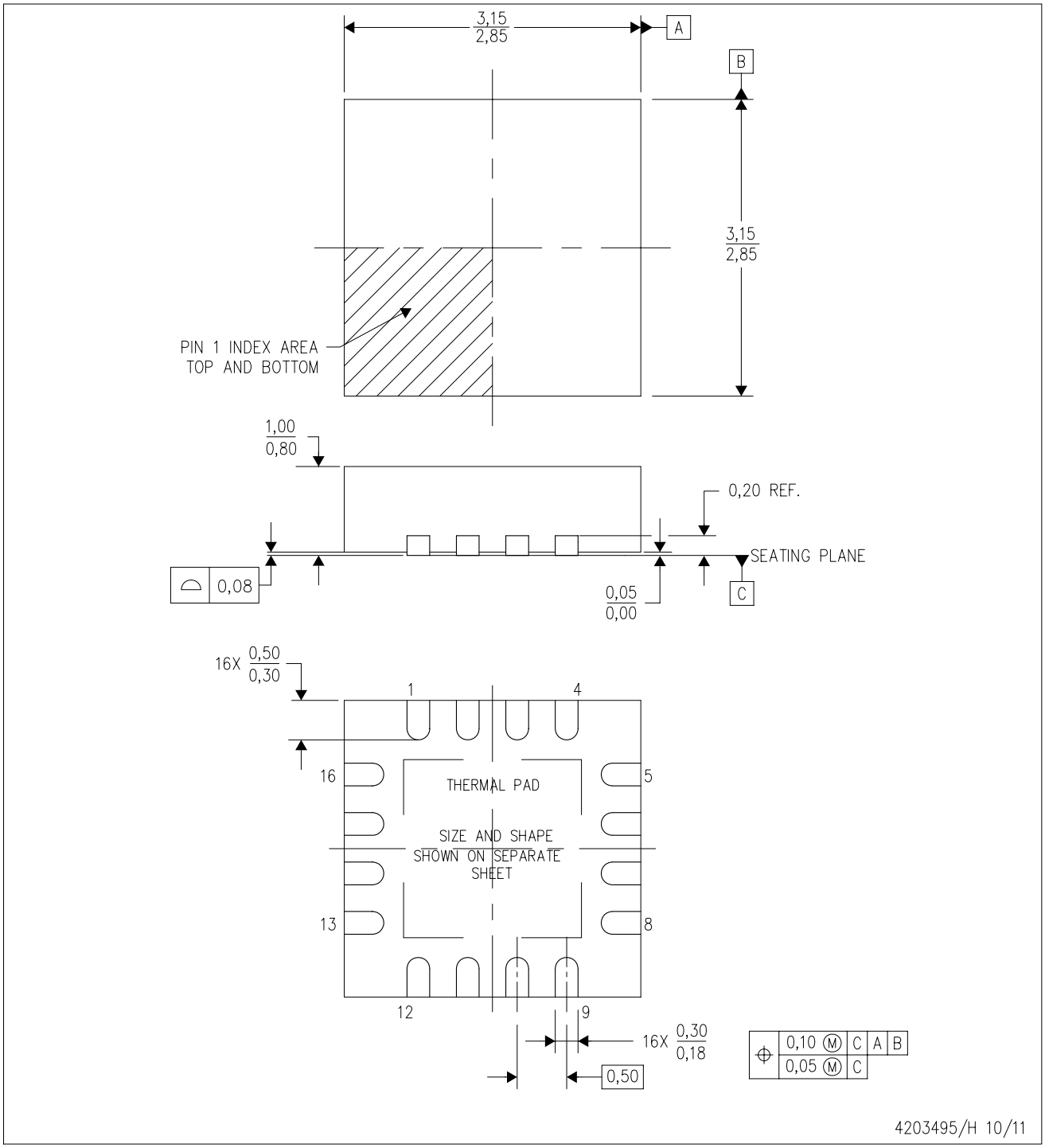
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLK4211EARGTT	QFN	RGT	16	250	338.1	338.1	20.6

RGT (S–PVQFN–N16) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Quad Flatpack, No–leads (QFN) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Falls within JEDEC MO–220.

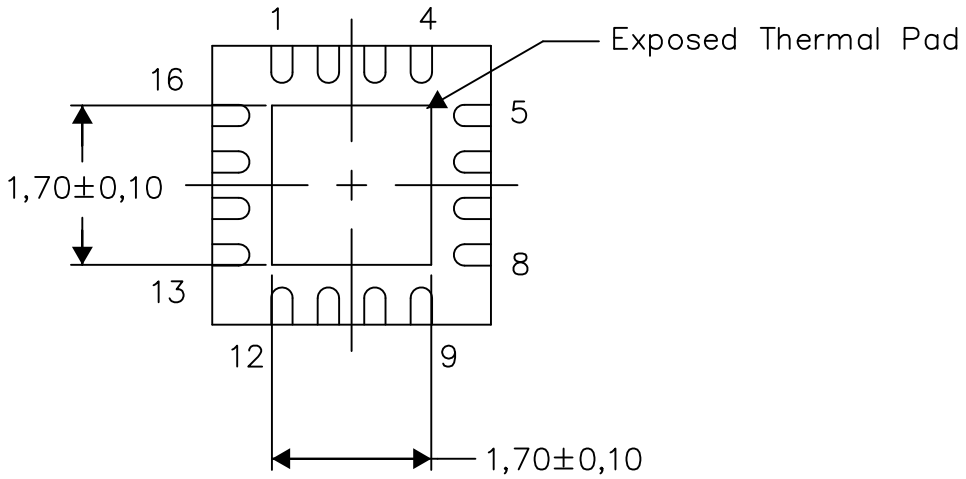
RGT (S–PVQFN–N16) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



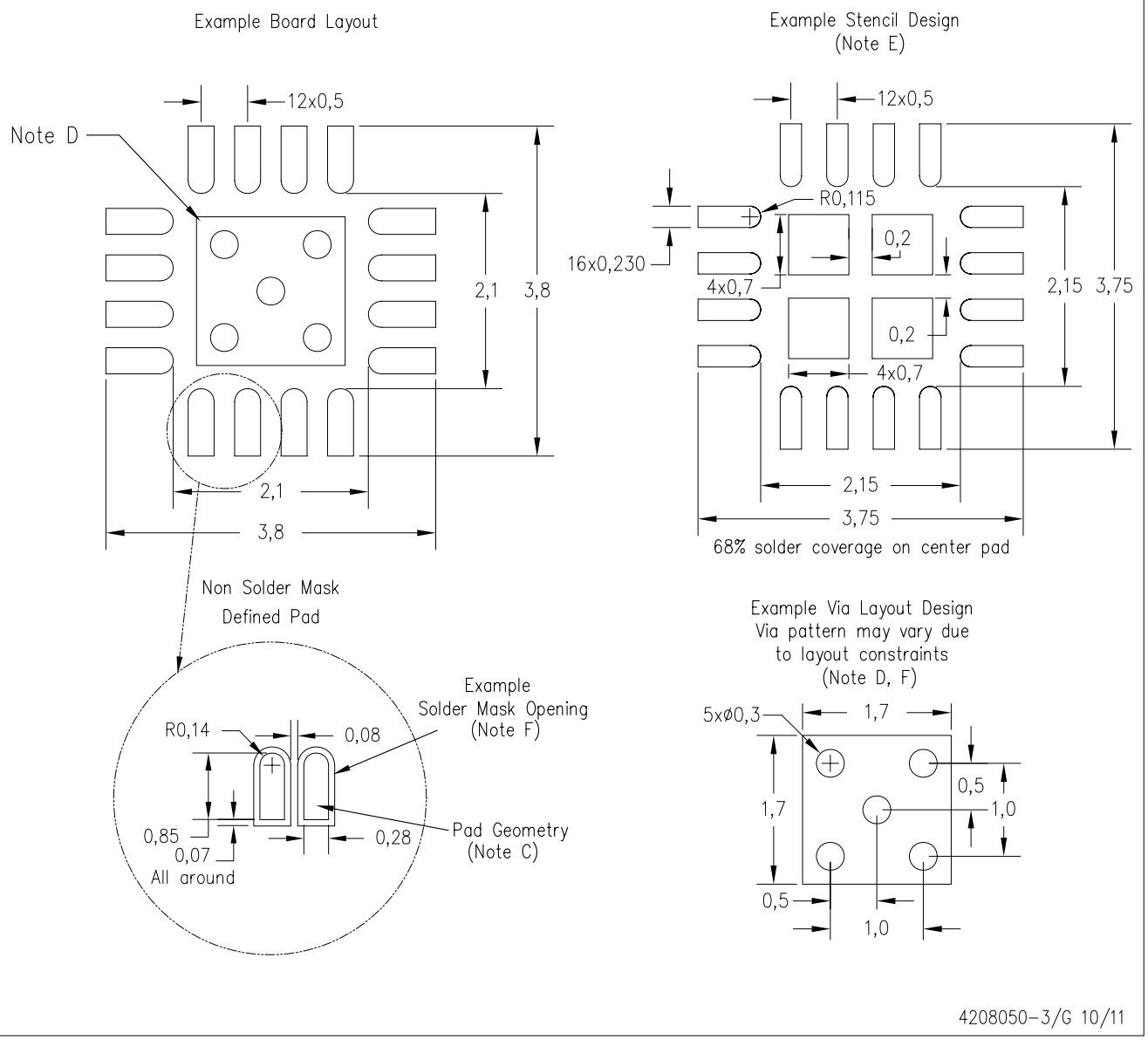
Bottom View

Exposed Thermal Pad Dimensions

4206349–4/R 12/12

NOTE: All linear dimensions are in millimeters

RGT (S–PVQFN–N16) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

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