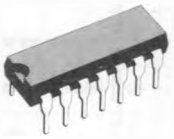
LOW NOISE JFET-INPUT QUAD OPERATIONAL AMPLIFIERS

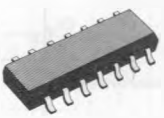
- LOW-NOISE
- LOW INPUT BIAS AND OFFSET CURRENTS
- HIGH INPUT IMPEDANCE . . . JFET-INPUT STAGE
- LOW POWER CONSUMPTION
- WIDE COMMON-MODE AND DIFFERENTIAL VOLTAGE RANGES
- OUTPUT SHORT-CIRCUIT PROTECTION
- INTERNAL FREQUENCY COMPENSATION
- LATCH-UP-FREE OPERATION
- HIGH SLEW-RATE . . . 13V/μs TYP.

The TL074 JFET-input operational amplifiers are designed to offer low-noise high slew-rate, low input bias and offset current, and low offset voltage temperature coefficient. Each JFET-input operational amplifier incorporates well-matched, high-voltage JFET and bipolar transistors in a monolithic integrated circuit.

Devices with an "I" suffix are characterized for operation from -25°C to 85°C, and those with a "C" suffix are characterized for operation from 0°C to 70°C.

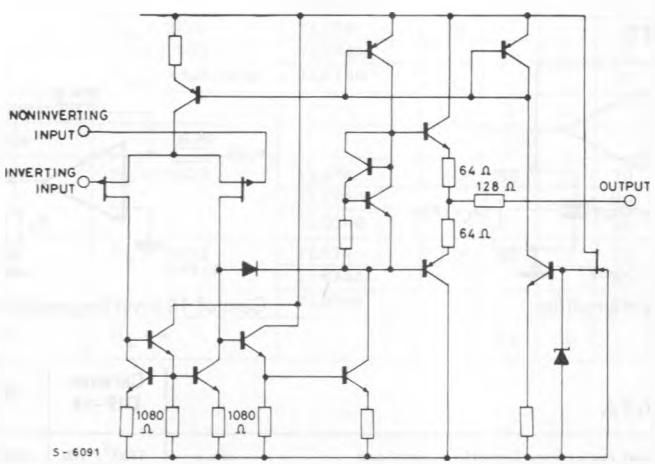


DIP-14
(Plastic and Ceramic)



SO-14 J

SCHEMATIC DIAGRAM
(one section)

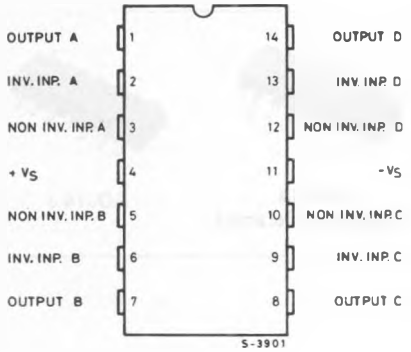


ABSOLUTE MAXIMUM RATINGS

V_s	Supply voltage	± 18	V
V_{is}	Differential input voltage	± 30	V
V_i	Input voltage	± 15	V
T_{op}	Operating temperature (TL074I)	-25 to 85	°C
	(TL074C)	0 to 70	°C
T_j	Junction temperature	150	°C
T_{stg}	Storage temperature	-55 to 150	°C

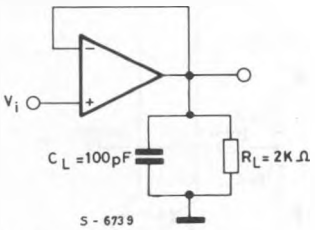
CONNECTION DIAGRAM AND ORDERING NUMBERS

(Top view)

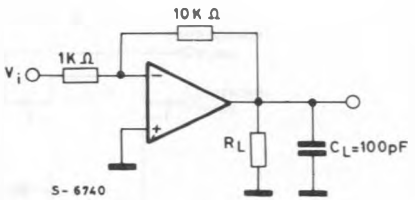


0 to 70°C	-25 + 85°C	Package
TL074CJ TL074ACJ TL074BCJ	TL074IJ — —	Ceramic DIP-14
TL074CN TL074ACN TL074BCN	TL074IN — —	Plastic DIP-14
TL074CD	TL074ID	SO-14

TEST CIRCUITS



Unity gain amplifier



Gain of 10 inverting amplifier

THERMAL DATA

			Ceramic DIP-14	SO-14	Plastic DIP-14
$R_{th\ j\text{-}amb}$	Thermal resistance junction-ambient	max	150°C/W	165°C/W	200°C/W

ELECTRICAL CHARACTERISTICS (V_s = 15V, T_{amb} = 25°C, otherwise specified)

Parameter		Test conditions		"I"			"C"			Unit
				Min.	Typ.	Max.	Min.	Typ.	Max.	
V_{OS}	Input offset voltage	R_s = 50Ω	TL074		3	6		3	10	mV
			TL074A					3	6	
			TL074B					2	3	
		R_s = 50Ω, T_{amb} = full range	TL074			9			13	
			TL074A						7.5	
			TL074B						5	
$\frac{\Delta V_{OS}}{\Delta T}$	Input offset voltage drift	R_s = 50Ω, T_{amb} = full range			10			10		µV/°C
I_{OS}	Input offset current		TL074		5	50		5	50	pA
			TL074A					5	50	
			TL074B					5	50	
		T_{amb} = full range	TL074			10			2	nA
			TL074A						2	
			TL074B						2	
I_b	Input bias current		TL074		30	200		30	200	pA
			TL074A					30	200	
			TL074B					30	200	
		T_{amb} = full range	TL074			20			7	nA
			TL074A						7	
			TL074B						7	
V_{CM}	Common mode input voltage range		TL074	± 11	± 12		± 10	± 11		V
			TL074A				± 11	± 12		
			TL074B				± 11	± 12		
V_{OPP}	Large signal voltage swing	T_{amb} = full range	R_L = 10KΩ	24	27		24	27		V
			R_L ≥ 10KΩ	24			24			
			R_L ≥ 2KΩ	20	24		20	24		
G_V	Large signal voltage gain	R_L ≥ 2KΩ, V_o = ± 10V	TL074	50	200		25	200		V/mV
			TL074A				50	200		
			TL074B				50	200		
		R_L ≥ 2KΩ, V_o = ± 10V, T_{amb} = full range	TL074	25			15			V/mV
			TL074A				25			
			TL074B				25			
B	Unity gain bandwidth				3			3		MHz
R_I	Input resistance				10^{12}			10^{12}		Ω
CMR	Common mode rejection	R_s ≥ 10KΩ	TL074	80	86		70	76		dB
			TL074A				80	86		
			TL074B				80	86		
SVR	Supply voltage rejection	R_s ≥ 10KΩ	TL074	80	86		70	76		dB
			TL074A				80	86		
			TL074B				80	86		
I_S	Supply current	R_L = ∞			5.6	10		5.6	10	mA

ELECTRICAL CHARACTERISTICS (continued)

Parameter		Test conditions		"I"			"C"			Unit
				Min.	Typ.	Max.	Min.	Typ.	Max.	
Cs	Channel separation	G_V = 100			120			120		dB
SR	Slew-rate at unity gain	V_I = 10V, C_L = 100pF	R_L = 2KΩ		13			13		V/μs
t_r	Rise time	V_I = 20mV	R_L = 2KΩ		0.1			0.1		μs
	Overshot factor	C_L = 100pF			10			10		%
e_N	Total input noise voltage	R_S = 100Ω	f = 1KHz		18			18		$\frac{nV}{\sqrt{Hz}}$
			f = 10Hz to 10KHz		4			4		μV
I_N	Input noise current	f = 1KHz			0.01			0.01		$\frac{pA}{\sqrt{Hz}}$
d	Total harmonic distortion	V_O = 10V_{rms}, $R_S \leq 1K\Omega$, $R_L > 2K\Omega$	f = 1KHz		0.01			0.01		%

Fig. 1 — Maximum peak to peak output voltage vs. frequency.

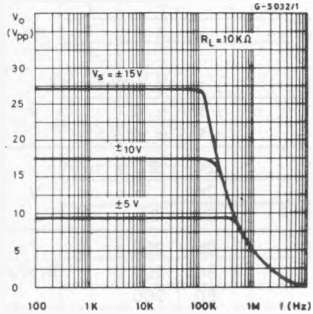


Fig. 2 — Maximum peak to peak output voltage vs. frequency

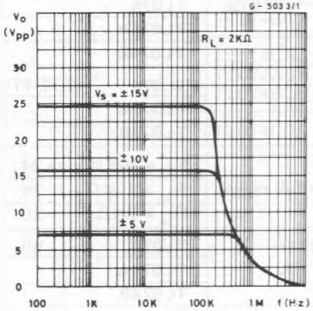


Fig. 3 — Maximum peak to peak output voltage vs. load resistance

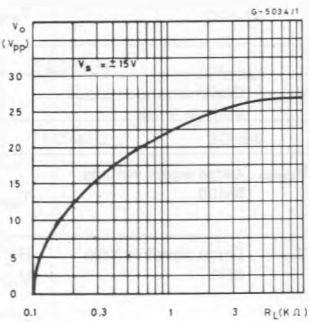


Fig. 4 — Large signal voltage gain and phase shift vs. frequency

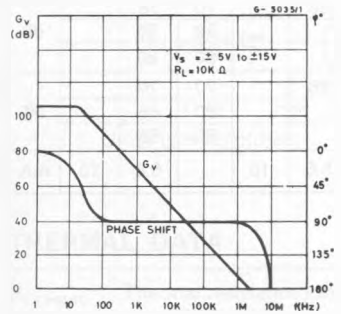


Fig. 5 Supply current vs. temperature

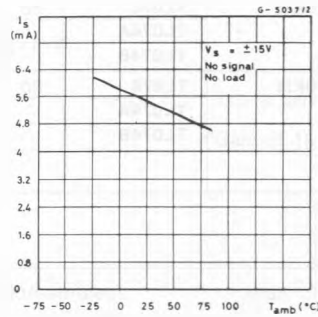


Fig. 6 — Supply current vs. supply voltage

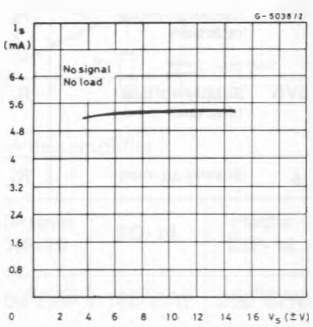


Fig. 7 – Input bias current vs. temperature

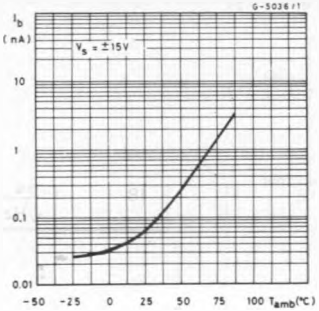


Fig. 8 – Voltage follower large signal pulse response

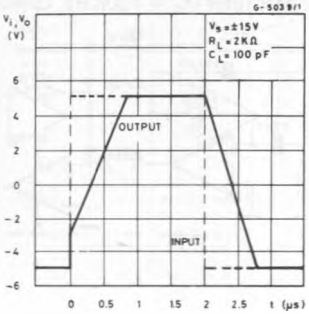


Fig. 9 – Output voltage vs. elapsed time

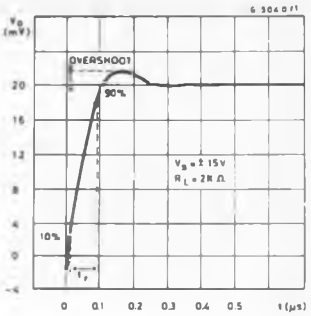


Fig. 10 – Equivalent input noise voltage vs. frequency

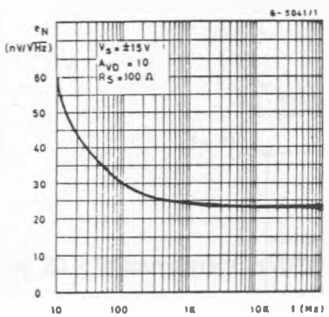


Fig. 11 – Total harmonic distortion vs. frequency

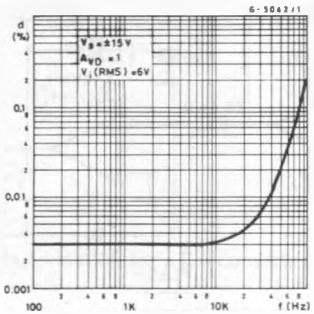
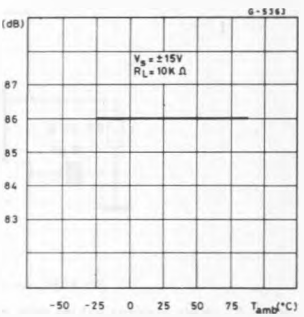
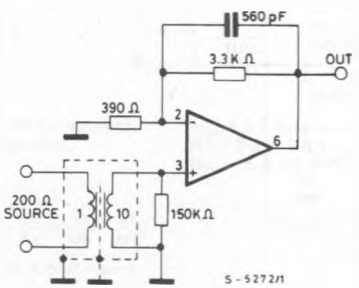


Fig. 12 Common mode rejection vs. temperature



APPLICATION INFORMATION

Fig. 13 - Low-Noise high Slew-Rate mike preamplifier (G_V = 40dB)



APPLICATION INFORMATION (continued)

Fig. 14 – Second order high Q band pass filter (f_o = 100KHz, Q = 30, gain = 4)

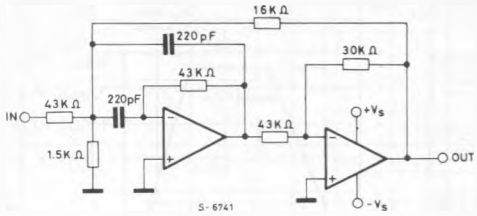
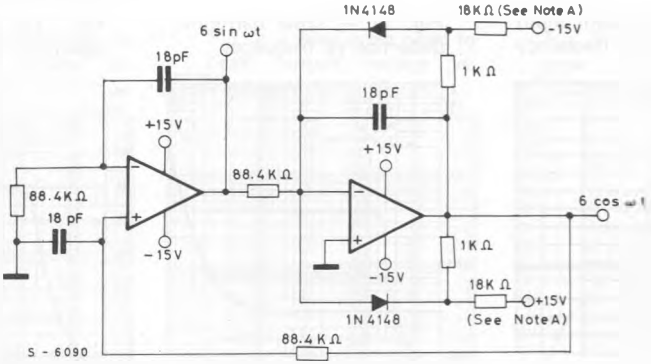


Fig. 15 – 100KHz quadrature oscillator



Note A: these resistor values may be adjusted for a simmetrical output

Fig 16 – 20Hz to 200Hz variable High-pass filter (G_v = 3dB)

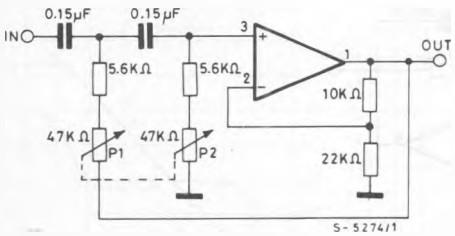
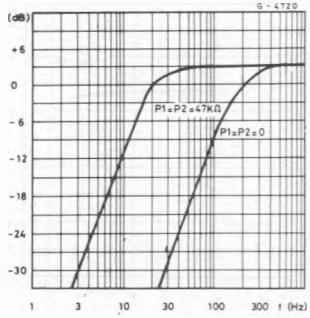


Fig. 17 – Frequency response fo the high-pass filter of fig. 16



APPLICATION INFORMATION (continued)

Fig. 18 – Unity-gain absolute-value circuit

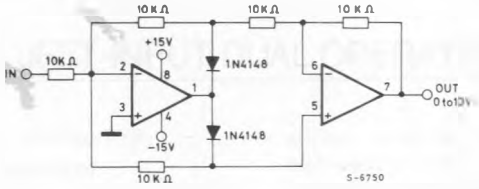


Fig. 19 – Single supply sample and hold

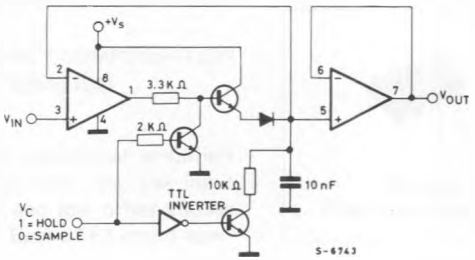
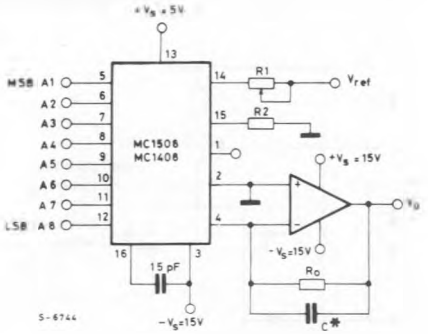


Fig. 20 – Output current to voltage transformation for a DA converter



(*) The value of C may be selected to minimize overshoot and ringing (C ≈ 68 pF).

Settling time to within 1/2 LSB (± 19.5 mV) is approximately 4.0 μs from the time all bits are switched.

Theoretical V_o :

$$V_o = \frac{V_{ref}}{R1}(R_o)\left[\frac{A1}{2} + \frac{A2}{4} + \frac{A3}{8} + \frac{A4}{16} + \frac{A5}{32} + \frac{A6}{64} + \frac{A7}{128} + \frac{A8}{256}\right]$$

Adjust V_{ref}, R1 or R_o so that V_o with all digital inputs at high level is equal to 9.961 volts.

$V_{ref} = 2.0\ V_{dc}$
$R1 = R2 \approx 1.0\ k\Omega$
$R_o = 5.0\ k\Omega$

$$V_o = \frac{2\ V}{1\ k}(5\ k)\left[\frac{1}{2} + \frac{1}{4} + \frac{1}{8} + \frac{1}{16} + \frac{1}{32} + \frac{1}{64} + \frac{1}{128} + \frac{1}{256}\right]$$

$$= 10V\left[\frac{255}{256}\right] = 9.961V$$