Wideband Operational Amplifier

FEATURES

- **Wide Bandwidth: 3 GHz**
- **High Slew Rate: 830 V/µs**
- **Low Voltage Noise: 2.4 nV/√Hz**
- **Single Supply: 5 V, 3 V**
- **Quiescent Current: 18 mA**

APPLICATIONS

- **Active Filter**
- **ADC Driver**
- **Ultrasound**
- **Gamma Camera**
- **RF/Telecom**

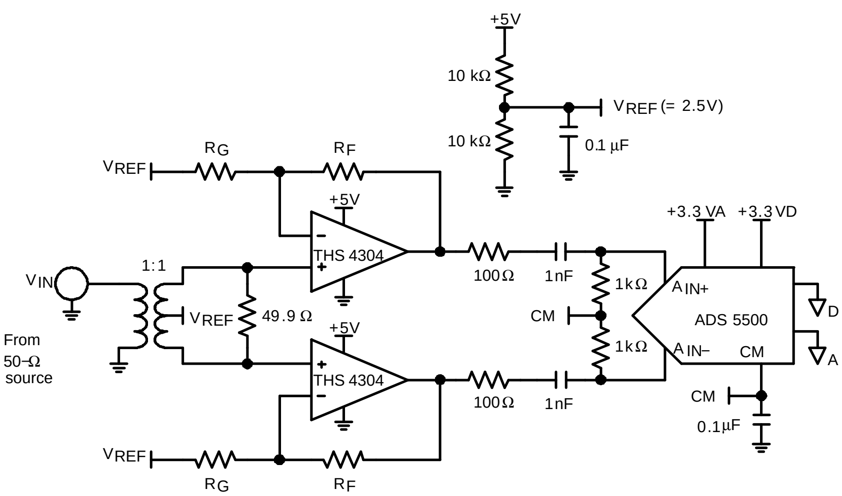
DESCRIPTION

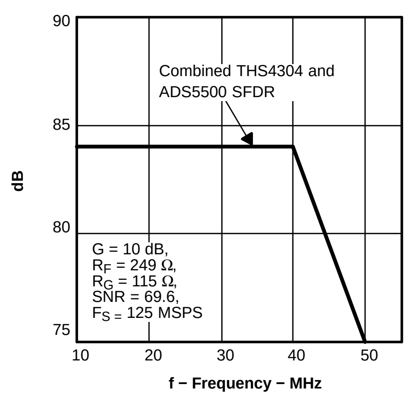
The THS4304 is a wideband, voltage-feedback operational amplifier designed for use in high-speed analog signal-processing chains operating with a single 5-V power supply. Developed in the BiCom3 silicon germanium process technology, the THS4304 offers best-in-class performance using a single 5-V supply as opposed to previous generations of operational amplifiers requiring ±5-V supplies.

The THS4304 is a traditional voltage-feedback topology that provides the following benefits: balanced inputs, low offset voltage and offset current, low offset drift, high common mode and power supply rejection ratio.

The THS4304 is offered in 8-pin MSOP package (DGK), the 8-pin SOIC package (D), and the space-saving 5-pin SOT-23 package (DBV).

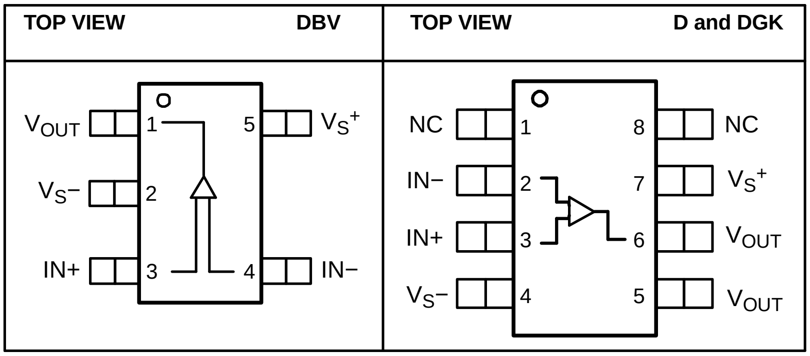
DIFFERENTIAL ADC DRIVE





These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

PINOUT DRAWING



NOTE: NC indicates there is no internal connection to these pins.

PACKAGING / ORDERING INFORMATION

PACKAGED DEVICES	PACKAGE TYPE	PACKAGE MARKINGS	TRANSPORT MEDIA, QUANTITY
THS4304DBVT	SOT-23-5	AKW	Tape and Reel, 250
THS4304DBVR			Tape and Reel, 3000
THS4304D	SOIC-8	—	Rails, 75
THS4304DR			Tape and Reel, 2500
THS4304DGK	MSOP-8	AKU	Rails, 100
THS4304DGKR			Tape and Reel, 2500

DISSIPATION RATINGS

PACKAGE	θ_{JC} (°C/W)	θ_{JA} (°C/W)(1)	POWER RATING(2)	
			$T_A \leq 25°C$	$T_A = 85°C$
DBV (5)	55	255.4	391 mW	156 mW
D (8)	38.3	97.5	1.02 W	410 mW
DGK (8)	71.5	180.8	553 mW	221 mW

(1) This data was taken using the JEDEC standard High-K test PCB.
(2) Power rating determined with a junction temperature of 125°C. This is the point where distortion starts to substantially increase. Thermal management of the final PCB should strive to keep the junction temperature at or below 125°C for best performance and long-term reliability.

ABSOLUTE MAXIMUM RATINGS[1]

over operating free-air temperature range (unless otherwise noted)

			UNIT
V_S	Supply voltage		+6.0 V
V_I	Input voltage		$\pm V_S$
I_O	Output current		150 mA
V_{ID}	Differential input voltage		±2 V
	Continuous power dissipation		See Dissipation Rating Table
T_J	Maximum junction temperature, any condition[2]		150°C
T_J	Operating free-air temperature range, continuous operation, long-term reliability[2]		125°C
T_{stg}	Storage temperature range		–65°C to 150°C
	Lead temperature: 1,6 mm (1/16 inch) from case for 10 seconds		300°C
	ESD Ratings	HBM	1600 V
	ESD Ratings	CDM	1000 V
	ESD Ratings	MM	100 V

(1) The absolute maximum ratings under any condition is limited by the constraints of the silicon process. Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.
(2) The maximum junction temperature for continuous operation is limited by package constraints. Operation above this temperature may result in reduced reliability and/or lifetime of the device.

RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
Supply voltage, (V_{S+} and V_{S-})	Dual supply	±1.35	±2.5	V
Supply voltage, (V_{S+} and V_{S-})	Single supply	2.7	5	V
Input common-mode voltage range		V_{S-} – 0.2	V_{S+} + 0.2	V

ELECTRICAL CHARACTERISTICS

Specifications: V_S = 5 V: R_F = 249 Ω, R_L = 100 Ω, and G = +2 unless otherwise noted

PARAMETER	CONDITIONS	TYP	OVER TEMPERATURE					TEST LEVEL (1)
		25°C	25°C	0°C to 70°C	–40°C to 85°C	UNITS	MIN/ MAX	
AC PERFORMANCE								
Small-Signal Bandwidth	G = +1, V_O = 100 mVpp	3				GHz	Typ	C
	G = +2, V_O = 100 mVpp	1				GHz	Typ	C
	G = +5, V_O = 100 mVpp	187				MHz	Typ	C
	G = +10, V_O = 100 mVpp	87				MHz	Typ	C
Gain Bandwidth Product	G >+10	870				MHz	Typ	C
0.1-dB Flat Bandwidth	G= +2, V_O = 100 mVpp, C_F = 0.5 pF	300				MHz	Typ	C
Large-Signal Bandwidth	G = +2, V_O = 2 V_{PP}	240				MHz	Typ	C
Slew Rate	G = +2, V_O = 1-V Step	830				V/µs	Typ	C
	G = +2, V_O = 2-V Step	790				V/µs	Typ	C
Settling Time to 1%	G = –2, V_O = 2-V Step	4.5				ns	Typ	C
Settling Time to 0.1%	G = –2, V_O = 2-V Step	7.5				ns	Typ	C
Settling Time to 0.01%	G = –2, V_O = 2-V Step	35				ns	Typ	C
Rise / Fall Times	G = +2, V_O = 2-V Step	2.5				ns	Typ	C
Harmonic Distortion								
Second Harmonic Distortion	G = +2, V_O = 2 V_{PP}, f = 10 MHz; R_L= 100 Ω	–84				dBc	Typ	C
	R_L = 1 kΩ	–95				dBc	Typ	C
Third Harmonic Distortion	R_L = 100 Ω	–100				dBc	Typ	C
	R_L = 1 kΩ	–100				dBc	Typ	C
Third-Order Intermodulation Distortion (IMD_3)	G = +2, V_O= 2-V_{PP} envelope, 200-kHz tone spacing, f = 20 MHz	–84				dBc	Typ	C
Third-Order Output Intercept (OIP_3)		48				dBm	Typ	C
Noise Figure	G = +2, f = 1 GHz	15				dB	Typ	C
Input Voltage Noise	f = 1 MHz	2.4				nV/√Hz	Typ	C
Input Current Noise	f = 1 MHz	2.1				pA/√Hz	Typ	C
DC PERFORMANCE								
Open-Loop Voltage Gain (A_{OL})	V_O = ± 0.8 V, V_{CM} = 2.5 V	65	54	50	50	dB	Min	A
Input Offset Voltage	V_{CM} = 2.5 V	0.5	4	5	5	mV	Max	A
Input Offset Voltage Drift				5	5	µV/°C	Typ	B
Input Bias Current		7	12	18	18	µA	Max	A
Input Bias Current Drift				50	50	nA/°C	Typ	B
Input Offset Current		0.5	1	1.2	1.2	µA	Max	A
Input Offset Current Drift				10	10	nA/°C	Typ	B
INPUT CHARACTERISTICS								
Common-Mode Input Range		–0.2 to 5.2	0.2 to 4.8	0.4 to 4.6	0.4 to 4.6	V	Min	A
Common-Mode Rejection Ratio	V_O = ± 0.2 V, V_{CM} = 2.5 V	95	80	73	73	dB	Min	A
Input Resistance	Each input, referenced to GND	100				kΩ	Typ	C
Input Capacitance		1.5				pF	Typ	C

(1) Test levels: (A) 100% tested at 25°C. Over temperature limits by characterization and simulation. (B) Limits set by characterization and simulation. (C) Typical value only for information.

ELECTRICAL CHARACTERISTICS (continued)

Specifications: V_S = 5 V: R_F = 249 Ω, R_L = 100 Ω, and G = +2 unless otherwise noted

PARAMETER	CONDITIONS	TYP	OVER TEMPERATURE					TEST LEVEL(1)
		25°C	25°C	0°C to 70°C	–40°C to 85°C	UNITS	MIN/ MAX	
OUTPUT CHARACTERISTICS								
Output Voltage Swing	R_L = 100 Ω	1.1 to 3.9	1.2 to 3.8	1.3 to 3.7	1.3 to 3.7	V	Min	A
	R_L = 1 kΩ	1 to 4	1.1 to 3.9	1.2 to 3.8	1.2 to 3.8			
Output Current (Sourcing)	R_L = 10 Ω	140	100	57	57	mA	Min	A
Output Current (Sinking)	R_L = 10 Ω	92	65	40	40	mA	Min	A
Output Impedance	f = 100 kHz	0.016				Ω	Typ	A
POWER SUPPLY								
Maximum Operating Voltage		5	5.5	5.5	5.5	V	Max	A
Minimum Operating Voltage		5	2.7	2.7	2.7		Min	
Maximum Quiescent Current		18	18.9	19.4	19.4	mA	Max	A
Minimum Quiescent Current		18	17.5	16.6	16.6	mA	Min	A
Power Supply Rejection (+PSRR)	V_{S+} = 5.5 V to 4.5 V, V_{S-} = 0 V	80	73	66	66	dB	Min	A
Power Supply Rejection (-PSRR)	V_{S+} = 5 V, V_{S-} = –0.5 V to +0.5 V	60	57	54	54	dB	Min	A

ELECTRICAL CHARACTERISTICS

Specifications: V_S = 3 V: R_F = 249 Ω, R_L = 499 Ω, and G = +2 unless otherwise noted

PARAMETER	CONDITIONS	TYP	OVER TEMPERATURE					TEST LEVEL(1)
		25°C	25°C	0°C to 70°C	–40°C to 85°C	UNITS	MIN/ MAX	
AC PERFORMANCE								
Small-Signal Bandwidth	G = +1, V_O = 100 mVpp	3				GHz	Typ	C
	G = +2, V_O = 100 mVpp	900				MHz	Typ	C
	G = +5, V_O = 100 mVpp	190				MHz	Typ	C
	G = +10, V_O = 100 mVpp	83				MHz	Typ	C
Gain Bandwidth Product	G >+10	830				MHz	Typ	C
Large-Signal Bandwidth	G = +2, V_O = 1 V_{PP}	450				MHz	Typ	C
Slew Rate	G = +2, V_O = 1-V Step	750				V/μs	Typ	C
	G = +2, V_O = 1-V Step	675				V/μs	Typ	C
Settling Time to 1%	G = –2, V_O = 0.5-V Step	4.5				ns	Typ	C
Settling Time to 0.1%	G = –2, V_O = 0.5-V Step	20				ns	Typ	C
Rise / Fall Times	G = +2, V_O = 0.5-V Step	1.5				ns	Typ	C
Harmonic Distortion								
Second Harmonic Distortion	G = +2, V_O = 0.5 V_{PP}, f = 10 MHz; R_L = 499 Ω	–92				dBc	Typ	C
Third Harmonic Distortion		–91				dBc	Typ	C
Noise Figure	G = +2, f = 1 GHz	15				dB	Typ	C
Input Voltage Noise	f = 1 MHz	2.4				nV/√Hz	Typ	C
Input Current Noise	f = 1 MHz	2.1				pA/√Hz	Typ	C
DC PERFORMANCE								
Open-Loop Voltage Gain (A_{OL})	V_O = ± 0.5 V, V_{CM} = 1.5 V	49	44			dB	Min	A
Input Offset Voltage	V_{CM} = 1.5 V	2	4	5	5	mV	Max	A
Input Offset Voltage Drift				5	5	μV/°C	Typ	B
Input Bias Current		7	12	18	18	μA	Max	A
Input Bias Current Drift				50	50	nA/°C	Typ	B
Input Offset Current		0.4	1	1.2	1.2	μA	Max	A
Input Offset Current Drift				10	10	nA/°C	Typ	B
INPUT CHARACTERISTICS								
Common-Mode Input Range		–0.2 to 3.2	0.2 to 2.8	0.4 to 2.6	0.4 to 2.6	V	Min	A
Common-Mode Rejection Ratio	V_O = ± 0.09 V, V_{CM} = 1.5 V	92	80	70	70	dB	Min	A
Input Resistance	Each input, referenced to GND	100				kΩ	Typ	C
Input Capacitance		1.5				pF	Typ	C

(1) Test levels: (A) 100% tested at 25°C. Over temperature limits by characterization and simulation. (B) Limits set by characterization and simulation. (C) Typical value only for information.

ELECTRICAL CHARACTERISTICS (continued)

Specifications: V_S = 3 V: R_F = 249 Ω, R_L = 499 Ω, and G = +2 unless otherwise noted

PARAMETER	CONDITIONS	TYP	OVER TEMPERATURE					TEST LEVEL(1)
		25°C	25°C	0°C to 70°C	–40°C to 85°C	UNITS	MIN/ MAX	
OUTPUT CHARACTERISTIC								
Output Voltage Swing	R_L = 100 Ω	1.1 to 1.9	1.2 to 1.8	1.3 to 1.7	1.3 to 1.7	V	Min	A
	R_L = 1 kΩ	1 to 2	1.1 to 1.9	1.2 to 1.8	1.2 to 1.8			
Output Current (Sourcing)	R_L = 10 Ω	57	50	40	40	mA	Min	A
Output Current (Sinking)	R_L = 10 Ω	57	45	35	35	mA	Min	A
Output Impedance	f = 100 kHz	0.016				Ω	Typ	A
POWER SUPPLY								
Maximum Operating Voltage		3	5.5	5.5	5.5	V	Max	A
Minimum Operating Voltage		3	2.7	2.7	2.7		Min	
Maximum Quiescent Current		17.2	17.9	18.4	18.4	mA	Max	A
Minimum Quiescent Current		17.2	16.5	15.6	15.6	mA	Min	A
Power Supply Rejection (+PSRR)	V_{S+} = 3.3 V to 2.7 V, V_{S-} = 0 V	80	60	54	54	dB	Min	A
Power Supply Rejection (-PSRR)	V_{S+} = 5 V, V_{S-} = –0.5 V to +0.5 V	60	55	52	52	dB	Min	A

TYPICAL CHARACTERISTICS

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3 V			
	Frequency response		32–35
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	Harmonic Distortion	vs Output voltage	38
SR	Slew rate	vs Output voltage	39
V_O	Settling time		40
V_O	Output voltage	vs Load resistance	41
I_{IB}	Input bias and offset current	vs Case temperature	42
V_{OS}	Input offset voltage	vs Case temperature	43
V_O	Large-signal transient response		44
V_O	Overdrive recovery time		45
Z_O	Output impedance	vs Frequency	46

TYPICAL CHARACTERISTICS (5 V)

FREQUENCY RESPONSE

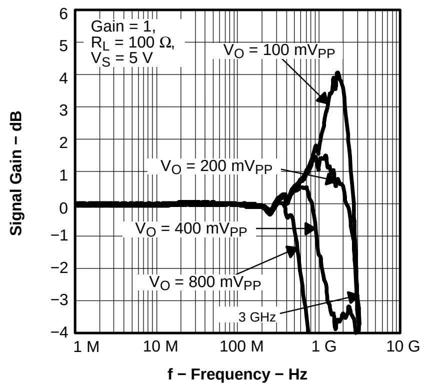

Figure 1.

FREQUENCY RESPONSE

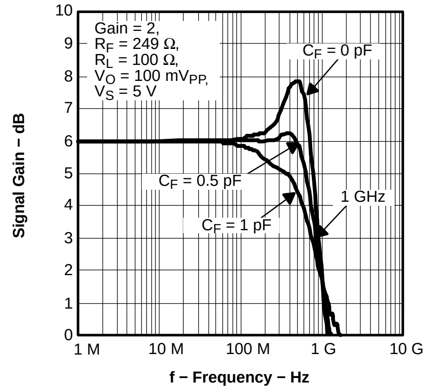

Figure 2.

FREQUENCY RESPONSE

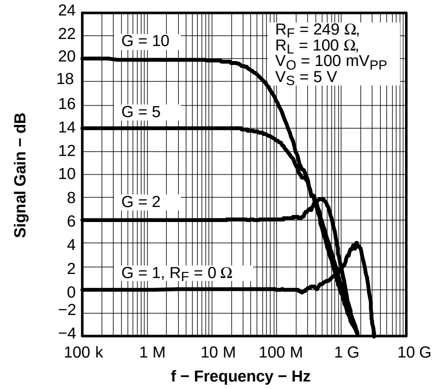

Figure 3.

0.1-dB FLATNESS

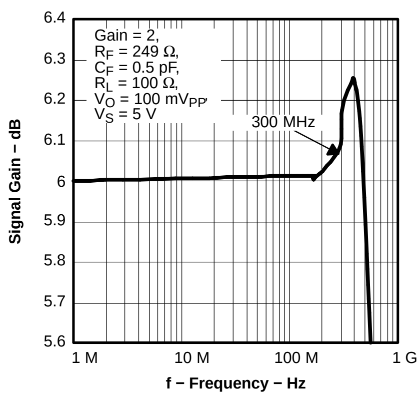

Figure 4.

FREQUENCY RESPONSE

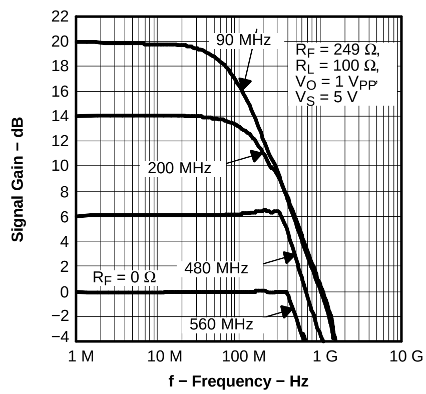

Figure 5.

FREQUENCY RESPONSE

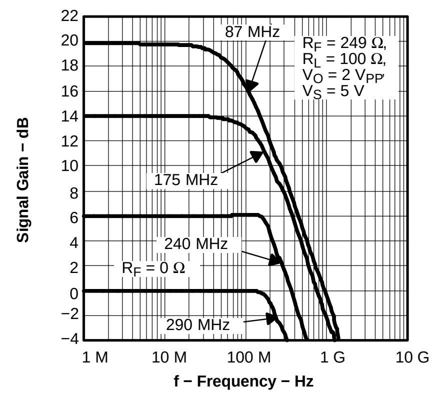

Figure 6.

FREQUENCY RESPONSE BY PACKAGE

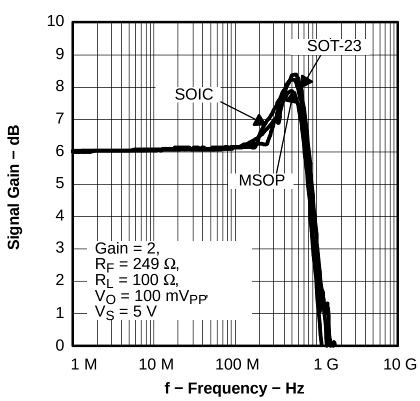

Figure 7.

S-PARAMETERS vs FREQUENCY

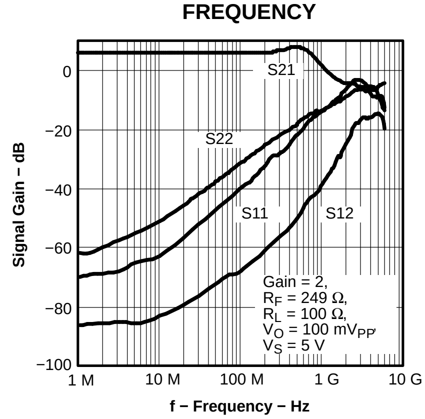

Figure 8.

2ND HARMONIC DISTORTION vs FREQUENCY

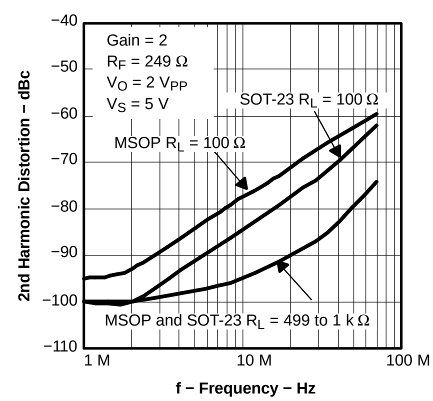

Figure 9.

TYPICAL CHARACTERISTICS (5 V) (continued)

3RD HARMONIC DISTORTION vs FREQUENCY

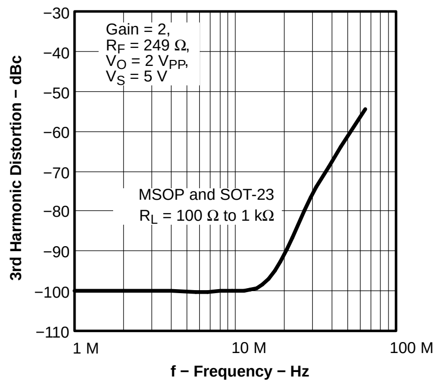

Figure 10.

2ND HARMONIC DISTORTION vs FREQUENCY

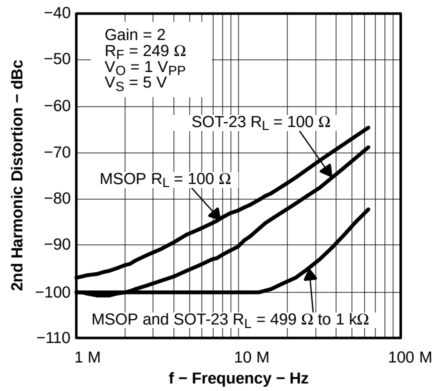

Figure 11.

3RD HARMONIC DISTORTION vs FREQUENCY

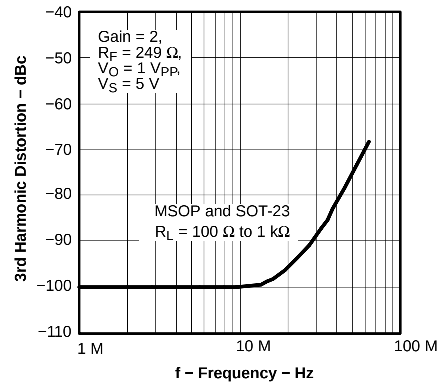

Figure 12.

2ND HARMONIC DISTORTION vs OUTPUT VOLTAGE

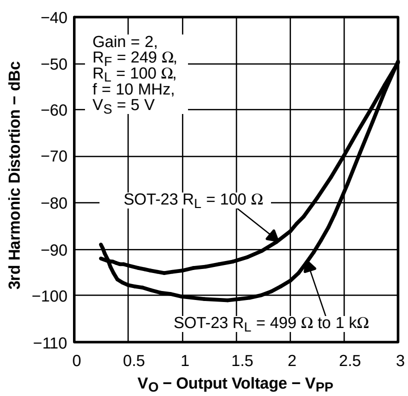

Figure 13.

3RD HARMONIC DISTORTION vs OUTPUT VOLTAGE

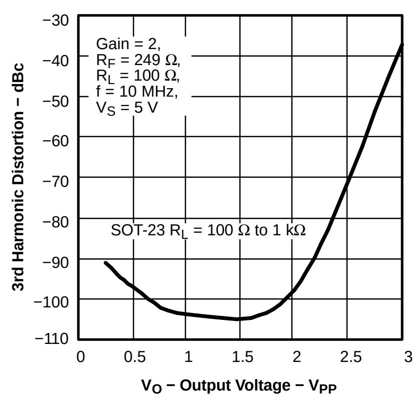

Figure 14.

3RD ORDER INTERMODULATION DISTORTION vs FREQUENCY

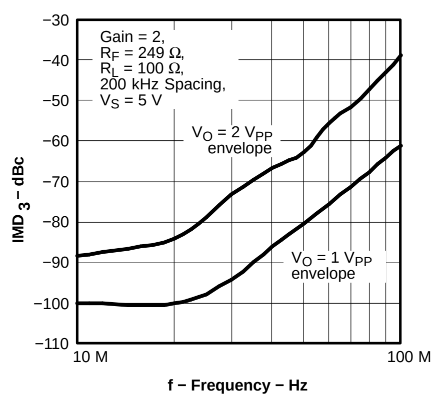

Figure 15.

3RD ORDER OUTPUT INTERCEPT POINT vs FREQUENCY

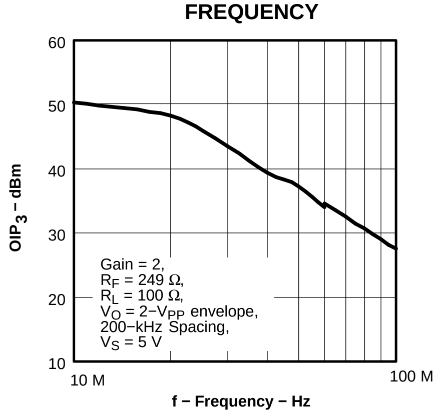

Figure 16.

SLEW RATE vs OUTPUT VOLTAGE

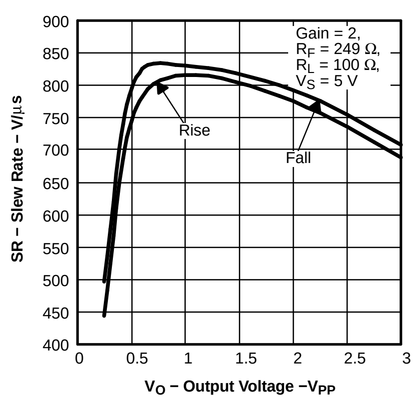

Figure 17.

NOISE vs FREQUENCY

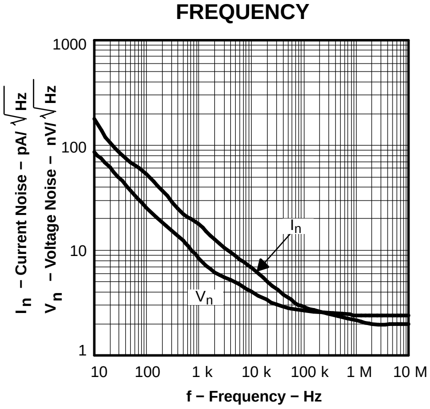

Figure 18.

TYPICAL CHARACTERISTICS (5 V) (continued)

NOISE FIGURE vs FREQUENCY

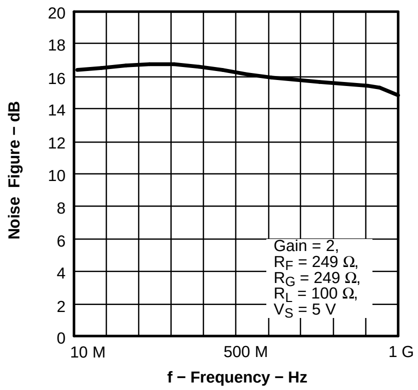

Figure 19.

QUIESCENT CURRENT vs SUPPLY VOLTAGE

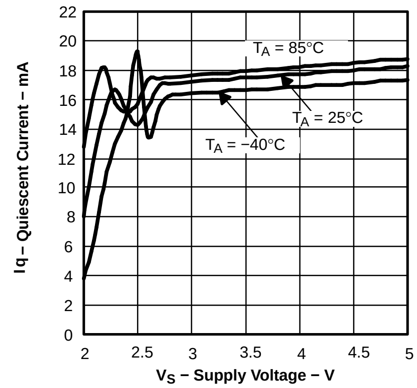

Figure 20.

REJECTION RATIO vs FREQUENCY

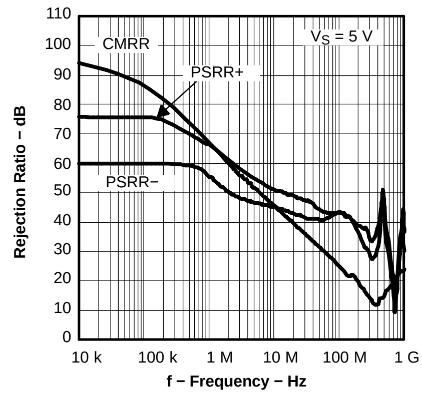

Figure 21.

OUTPUT VOLTAGE vs LOAD RESISTANCE

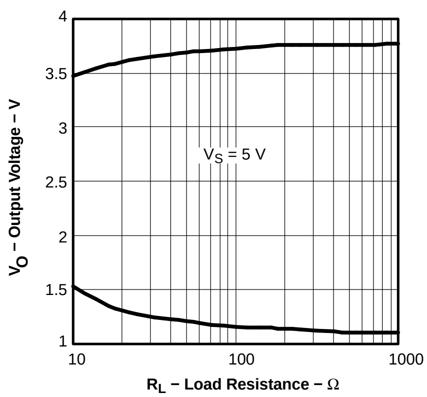

Figure 22.

INPUT OFFSET VOLTAGE vs INPUT COMMON-MODE VOLTAGE

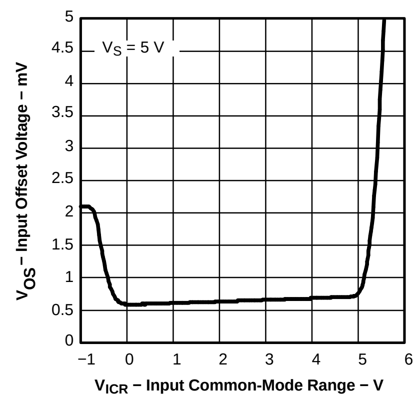

Figure 23.

INPUT BIAS AND OFFSET CURRENT vs CASE TEMPERATURE

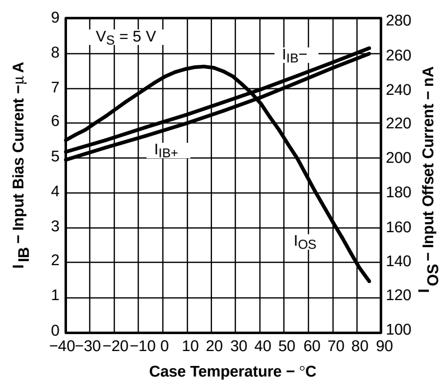

Figure 24.

INPUT OFFSET VOLTAGE vs CASE TEMPERATURE

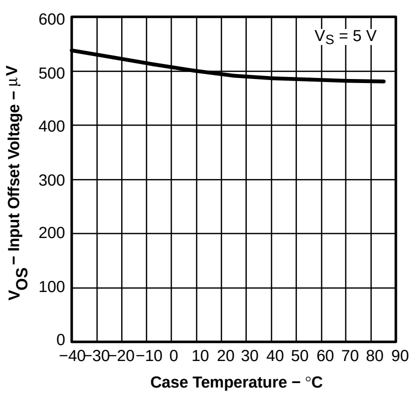

Figure 25.

OPEN-LOOP GAIN vs FREQUENCY

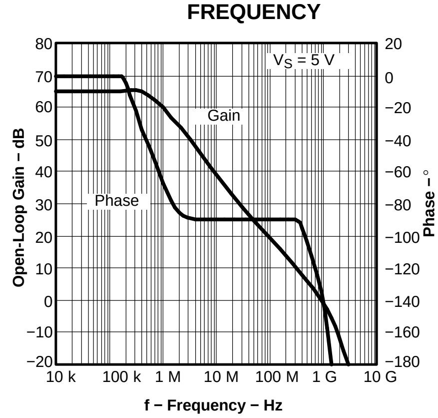

Figure 26.

SMALL-SIGNAL TRANSIENT RESPONSE

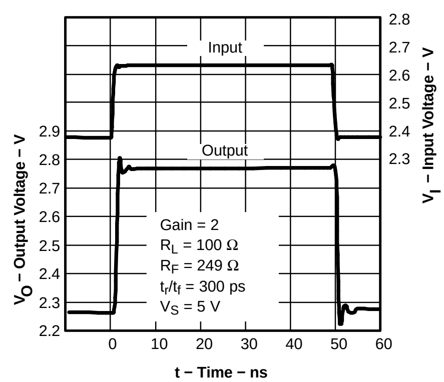

Figure 27.

TYPICAL CHARACTERISTICS (5 V) (continued)

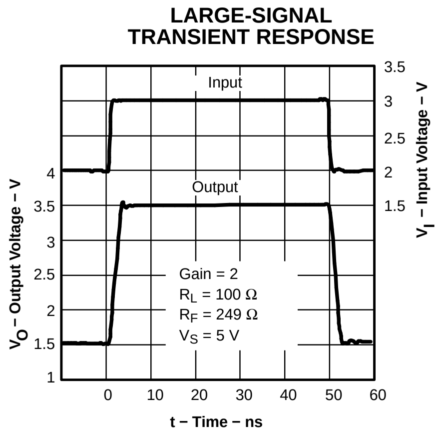

Figure 28.

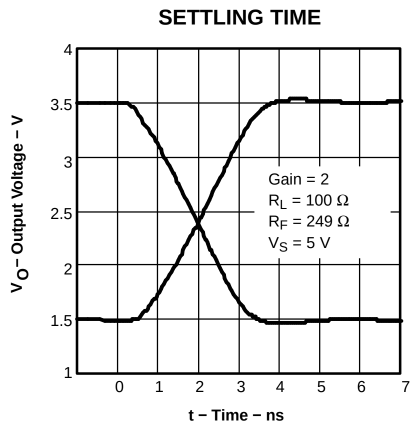

Figure 29.

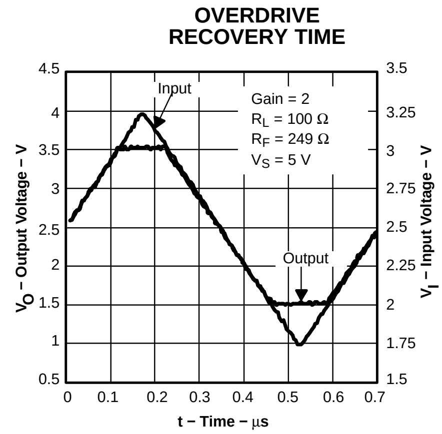

Figure 30.

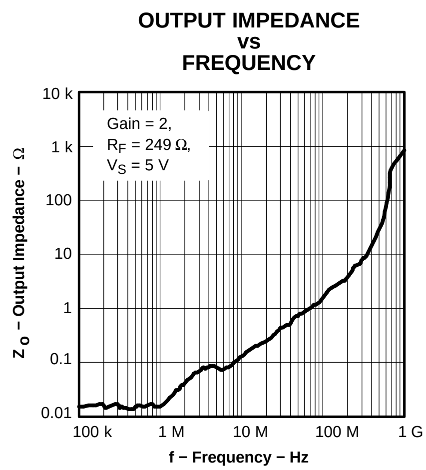

Figure 31.

TYPICAL CHARACTERISTICS (3 V)

FREQUENCY RESPONSE

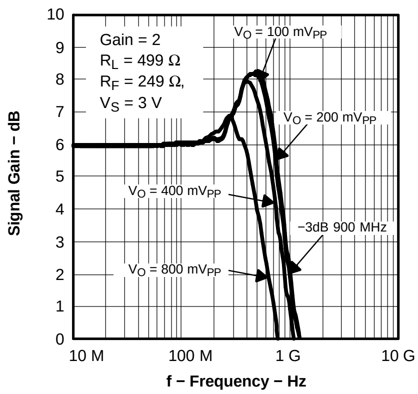

Figure 32.

FREQUENCY RESPONSE

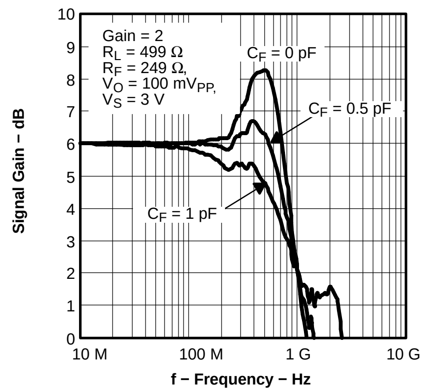

Figure 33.

FREQUENCY RESPONSE

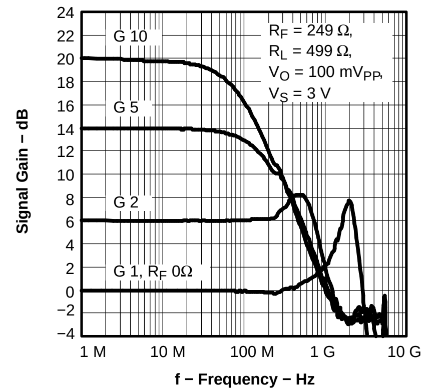

Figure 34.

FREQUENCY RESPONSE

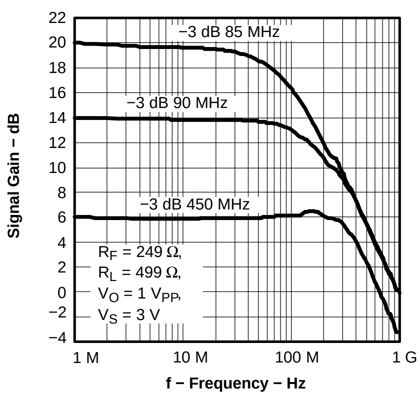

Figure 35.

2ND HARMONIC DISTORTION vs FREQUENCY

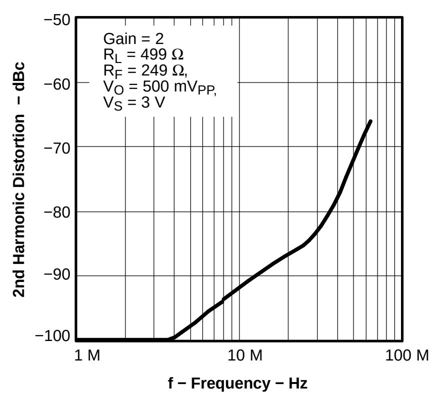

Figure 36.

3RD HARMONIC DISTORTION vs FREQUENCY

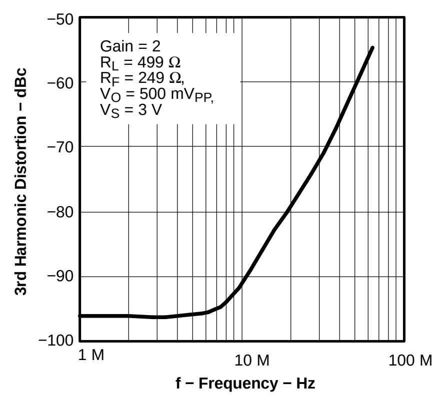

Figure 37.

HARMONIC DISTORTION vs OUTPUT VOLTAGE

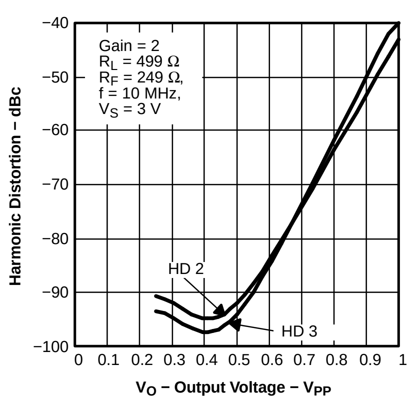

Figure 38.

SLEW RATE vs OUTPUT VOLTAGE

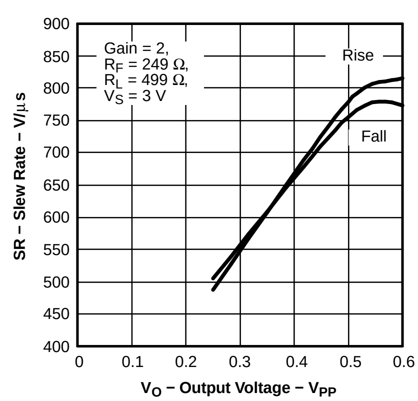

Figure 39.

SETTLING TIME

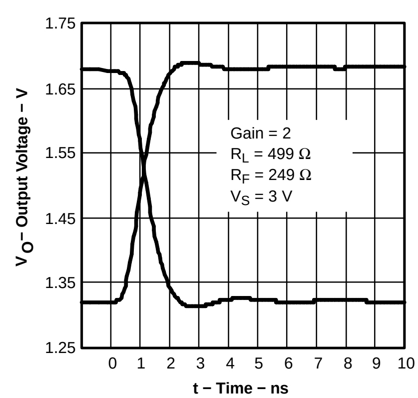

Figure 40.

TYPICAL CHARACTERISTICS (3 V) (continued)

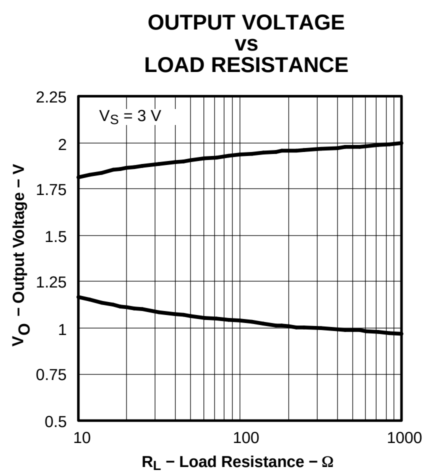

Figure 41.

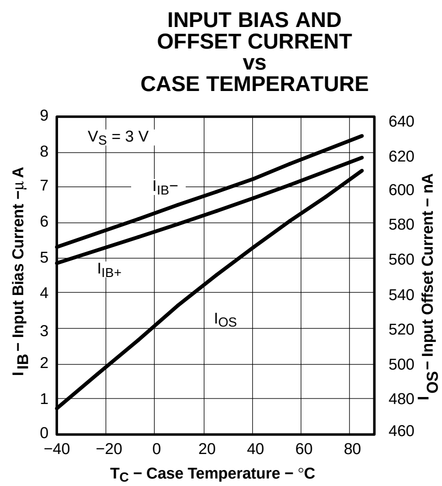

Figure 42.

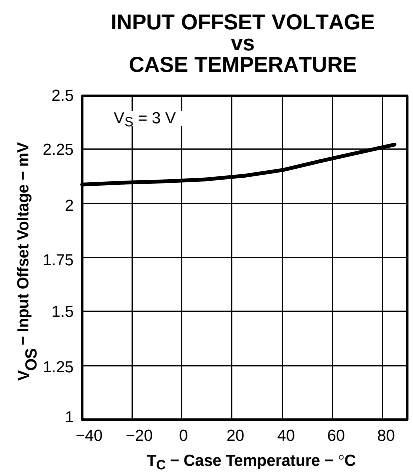

Figure 43.

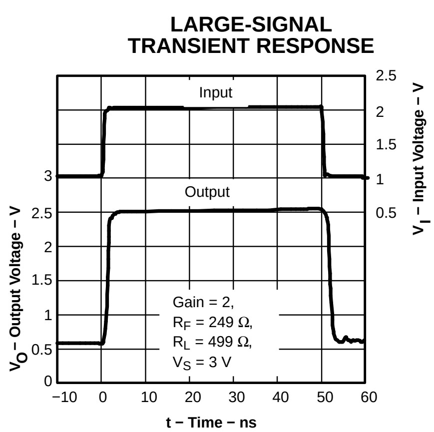

Figure 44.

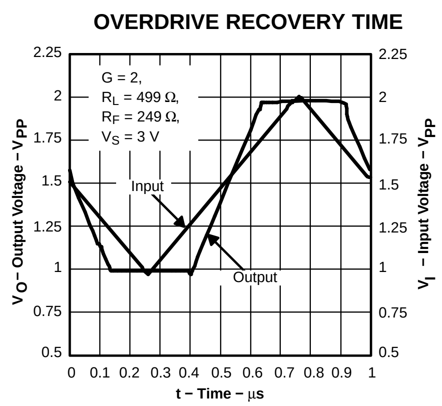

Figure 45.

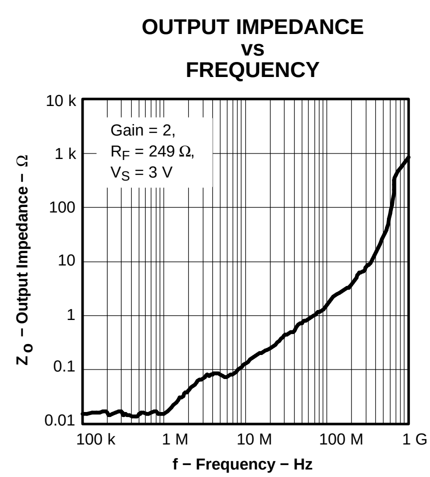

Figure 46.

APPLICATION INFORMATION

For many years, high-performance analog design has required the generation of split power supply voltages, like ±15 V, ±8 V, and more recently ±5 V, in order to realize the full performance of the amplifiers available. Modern trends in high-performance analog are moving towards single-supply operation at 5 V, 3 V, and lower. This reduces power supply cost due to less voltages being generated and conserves energy in low power applications. It can also take a toll on available dynamic range, a valuable commodity in analog design, if the available voltage swing of the signal must also be reduced.

Two key figures of merit for dynamic range are signal-to-noise ratio (SNR) and spurious free dynamic range (SFDR).

SNR is simply the signal level divided by the noise:

$$\text{SNR} = \frac{\text{Signal}}{\text{Noise}}$$

and SFDR is the signal level divided by the highest spur:

$$\text{SFDR} = \frac{\text{Signal}}{\text{Spur}}$$

In an operational amplifier, reduced supply voltage typically results in reduced signal levels due to lower voltage available to operate the transistors within the amplifier. When noise and distortion remain constant, the result is a commensurate reduction in SNR and SFDR. To regain dynamic range, the process and the architecture used to make the operational amplifier must have superior noise and distortion performance with lower power supply overhead required for proper transistor operation.

The THS4304 BiCom3 operational amplifier is just such a device. It is able to provide 2-Vpp signal swing at its output on a single 5-V supply with noise and distortion performance similar to the best 10-V operational amplifiers on the market today

GENERAL APPLICATION

The THS4304 is a traditional voltage-feedback topology with wideband performance up to 3 GHz at unity gain. Care must be taken to ensure that parasitic elements do not erode the phase margin.

Capacitance at the output and inverting input, and resistance and inductance in the feedback path, can cause problems.

To reduce parasitic capacitance, the ground plane should be removed from under the part.

To reduce inductance in the feedback, the circuit traces should be kept as short and direct as possible. For best performance in non-inverting unity gain (G=+1V/V), it is recommended to use a wide trace directly between the output and inverting input.

For a gain of +2V/V, it is recommended to use a 249-Ω feedback resistor. With good layout, this should keep the frequency response peaking to around 2 dB. This resistance is high enough to not load the output excessively, and the part is capable of driving 100-Ω load with good performance. Higher-value resistors can be used, with more peaking. For example, 499 Ω gives about 5 dB of peaking, and gives slightly better distortion performance with 100-Ω load. Lower value feedback resistors can also be used to reduce peaking, but degrades the distortion performance with heavy loads.

Power supply bypass capacitors are required for proper operation. The most critical are 0.1-µF ceramic capacitors; these should be placed as close to the part as possible. Larger bulk capacitors can be shared with other components in the same area as the operational amplifier.

HARMONIC DISTORTION

For best second harmonic (HD2), it is important to use a single-point ground between the power supply bypass capacitors when using a split supply. It is also recommended to use a single ground or reference point for input termination and gain-setting resistors (R8 and R11 in the non-inverting circuit). It is recommended to follow the EVM layout closely in your application.

APPLICATION INFORMATION (continued)

SOT-23 versus MSOP

With light loading of 500-Ω and higher resistance, the THS4304 shows HD2 that is not dependant of package. With heavy output loading of 100 Ω, the THS4304 in SOT-23 package shows about 6 dB better HD2 performance versus the MSOP package.

EVALUATION MODULES

The THS4304 has two evaluation modules (EVMs) available. One is for the MSOP (DGK) package and the other for the SOT-23 (DBV) package. These provide a convenient platform for evaluating the performance of the part and building various different circuits. The full schematics, board layout, and bill of materials (as supplied) for the boards are shown in the following illustrations.

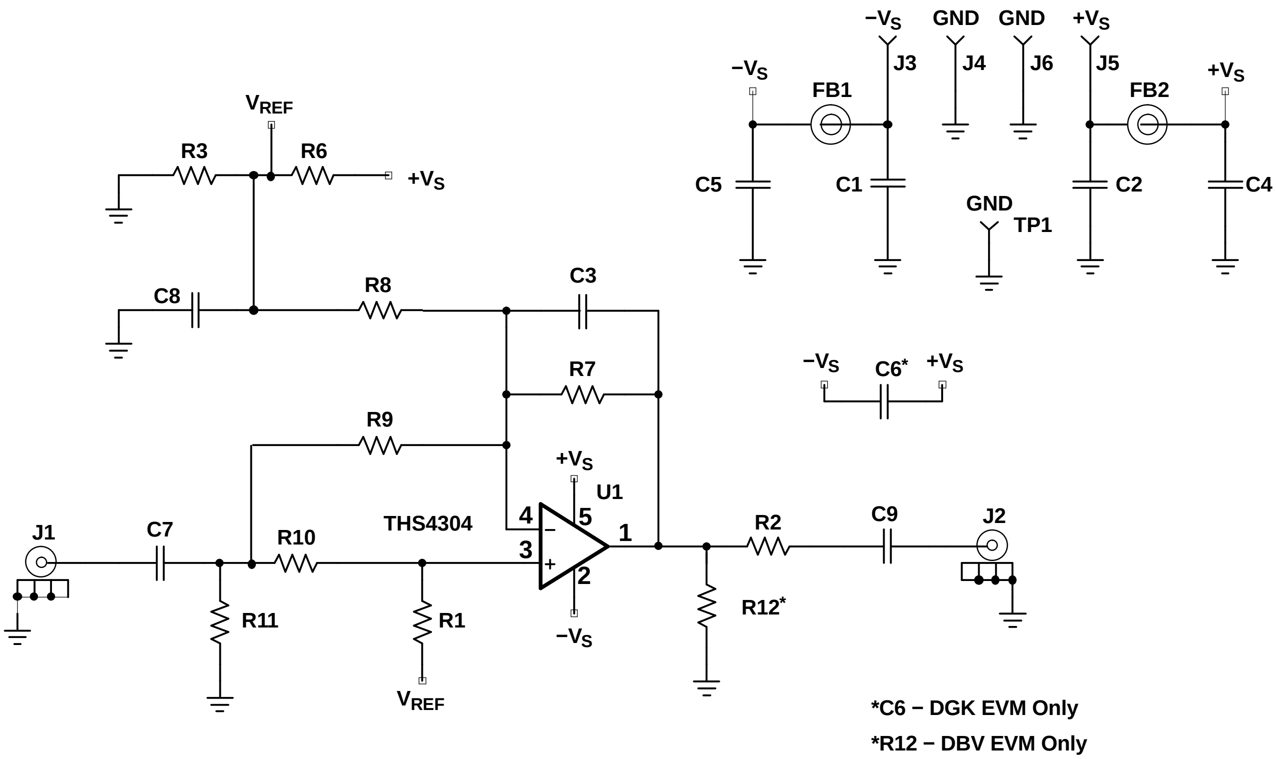

Figure 47. EVM Full Schematic

APPLICATION INFORMATION (continued)

EVM BILL OF MATERIALS

THS4304 EVM(1)						
Item	**Description**	**SMD Size**	**Reference Designator**	**PCB Quantity**	**Manufacturer's Part Number**	**Distributor's Part Number**
1	Bead, ferrite, 3-A, 80-Ω	1206	FB1, FB2	2	(STEWARD) HI1206N800R-00	(DIGI-KEY) 240-1010-1-ND
2	Capacitor, 3.3-µF, Ceramic	1206	C1, C2	2	(AVX) 1206YG335ZAT2A	(GARRETT) 1206YG335ZAT2A
3	Capacitor, 0.1-µF, Ceramic	0603	C4, C5	2	(AVX) 0603YC104KAT2A	(GARRETT) 0603YC104KAT2A
4	Open	0603	C3, C6(2)	2		
5	Open	0603	R1, R3, R6, R9, R12(3)	5		
6	Resistor, 0-Ω, 1/10-W, 1%	0603	C7. C8, C9, C10	4	(KOA) RK73Z1JTTD	(GARRETT) RK73Z1JTTD
7	Resistor, 49.9-Ω, 1/10-W, 1%	0603	R2, R11	2	(KOA) RK73H1JLTD49R9F	(GARRETT) RK73H1JLTD49R9F
8	Resistor, 249-Ω, 1/10-W, 1%	0603	R7, R8	2	(KOA) RK73H1JLTD2490F	(GARRETT) RK73H1JLTD2490F
9	Jack, banana recepticle, 0.25-in. diameter hole		J3, J4, J5, J6	4	(HH SMITH) 101	(NEWARK) 35F865
10	Test point, black		TP1	1	(KEYSTONE) 5001	(DIGI-KEY) 5001K-ND
11	Connector, edge, SMA PCB jack		J1, J2	2	(JOHNSON) 142-0701-801	(NEWARK) 90F2624
12	Integrated Circuit, THS4304		U1	1	(TI) THS4304DGK, or (TI) THS4304DBV	
13	Standoff, 4-40 HEX, 0.625-in. Length			4	(KEYSTONE) 1808	NEWARK) 89F1934
14	Screw, Phillips, 4-40, 0.250-in.			4	SHR-0440-016-SN	
15	Board, printed-circuit			1	(TI) THS4304DGK ENG A, or (TI) THS4304DBV ENG A	

(1) NOTE: All items are designated for both the DBV and DGK EVMs unless otherwise noted.
(2) C6 used on DGK EVM only.
(3) R12 used on DBV EVM only.

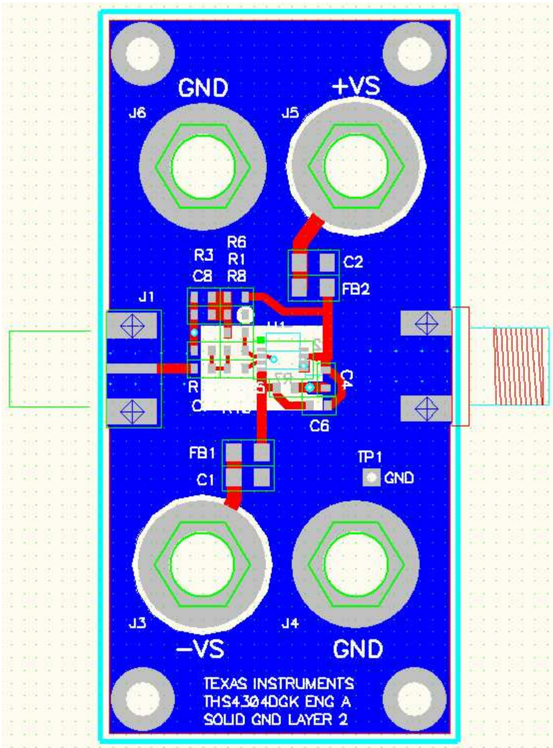

Figure 48. THS4304DGK EVM Layout Top and L2

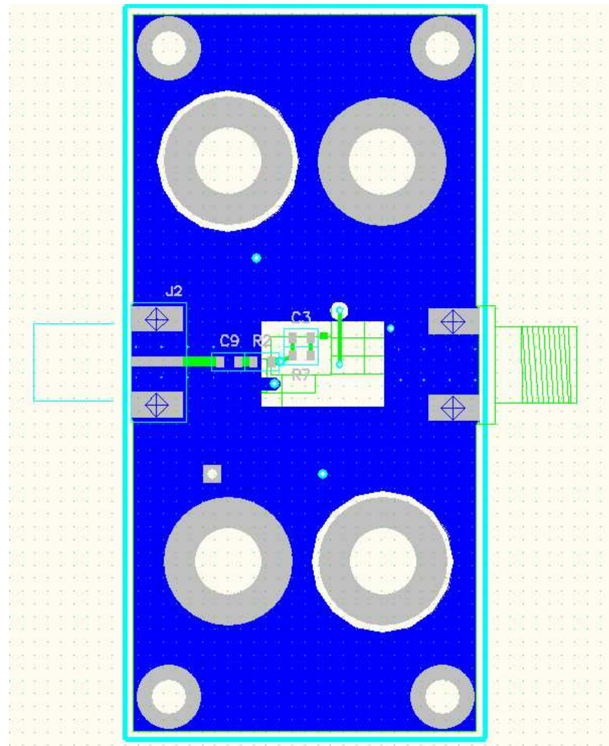

Figure 49. THS4304DGK EVM Layout Bottom and L3

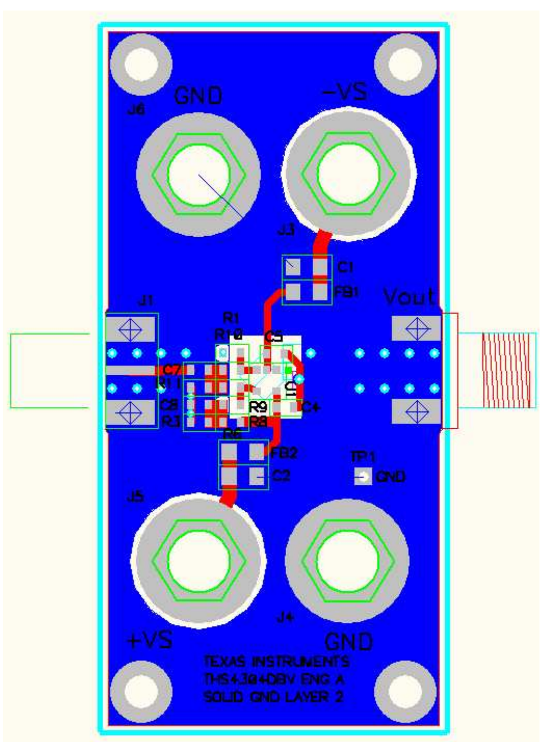

Figure 50. THS4304DBV EVM Layout Top and L2

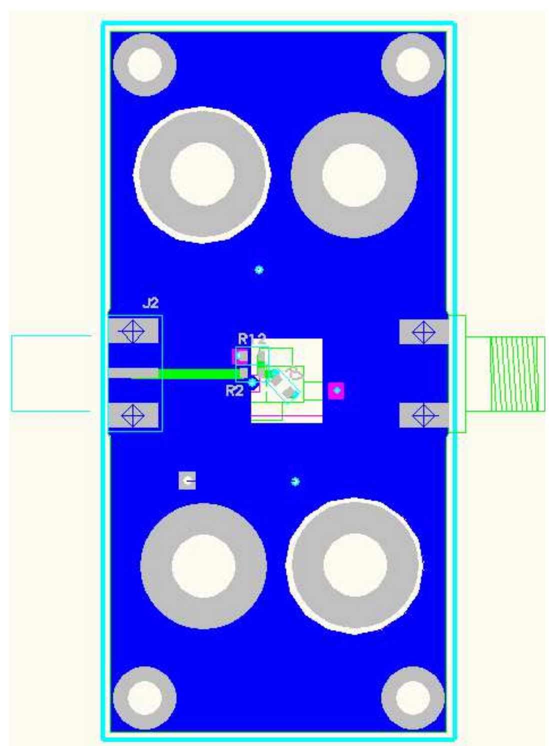

Figure 51. THS4304DBV EVM Layout Bottom and L3

NON-INVERTING GAIN WITH SPLIT SUPPLY

The following schematic shows how to configure the operational amplifier for non-inverting gain with split power supply (± 2.5V). This is how the EVM is supplied from TI. This configuration is convenient for test purposes because most signal generators and analyzer are designed to use ground-referenced signals by default. Note the input and output provides 50-Ω termination.

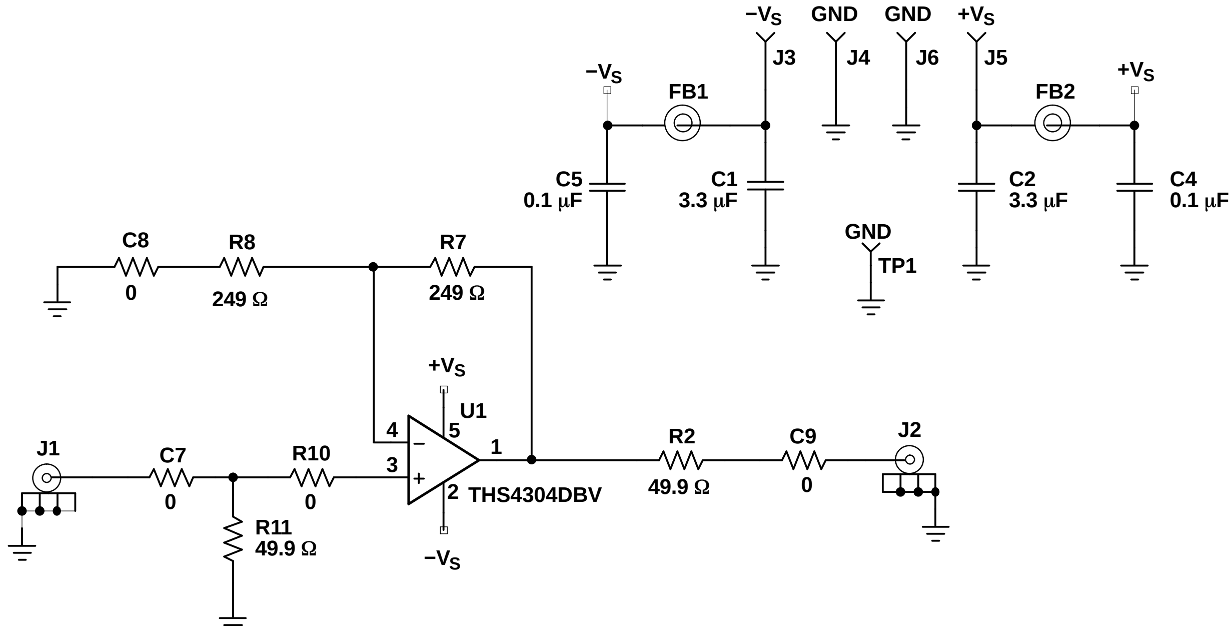

Figure 52. Non-Inverting Gain with Split Power Supply

INVERTING GAIN WITH SPLIT POWER SUPPLY

The following schematic shows how to configure the operational amplifier for inverting gain of 1 (–1 V/V) with split power supply (±2.5 V). Note the input and output provides 50-Ω termination for convenient interface to common test equipment.

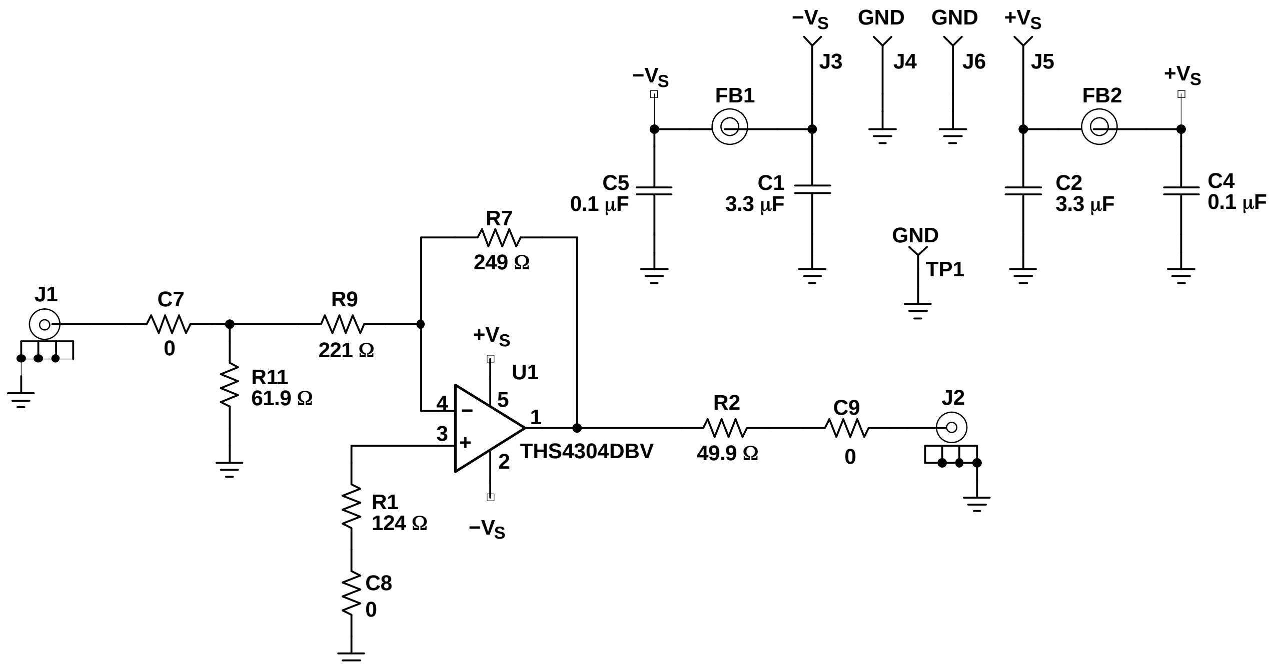

Figure 53. Inverting Gain with Split Power Supply

NON-INVERTING SINGLE-SUPPLY OPERATION

The THS4304 EVM can easily be configured for single 5-V supply operation, as shown in the following schematic, with no change in performance. This circuit passes dc signals at the input, so care must be taken to reference (or bias) the input signal to mid-supply.

If dc operation is not required, the amplifier can be ac coupled by inserting a capacitor in series with the input (C7) and output (C9).

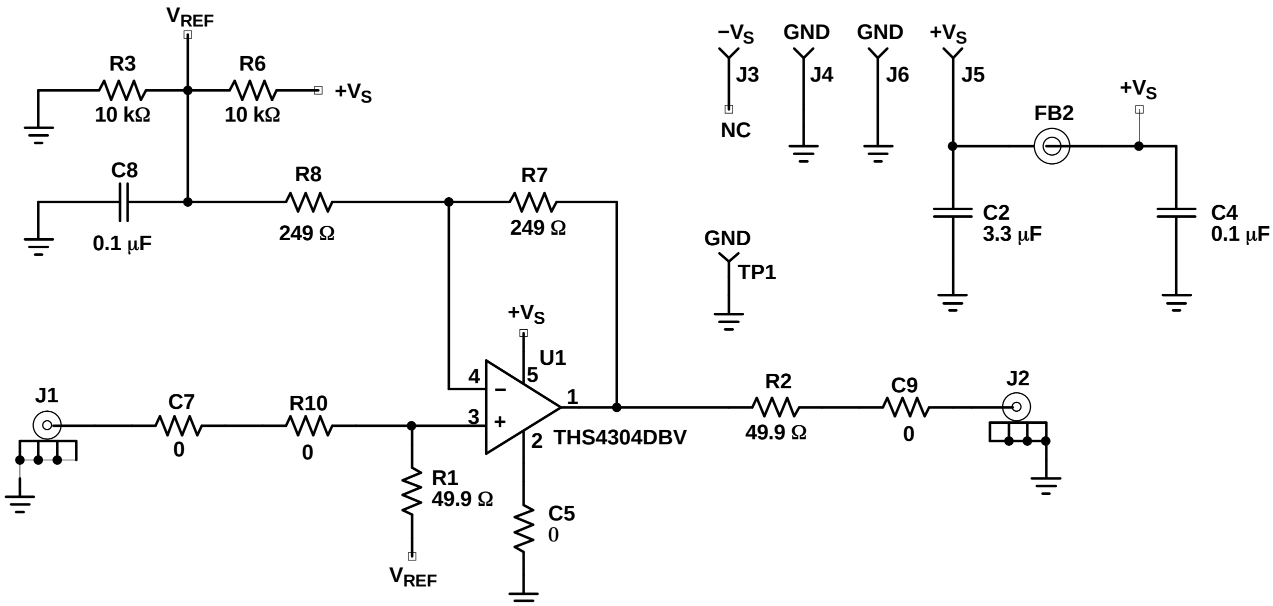

Figure 54. Non-Inverting 5-V Single-Supply Amplifier

DIFFERENTIAL ADC DRIVE AMPLIFIER

The circuit shown in Figure 54 is adapted as shown in Figure 55 to provide a high-performance differential amplifier drive circuit for use with high-performance ADCs, like the ADS5500 (14-bit 125-MSP ADC). For testing purposes, the circuit uses a transformer to convert the signal from a single-ended source to differential. If the input signal source in your application is differential and biased to mid-rail, no transformer is required.

The circuit employs two amplifiers to provide a differential signal path to the ADS5500. A resistor divider (two 10-kΩ resistors) is used to obtain a mid-supply reference voltage of 2.5 V (VREF) (the same as shown in the single-supply circuit of Figure 54). Applying this voltage to the one side of RG and to the positive input of the operational amplifier (via the center-tap of the transformer) sets the input and output common-mode voltage of the operational amplifiers to mid-rail to optimize their performance. The ADS5500 requires an input common-mode voltage of 1.5 V. Due to the mismatch in required common-mode voltage, the signal is ac coupled from the amplifier output, via the two 1-nF capacitors, to the input of the ADC. The CM voltage of the ADS5500 is used to bias the ADC input to the required voltage, via the 1-kΩ resistors. Note: 100-µA common-mode current is drawn by the ADS5500 input stage (at 125 MSPS). This causes a 100-mV shift in the input common-mode voltage, which does not impact the performance when driving the input to –1 dB of full scale. To offset this effect, a voltage divider from the power supply can be used to derive the input common-mode voltage reference.

Because the operational amplifiers are configured as non-inverting, the inputs are high impedance. This is particularly useful when interfacing to a high-impedance source. In this situation, the amplifiers provide impedance matching and amplification of the signal.

The SFDR performance of the circuit is shown in the following graph (see Figure 56) and provides for full performance from the ADS5500 to 40 MHz.

The differential topology employed in this circuit provides for significant suppression of the 2nd-order harmonic distortion of the amplifiers. This, along with the superior 3rd-order harmonic distortion performance of the amplifiers, results in the SFDR performance of the circuit (at frequencies up to 40 MHz) being set by higher-order harmonics generated by the sampling process of the ADS5500.

The amplifier circuit (with resistor divider for bias voltage generation) requires a total of 185 mW of power from a single 5-V power supply.

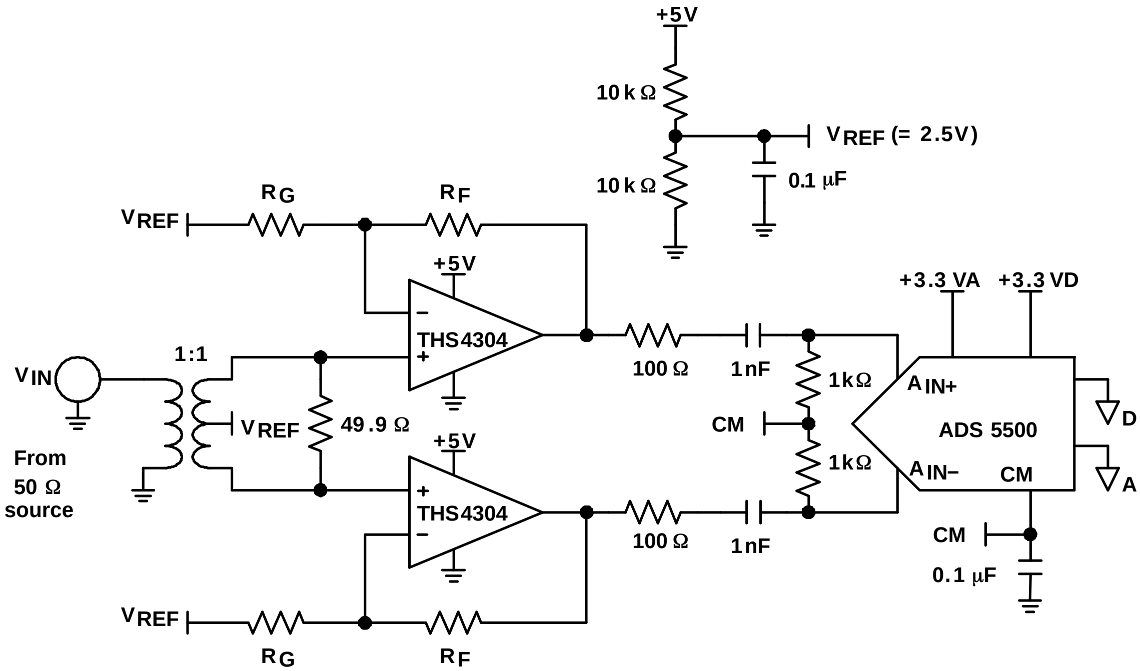

Figure 55. Differential ADC Drive Amplifier Circuit

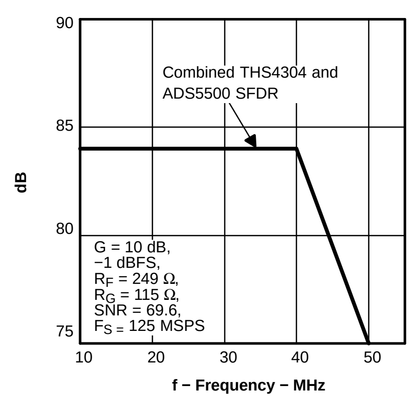

Figure 56. SFDR Performance versus Frequency – THS4304 Driving ADS5500

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
THS4304D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	4304	Samples
THS4304DBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	AKW	Samples
THS4304DBVRG4	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	AKW	Samples
THS4304DBVT	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	AKW	Samples
THS4304DBVTG4	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	AKW	Samples
THS4304DG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	4304	Samples
THS4304DGK	ACTIVE	VSSOP	DGK	8	80	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	AKU	Samples
THS4304DGKG4	ACTIVE	VSSOP	DGK	8	80	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	AKU	Samples
THS4304DR	OBSOLETE	SOIC	D	8		TBD	Call TI	Call TI	-40 to 85	4304	
THS4304DRG4	OBSOLETE	SOIC	D	8		TBD	Call TI	Call TI	-40 to 85	4304	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Only one of markings shown within the brackets will appear on the physical device.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF THS4304 :

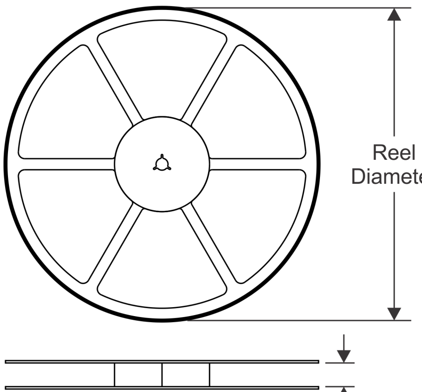
- Space: THS4304-SP

NOTE: Qualified Version Definitions:

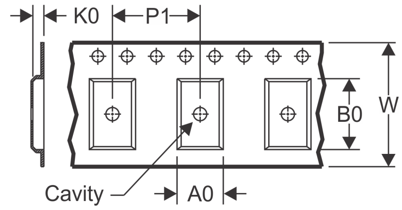
- Space - Radiation tolerant, ceramic packaging and qualified for use in Space-based application

TAPE AND REEL INFORMATION

REEL DIMENSIONS

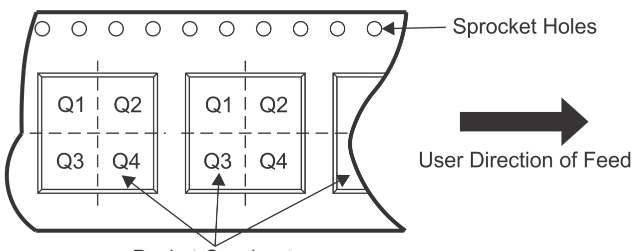


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

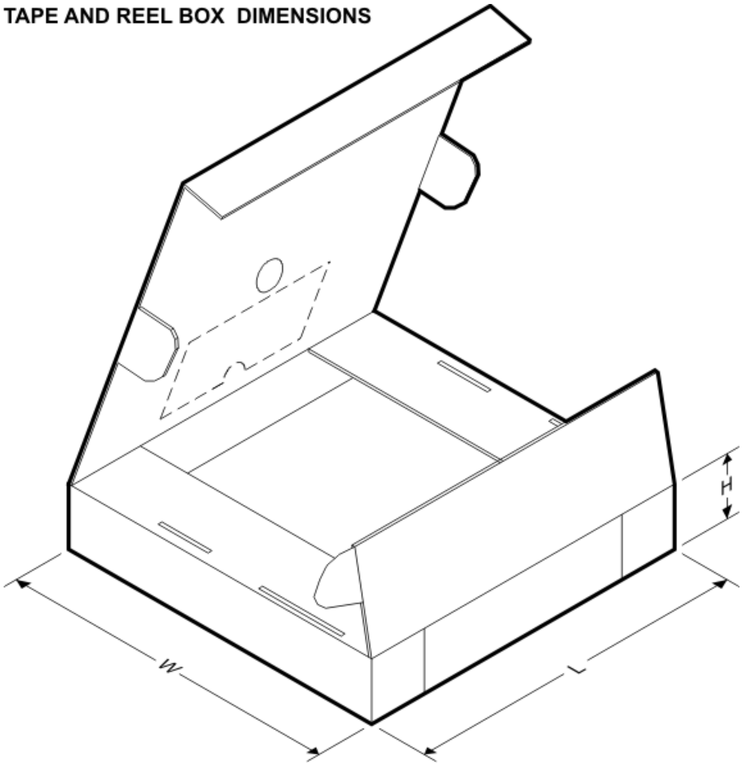
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
THS4304DBVR	SOT-23	DBV	5	3000	180.0	9.0	3.15	3.2	1.4	4.0	8.0	Q3
THS4304DBVT	SOT-23	DBV	5	250	180.0	9.0	3.15	3.2	1.4	4.0	8.0	Q3

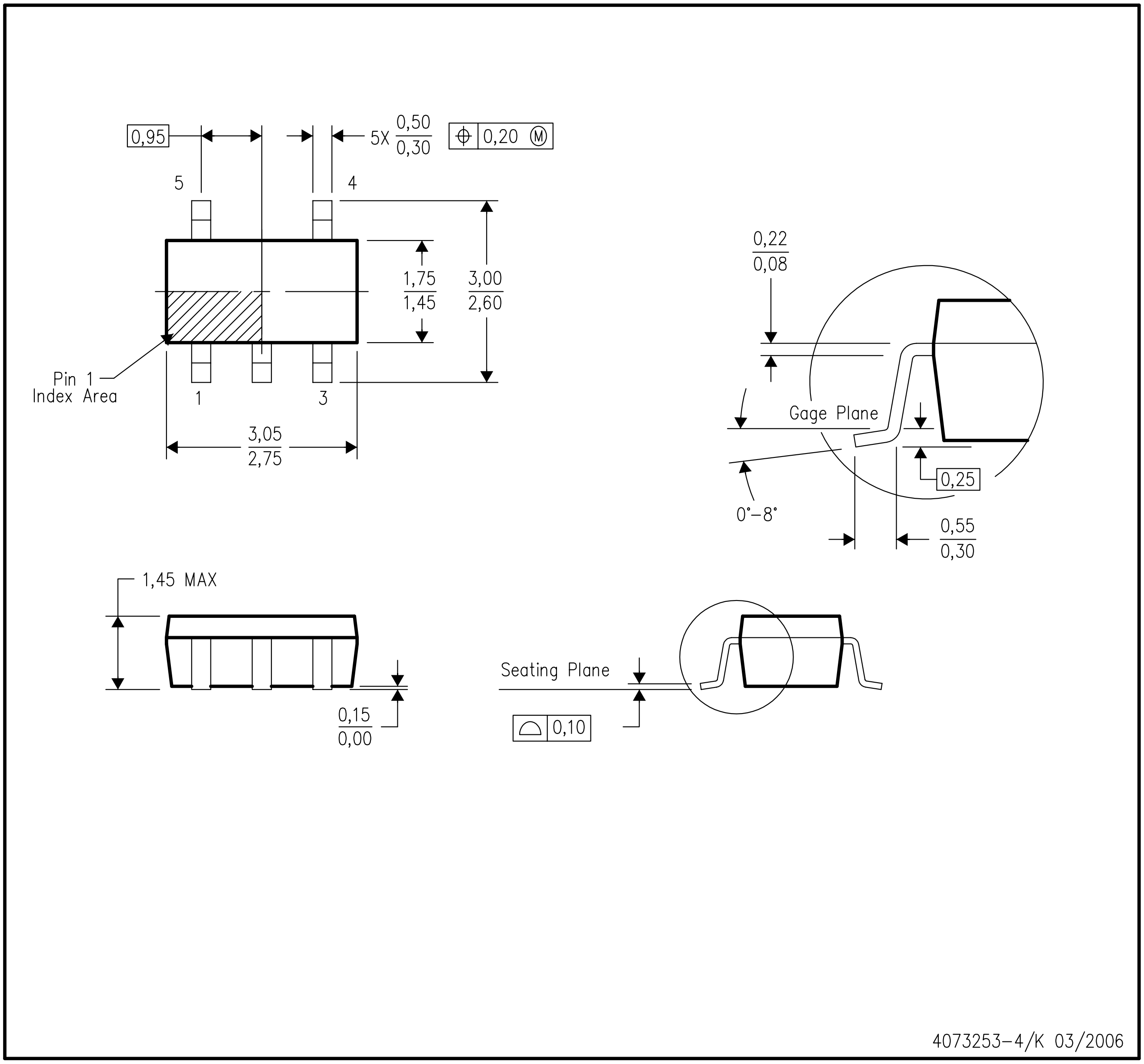
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

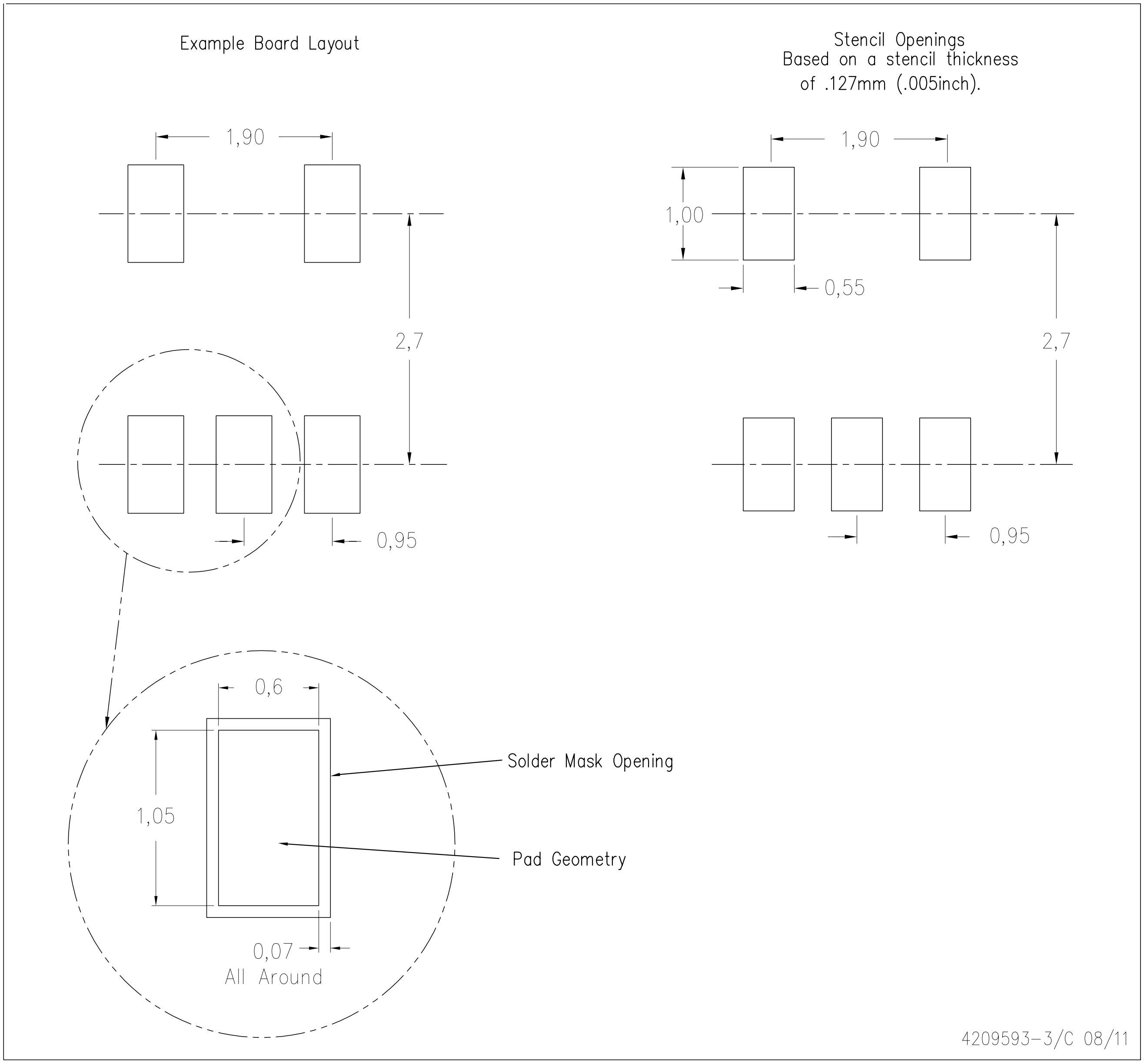
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
THS4304DBVR	SOT-23	DBV	5	3000	182.0	182.0	20.0
THS4304DBVT	SOT-23	DBV	5	250	182.0	182.0	20.0

DBV (R-PDSO-G5) PLASTIC SMALL-OUTLINE PACKAGE



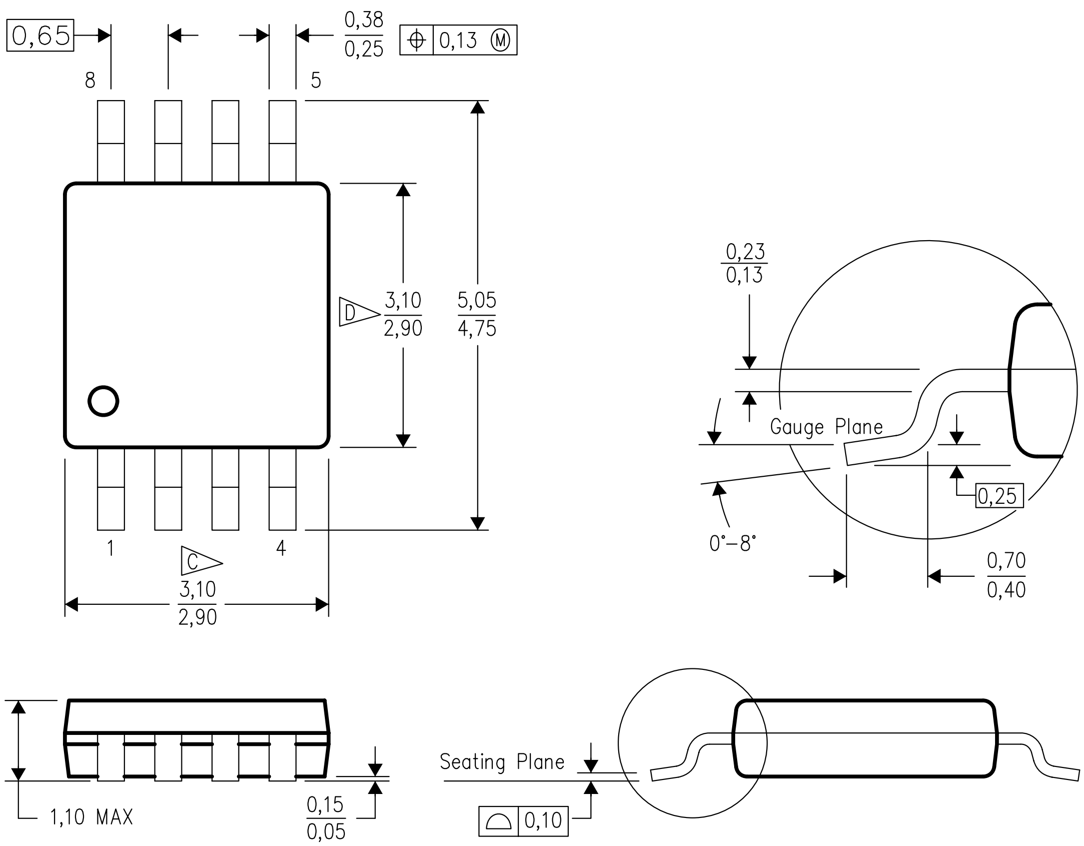
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. Falls within JEDEC MO-178 Variation AA.

DBV (R-PDSO-G5) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. Publication IPC-7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.

DGK (S–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE



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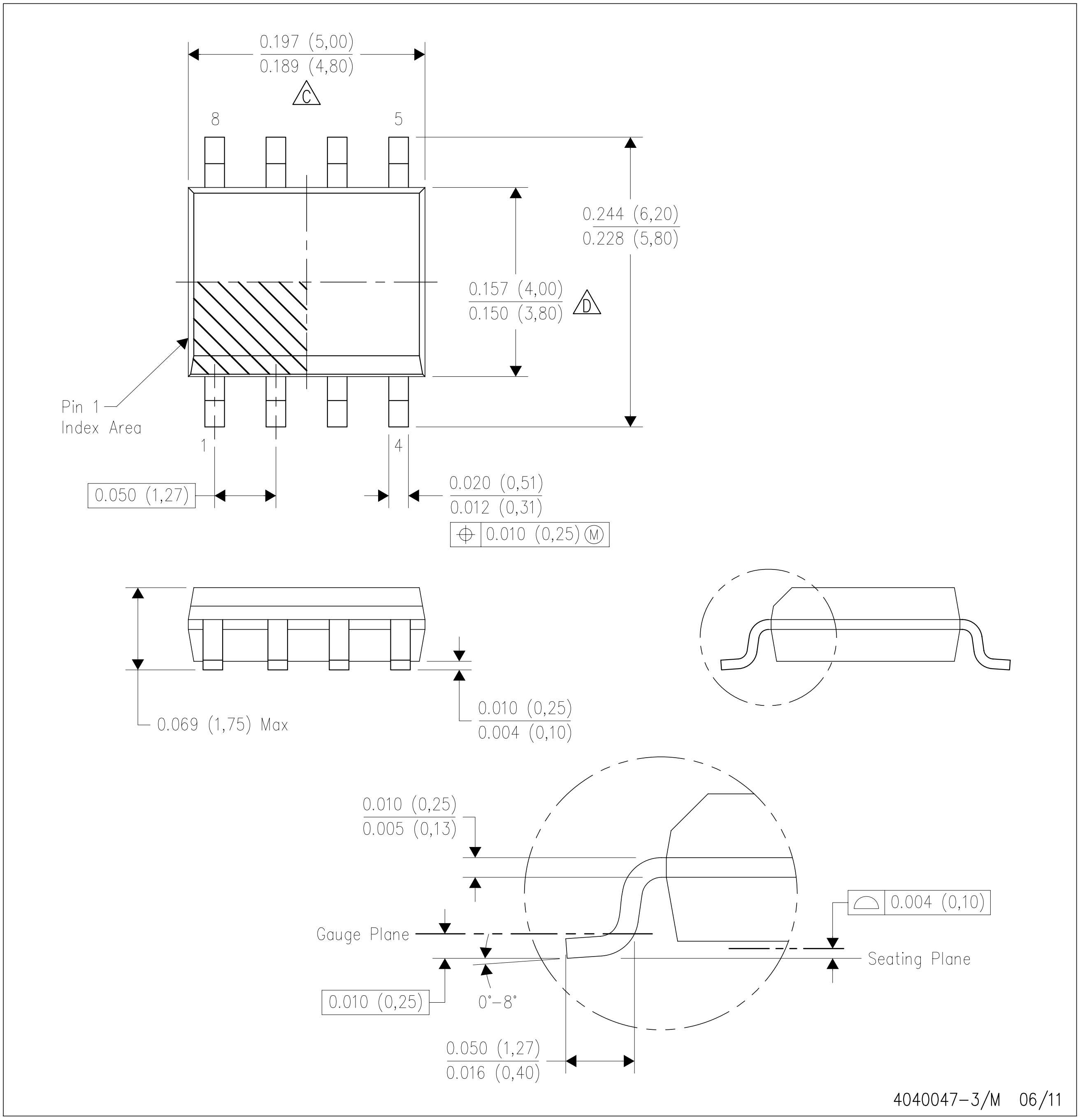
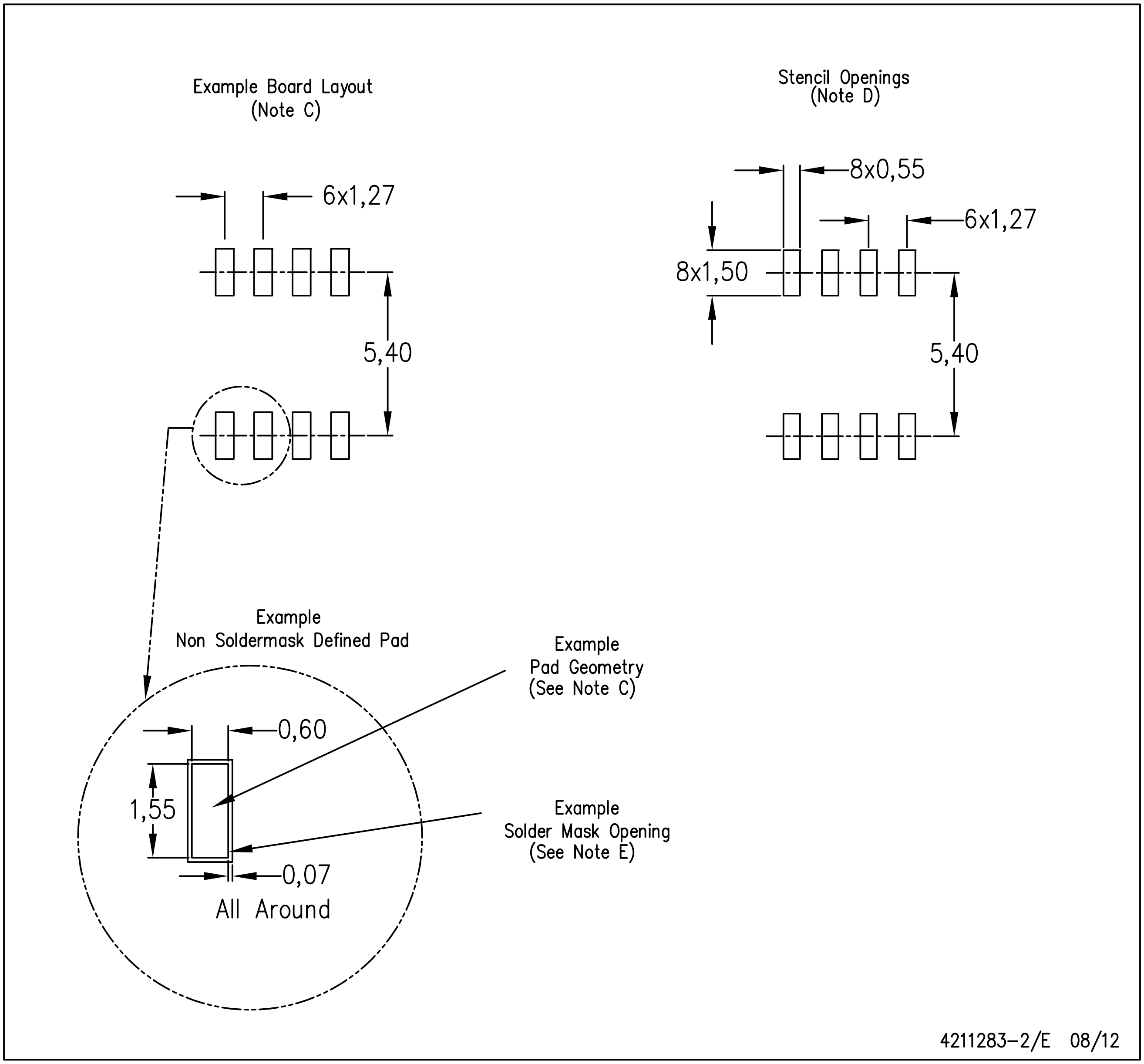
NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
E. Falls within JEDEC MO–187 variation AA, except interlead flash.

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS-012 variation AA.

D (R-PDSO-G8) PLASTIC SMALL OUTLINE



NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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