70-MHz HIGH-SPEED AMPLIFIERS

FEATURES

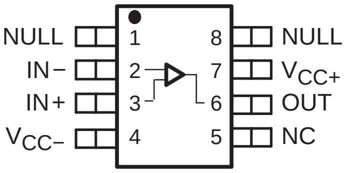
- High Speed:
  - 70 MHz Bandwidth (G = 1, −3 dB)
  - 240 V/µs Slew Rate
  - 60-ns Settling Time (0.1%)
- High Output Drive, I_O = 100 mA (typ)
- Excellent Video Performance:
  - 0.1 dB Bandwidth of 30 MHz (G = 1)
  - 0.01% Differential Gain
  - 0.01° Differential Phase
- Very Low Distortion:
  - THD = −82 dBc (f = 1 MHz, R_L = 150 Ω)
  - THD = −89 dBc (f = 1 MHz, R_L = 1 kΩ)
- Wide Range of Power Supplies:
  - V_{CC} = ±5 V to ±15 V
- Available in Standard SOIC, MSOP PowerPAD™, JG, or FK Packages
- Evaluation Module Available

DESCRIPTION

The THS4051 and THS4052 are general-purpose, single/dual, high-speed voltage feedback amplifiers ideal for a wide range of applications including video, communication, and imaging. The devices offer very good ac performance with 70-MHz bandwidth, 240-V/µs slew rate, and 60-ns settling time (0.1%). The THS4051/2 are stable at all gains for both inverting and non-inverting configurations. These amplifiers have a high output drive capability of 100 mA and draw only 8.5-mA supply current per channel. Excellent professional video results can be obtained with the low differential gain/phase errors of 0.01%/ 0.01° and wide 0.1-dB flatness to 30 MHz. For applications requiring low distortion, the THS4051/2 is ideally suited with total harmonic distortion of −82 dBc at 1 MHz.

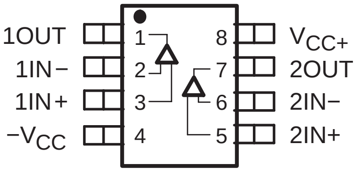
RELATED DEVICES	
DEVICE	**DESCRIPTION**
THS4011/2	290-MHz Low Distortion High-Speed Amplifiers
THS4031/2	100-MHz Low Noise High-Speed Amplifiers
THS4081/2	175-MHz Low Power High-Speed Amplifiers

THS4051
D, DGN, AND JG PACKAGES
(TOP VIEW)



NC − No internal connection

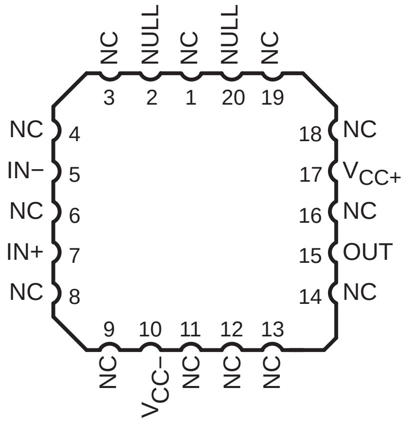
THS4052
D AND DGN† PACKAGES
(TOP VIEW)



Cross Section View Showing PowerPAD™ Option (DGN)

† This device is in the Product Preview stage of development. Please contact your local TI sales office for availability.

THS4051
FK PACKAGE
(TOP VIEW)



CAUTION: The THS4051 and THS4052 provide ESD protection circuitry. However, permanent damage can still occur if this device is subjected to high-energy electrostatic discharges. Proper ESD precautions are recommended to avoid any performance degradation or loss of functionality.

ABSOLUTE MAXIMUM RATINGS OVER OPERATING FREE-AIR TEMPERATURE (UNLESS OTHERWISE NOTED)(1)

Supply voltage, V_{CC}		±16.5 V
Input voltage, V_I		$\pm V_{CC}$
Output current, I_O		150 mA
Differential input voltage, V_{IO}		±4 V
Continuous total power dissipation		See Dissipation Rating Table
Maximum junction temperature, T_J		150°C
Operating free-air temperature, T_A:	C-suffix	0°C to 70°C
	I-suffix	−40°C to 85°C
	M-suffix	−55°C to 125°C
Storage temperature, T_{stg}		−65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds		300°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds, JG package		300°C
Case temperature for 60 seconds, FK package		260°C

(1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

DISSIPATION RATING TABLE

PACKAGE	θ_{JA} (°C/W)	θ_{JC} (°C/W)	T_A = 25°C POWER RATING
D	167‡	38.3	740 mW
DGN§	58.4	4.7	2.14 W
JG	119	28	1050 mW
FK	87.7	20	1375 mW

‡ This data was taken using the JEDEC standard Low-K test PCB. For the JEDEC Proposed High-K test PCB, the θ_{JA} is 95°C/W with a power rating at T_A = 25°C of 1.32 W.

§ This data was taken using 2 oz. trace and copper pad that is soldered directly to a 3 in. × 3 in. PC. For further information, refer to *Application Information* section of this data sheet.

RECOMMENDED OPERATING CONDITIONS

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC+} and V_{CC-}	Dual supply	±4.5		±16	V
	Single supply	9		32	
Operating free-air temperature, T_A	C-suffix	0		70	°C
	I-suffix	−40		85	
	M-suffix	−55		125	

AVAILABLE OPTIONS(1)

T_A	NUMBER OF CHANNELS	PACKAGED DEVICES					EVALUATION MODULE
		PLASTIC SMALL OUTLINE† (D)	PLASTIC MSOP† (DGN)		CERAMIC DIP (JG)	CHIP CARRIER (FK)	
			DEVICE	SYMBOL			
0°C to 70°C	1	THS4051CD	THS4051CDGN	ACQ	—	—	THS4051EVM
	2	THS4052CD	THS4052CDGN‡	ACE	—	—	THS4052EVM
−40°C to 85°C	1	THS4051ID	THS4051IDGN	ACR	—	—	—
	2	THS4052ID	THS4052IDGN‡	ACF	—	—	—
−55°C to 125°C	1	—	—	—	THS4051MJG	THS4051MFK	—

(1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.

† The D and DGN packages are available taped and reeled. Add an R suffix to the device type (i.e., THS4051CDGN).

‡ This device is in the Product Preview stage of development. Please contact your local TI sales office for availability.

FUNCTIONAL BLOCK DIAGRAM

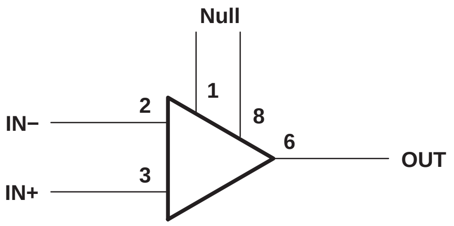


Figure 1. THS4051 − Single Channel

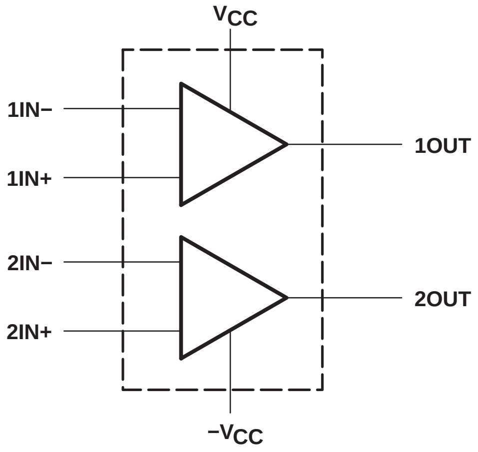
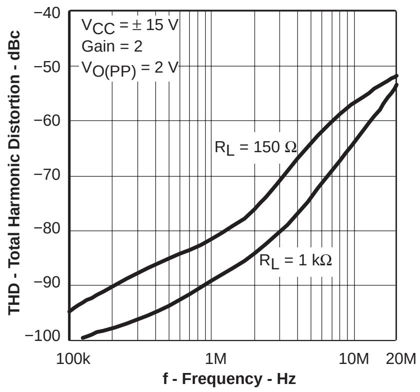


Figure 2. THS4052 − Dual Channel

T HARMONIC DISTORTION
vs
FREQUENCY



ELECTRICAL CHARACTERISTICS AT T_A = 25°C, V_{CC} = ±15 V, R_L = 150 Ω (unless otherwise noted)

dynamic performance

PARAMETER		TEST CONDITIONS[†]		THS405xC, THS405xI			UNIT
				MIN	TYP	MAX	
BW	Dynamic performance small-signal bandwidth (−3 dB)	V_{CC} = ±15 V	Gain = 1		70		MHz
		V_{CC} = ±5 V			70		
		V_{CC} = ±15 V	Gain = 2		38		MHz
		V_{CC} = ±5 V			38		
	Bandwidth for 0.1 dB flatness	V_{CC} = ±15 V	Gain = 1		30		MHz
		V_{CC} = ±5 V			30		
	Full power bandwidth[§]	$V_{O(pp)}$ = 20 V, V_{CC} = ±15 V			3.8		MHz
		$V_{O(pp)}$ = 5 V, V_{CC} = ±5 V			12.7		
SR	Slew rate[‡]	V_{CC} = ±15 V, 20-V step,	Gain = 5		240		V/μs
		V_{CC} = ±5 V, 5-V step	Gain = −1		200		
t_S	Settling time to 0.1%	V_{CC} = ±15 V, 5-V step	Gain = −1		60		ns
		V_{CC} = ±5 V, 2-V step			60		
	Settling time to 0.01%	V_{CC} = ±15 V, 5-V step	Gain = −1		130		ns
		V_{CC} = ±5 V, 2-V step			140		

[†] Full range = 0°C to 70°C for C suffix and −40°C to 85°C for I suffix

[‡] Slew rate is measured from an output level range of 25% to 75%.

[§] Full power bandwidth = slew rate/2 $\pi V_{O(Peak)}$.

noise/distortion performance

PARAMETER		TEST CONDITIONS[†]			THS405xC, THS405xI			UNIT
					MIN	TYP	MAX	
THD	Total harmonic distortion	$V_{O(pp)}$ = 2 V, f = 1 MHz, Gain = 2	V_{CC} = ±15 V	R_L = 150 Ω		−82		dBc
				R_L = 1 kΩ		−89		
			V_{CC} = ±5 V	R_L = 150 Ω		−78		
				R_L = 1 kΩ		−87		
V_n	Input voltage noise	V_{CC} = ±5 V or ±15 V,	f = 10 kHz			14		nV/√Hz
I_n	Input current noise	V_{CC} = ±5 V or ±15 V,	f = 10 kHz			0.9		pA/√Hz
	Differential gain error	Gain = 2, 40 IRE modulation,	NTSC, ±100 IRE ramp	V_{CC} = ±15 V		0.01%		
				V_{CC} = ±5 V		0.01%		
	Differential phase error	Gain = 2, 40 IRE modulation,	NTSC, ±100 IRE ramp	V_{CC} = ±15 V		0.01°		
				V_{CC} = ±5 V		0.03°		
	Channel-to-channel crosstalk (THS4052 only)	V_{CC} = ±5 V or ±15 V,	f = 1 MHz			−57		dB

[†] Full range = 0°C to 70°C for C suffix and −40°C to 85°C for I suffix.

electrical characteristics at T_A = 25°C, V_{CC} = ±15 V, R_L = 150 Ω (unless otherwise noted) (continued)

dc performance

PARAMETER		TEST CONDITIONS†		THS405xC, THS405xI			UNIT
				MIN	TYP	MAX	
	Open loop gain	V_{CC} = ±15 V, R_L = 1 kΩ V_O = ±10 V	T_A = 25°C	5	9		V/mV
			T_A = full range	3			
		V_{CC} = ±5 V, R_L = 250 Ω V_O = ±2.5 V	T_A = 25°C	2.5	6		V/mV
			T_A = full range	2			
V_{OS}	Input offset voltage	V_{CC} = ±5 V or ±15 V	T_A = 25°C		2.5	10	mV
			T_A = full range			12	
	Offset voltage drift	V_{CC} = ±5 V or ±15 V	T_A = full range		15		µV/°C
I_{IB}	Input bias current	V_{CC} = ±5 V or ±15 V	T_A = 25°C		2.5	6	µA
			T_A = full range			8	
I_{OS}	Input offset current	V_{CC} = ±5 V or ±15 V	T_A = 25°C		35	250	nA
			T_A = full range			400	
	Offset current drift	T_A = full range			0.3		nA/°C

† Full range = 0°C to 70°C for C suffix and −40°C to 85°C for I suffix

input characteristics

PARAMETER		TEST CONDITIONS†			THS405xC, THS405xI			UNIT
					MIN	TYP	MAX	
V_{ICR}	Common-mode input voltage range	V_{CC} = ±15 V			±13.8	±14.3		V
		V_{CC} = ±5 V			±3.8	±4.3		
CMRR	Common mode rejection ratio	V_{CC} = ±15 V,	V_{ICR} = ±12 V	T_A = full range	70	100		dB
		V_{CC} = ±5 V,	V_{ICR} = ±2.5 V		70	100		
r_i	Input resistance					1		MΩ
C_i	Input capacitance					1.5		pF

† Full range = 0°C to 70°C for C suffix and −40°C to 85°C for I suffix

output characteristics

PARAMETER		TEST CONDITIONS†		THS405xC, THS405xI			UNIT
				MIN	TYP	MAX	
V_O	Output voltage swing	V_{CC} = ±15 V	R_L = 250 Ω	±11.5	±13		V
		V_{CC} = ±5 V	R_L = 150 Ω	±3.2	±3.5		
		V_{CC} = ±15 V	R_L = 1 kΩ	±13	±13.6		V
		V_{CC} = ±5 V		±3.5	±3.8		
I_O	Output current‡	V_{CC} = ±15 V	R_L = 20 Ω	80	100		mA
		V_{CC} = ±5 V		50	75		
I_{SC}	Short-circuit current‡	V_{CC} = ±15 V			150		mA
R_O	Output resistance	Open loop			13		W

† Full range = 0°C to 70°C for C suffix and −40°C to 85°C for I suffix

‡ Observe power dissipation ratings to keep the junction temperature below the absolute maximum rating when the output is heavily loaded or shorted. See the absolute maximum ratings section of this data sheet for more information.

electrical characteristics at T_A = 25°C, V_{CC} = ±15 V, R_L = 150 Ω (unless otherwise noted) (continued)

power supply

PARAMETER		TEST CONDITIONS[†]		THS405xC, THS405xI			UNIT
				MIN	TYP	MAX	
V_{CC}	Supply voltage operating range	Dual supply		±4.5		±16.5	V
		Single supply		9		33	
I_{CC}	Supply current (per amplifier)	V_{CC} = ±15 V	T_A = 25°C		8.5	10.5	mA
			T_A = full range			11.5	
		V_{CC} = ±5 V	T_A = 25°C		7.5	9.5	
			T_A = full range			10.5	
PSRR	Power supply rejection ratio	V_{CC} = ±5 V or ±15 V	T_A = 25°C	70	84		dB
			T_A = full range	68			

[†] Full range = 0°C to 70°C for C suffix and −40°C to 85°C for I suffix

ELECTRICAL CHARACTERISTICS AT T_A = FULL RANGE, V_{CC} = ±15 V, R_L = 1 KΩ (UNLESS OTHERWISE NOTED)

dynamic performance

PARAMETER		TEST CONDITIONS[†]			THS4051M			UNIT
					MIN	TYP	MAX	
BW	Unity gain bandwidth	V_{CC} = ±15 V,	Closed loop	R_L = 1 kΩ	50[§]	70		MHz
	Dynamic performance small-signal bandwidth (−3 dB)	V_{CC} = ±15 V		Gain = 1		70		MHz
		V_{CC} = ±5 V				70		
		V_{CC} = ±15 V		Gain = 2		38		
		V_{CC} = ±5 V				38		
	Bandwidth for 0.1 dB flatness	V_{CC} = ±15 V		Gain = 1		30		MHz
		V_{CC} = ±5 V				30		
	Full power bandwidth[‡]	$V_{O(pp)}$ = 20 V,	V_{CC} = ±15 V			3.8		MHz
		$V_{O(pp)}$ = 5 V,	V_{CC} = ±5 V			12.7		
SR	Slew rate	V_{CC} = ±15 V,		R_L = 1 kΩ	240[§]	300		V/µs
		V_{CC} = ±5 V,	5-V step	Gain = −1		200		
t_s	Settling time to 0.1%	V_{CC} = ±15 V,	5-V step	Gain = −1		60		ns
		V_{CC} = ±5 V,	2-V step			60		
	Settling time to 0.01%	V_{CC} = ±15 V,	5-V step	Gain = −1		130		ns
		V_{CC} = ±5 V,	2-V step			140		

[†] Full range = −55°C to 125°C for the THS4051M.
[‡] Full power bandwidth = slew rate/2 $\pi V_{O(Peak)}$.
[§] This parameter is not tested.

electrical characteristics at T_A = full range, V_{CC} = ±15 V, R_L = 1 kΩ (unless otherwise noted)

noise/distortion performance

PARAMETER		TEST CONDITIONS†			THS4051M			UNIT
					MIN	TYP	MAX	
THD	Total harmonic distortion	$V_{O(pp)}$ = 2 V, f = 1 MHz, Gain = 2, T_A = 25°C	V_{CC} = ±15 V	R_L = 150 Ω		−82		dBc
				R_L = 1 kΩ		−89		
			V_{CC} = ±5 V	R_L = 150 Ω		−78		
				R_L = 1 kΩ		−87		
V_n	Input voltage noise	V_{CC} = ±5 V or ±15 V, T_A = 25°C	f = 10 kHz,	R_L = 150 Ω		14		nV/√Hz
I_n	Input current noise	V_{CC} = ±5 V or ±15 V, T_A = 25°C	f = 10 kHz,	R_L = 150 Ω		0.9		pA/√Hz
	Differential gain error	Gain = 2, 40 IRE modulation, T_A = 25°C,	NTSC, ±100 IRE ramp, R_L = 150 Ω	V_{CC} = ±15 V		0.01%		
				V_{CC} = ±5 V		0.01%		
	Differential phase error	Gain = 2, 40 IRE modulation, T_A = 25°C,	NTSC, ±100 IRE ramp, R_L = 150 Ω	V_{CC} = ±15 V		0.01°		
				V_{CC} = ±5 V		0.03°		

† Full range = −55°C to 125°C for the THS4051M.

dc performance

PARAMETER		TEST CONDITIONS†		THS4051M			UNIT
				MIN	TYP	MAX	
	Open loop gain	V_{CC} = ±15 V, V_O = ±10 V	T_A = 25°C	5	9		V/mV
			T_A = full range	3			
		V_{CC} = ±5 V, V_O = ±2.5 V	T_A = 25°C	2.5	6		V/mV
			T_A = full range	2			
V_{IO}	Input offset voltage	V_{CC} = ±5 V or ±15 V	T_A = 25°C		2.5	10	mV
			T_A = full range			13	
	Offset voltage drift	V_{CC} = ±5 V or ±15 V	T_A = full range		15		µV/°C
I_{IB}	Input bias current	V_{CC} = ±5 V or ±15 V	T_A = 25°C		2.5	6	µA
			T_A = full range			8	
I_{IO}	Input offset current	V_{CC} = ±5 V or ±15 V	T_A = 25°C		35	250	nA
			T_A = full range			400	
	Offset current drift	T_A = full range			0.3		nA/°C

† Full range = −55°C to 125°C for the THS4051M.

input characteristics

PARAMETER		TEST CONDITIONS†			THS4051M			UNIT
					MIN	TYP	MAX	
V_{ICR}	Common-mode input voltage range	V_{CC} = ±15 V			±13.8	±14.3		V
		V_{CC} = ±5 V			±3.8	±4.3		
CMRR	Common mode rejection ratio	V_{CC} = ±15 V,	V_{ICR} = ±12 V	T_A = full range	70	100		dB
		V_{CC} = ±5 V,	V_{ICR} = ±2.5 V		70	100		
r_i	Input resistance					1		MΩ
C_i	Input capacitance					1.5		pF

† Full range = −55°C to 125°C for the THS4051M.

electrical characteristics at T_A = full range, V_{CC} = ±15 V, R_L = 1 kΩ (unless otherwise noted) (continued)

output characteristics

PARAMETER		TEST CONDITIONS[†]		THS4051M			UNIT
				MIN	TYP	MAX	
V_O	Output voltage swing	V_{CC} = ±15 V	R_L = 250 Ω	±12	±13		V
		V_{CC} = ±5 V	R_L = 150 Ω	±3.2	±3.5		
		V_{CC} = ±15 V	R_L = 1 kΩ	±13	±13.6		V
		V_{CC} = ±5 V		±3.5	±3.8		
I_O	Output current[‡]	V_{CC} = ±15 V, T_A = 25°C	R_L = 20 Ω	80	100		mA
		V_{CC} = ±15 V, T_A = full range		70			
		V_{CC} = ±5 V		50	75		
I_{SC}	Short-circuit current[‡]	V_{CC} = ±15 V			150		mA
R_O	Output resistance	Open loop			13		W

[†] Full range = −55°C to 125°C for the THS4051M.

[‡] Observe power dissipation ratings to keep the junction temperature below the absolute maximum rating when the output is heavily loaded or shorted. See the absolute maximum ratings section of this data sheet for more information.

power supply

PARAMETER		TEST CONDITIONS[†]		THS4051M			UNIT
				MIN	TYP	MAX	
V_{CC}	Supply voltage operating range	Dual supply		±4.5		±16.5	V
		Single supply		9		33	
I_{CC}	Supply current (per amplifier)	V_{CC} = ±15 V	T_A = 25°C		8.5	10.5	mA
			T_A = full range			11.5	
		V_{CC} = ±5 V	T_A = 25°C		7.5	9.5	
			T_A = full range			10.5	
PSRR	Power supply rejection ratio	V_{CC} = ±5 V or ±15 V	T_A = full range	70	84		dB

[†] Full range = −55°C to 125°C for the THS4051M.

TYPICAL CHARACTERISTICS

INPUT OFFSET VOLTAGE vs FREE-AIR TEMPERATURE

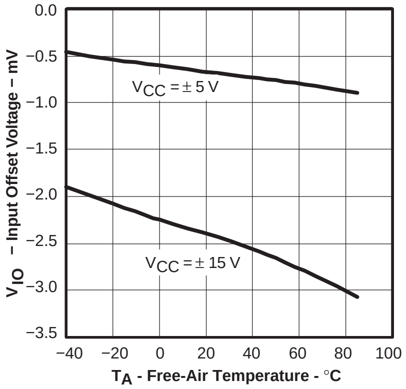


Figure 3

INPUT BIAS CURRENT vs FREE-AIR TEMPERATURE

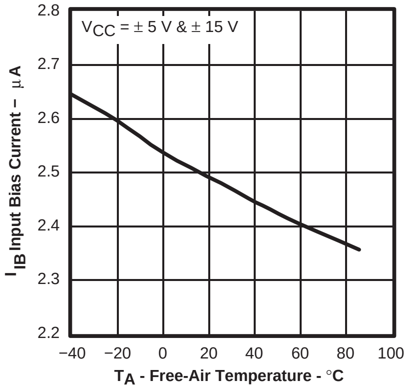


Figure 4

OUTPUT VOLTAGE vs SUPPLY VOLTAGE

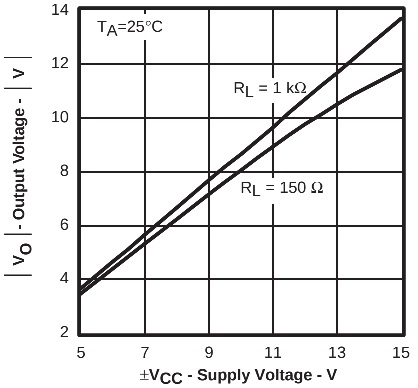


Figure 5

COMMON-MODE INPUT VOLTAGE vs SUPPLY VOLTAGE

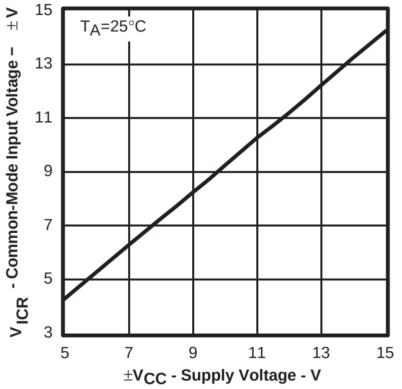


Figure 6

OUTPUT VOLTAGE vs FREE-AIR TEMPERATURE

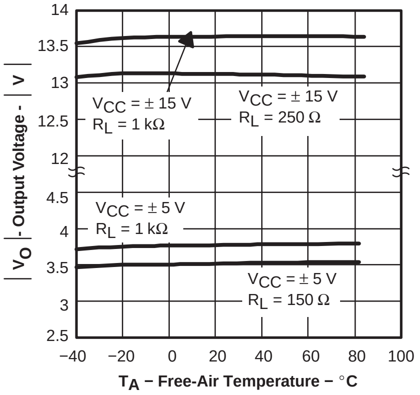


Figure 7

SUPPLY CURRENT vs SUPPLY VOLTAGE

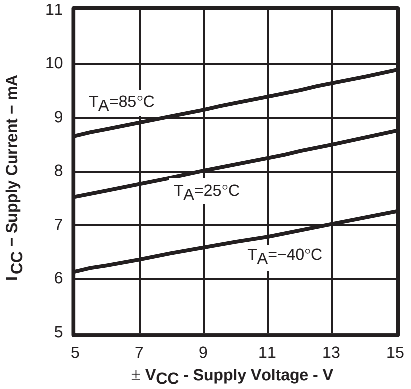


Figure 8

VOLTAGE & CURRENT NOISE vs FREQUENCY

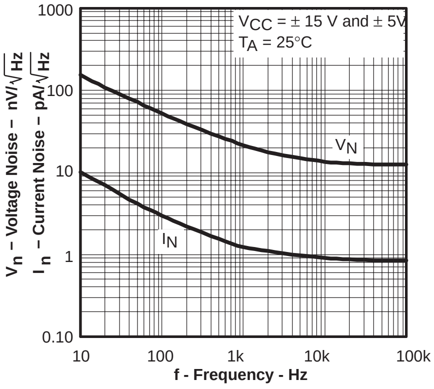


Figure 9

POWER-SUPPLY REJECTION RATIO vs FREQUENCY

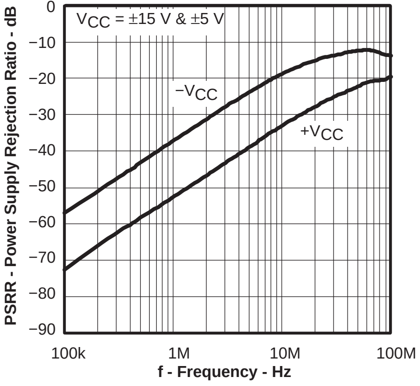


Figure 10

CMRR vs FREQUENCY

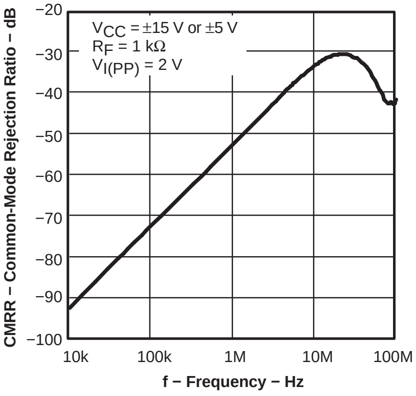


Figure 11

TYPICAL CHARACTERISTICS

CROSSTALK vs FREQUENCY

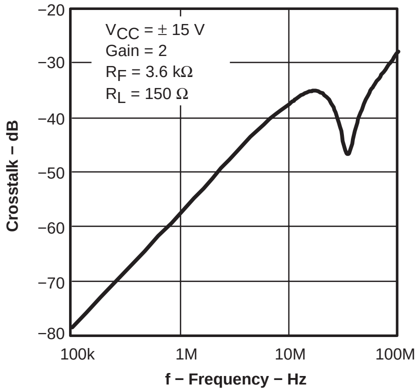


Figure 12

OPEN LOOP GAIN AND PHASE RESPONSE vs FREQUENCY

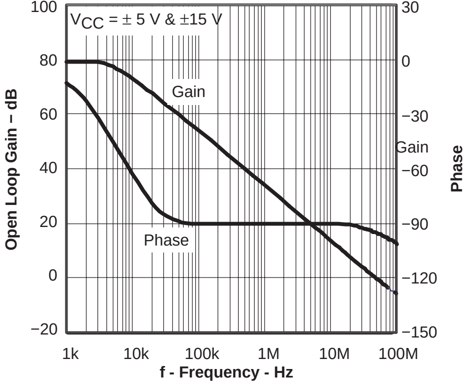


Figure 13

T HARMONIC DISTORTION vs FREQUENCY

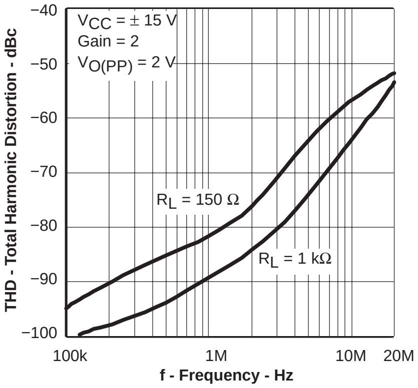


Figure 14

DISTORTION vs OUTPUT VOLTAGE

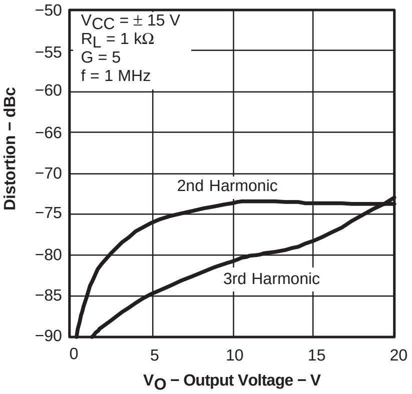


Figure 15

DISTORTION vs OUTPUT VOLTAGE

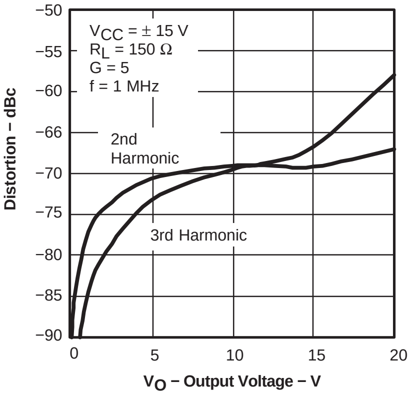


Figure 16

DISTORTION vs FREQUENCY

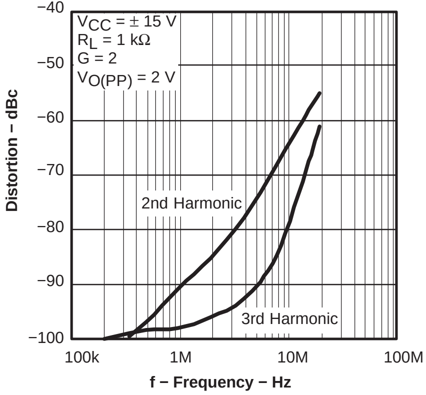


Figure 17

DISTORTION vs FREQUENCY

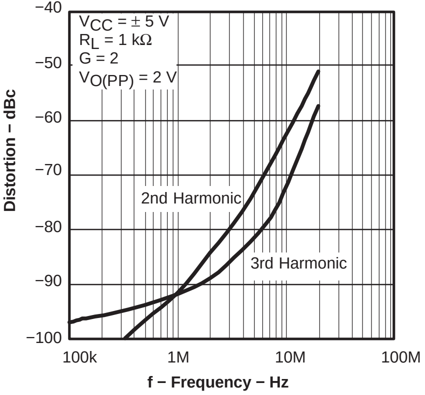


Figure 18

DISTORTION vs FREQUENCY

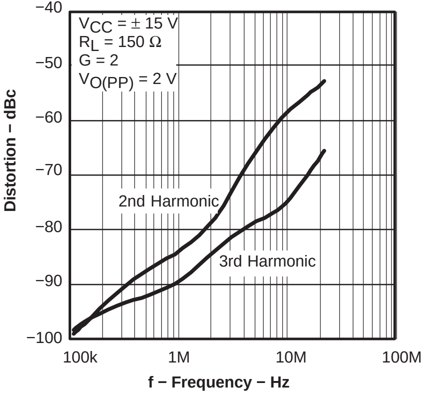


Figure 19

TYPICAL CHARACTERISTICS

DISTORTION
vs
FREQUENCY

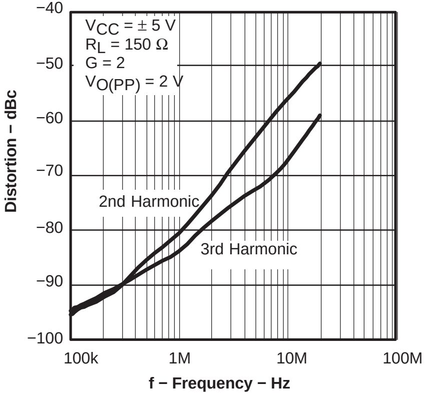


Figure 20

OUTPUT AMPLITUDE
vs
FREQUENCY

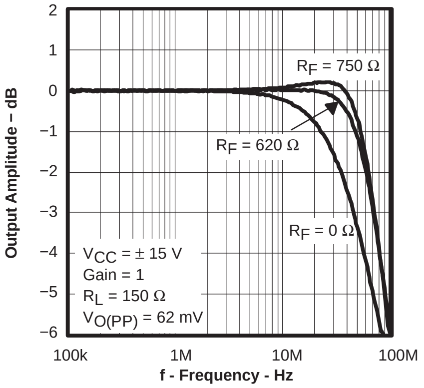


Figure 21

OUTPUT AMPLITUDE
vs
FREQUENCY

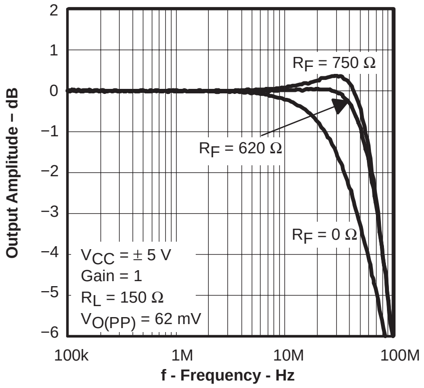


Figure 22

OUTPUT AMPLITUDE
vs
FREQUENCY

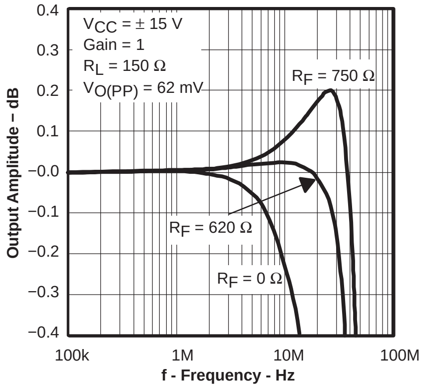


Figure 23

OUTPUT AMPLITUDE
vs
FREQUENCY

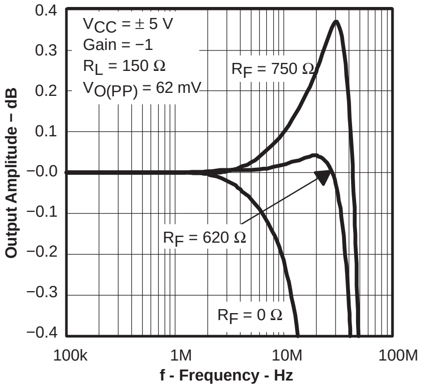


Figure 24

OUTPUT AMPLITUDE
vs
FREQUENCY

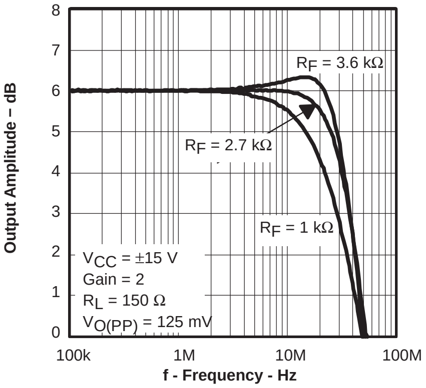


Figure 25

OUTPUT AMPLITUDE
vs
FREQUENCY

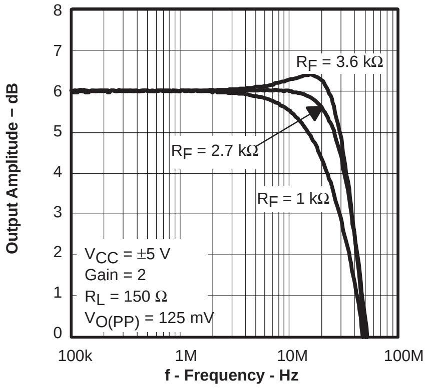


Figure 26

OUTPUT AMPLITUDE
vs
FREQUENCY

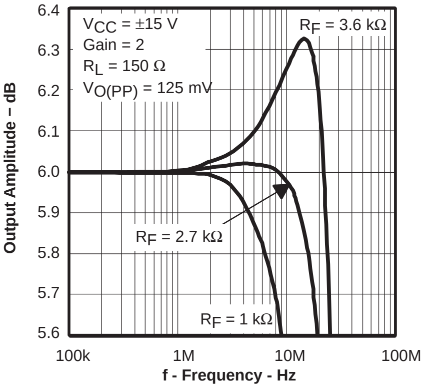


Figure 27

OUTPUT AMPLITUDE
vs
FREQUENCY

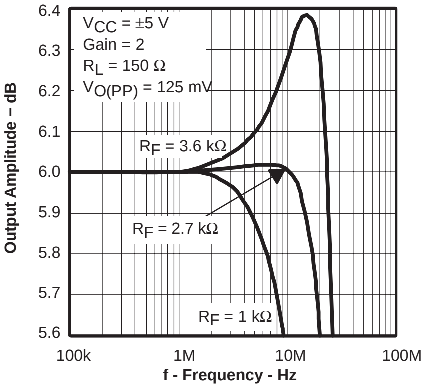
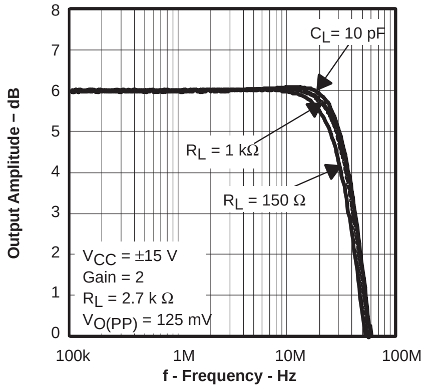


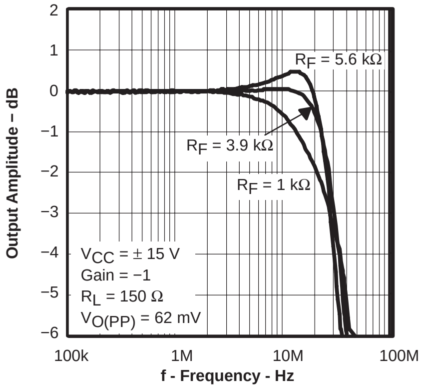
Figure 28

TYPICAL CHARACTERISTICS



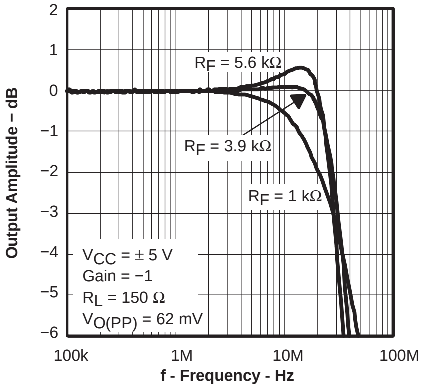
OUTPUT AMPLITUDE vs FREQUENCY

Figure 29



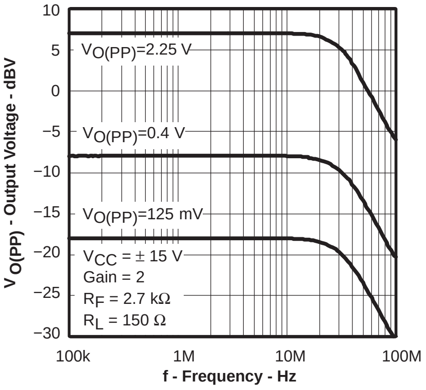
OUTPUT AMPLITUDE vs FREQUENCY

Figure 30



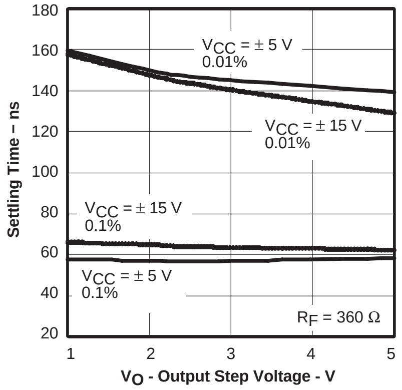
OUTPUT AMPLITUDE vs FREQUENCY

Figure 31



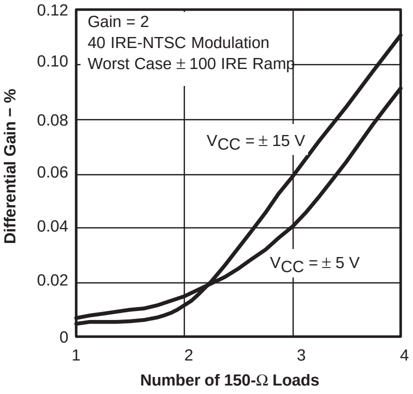
OUTPUT AMPLITUDE vs FREQUENCY

Figure 32



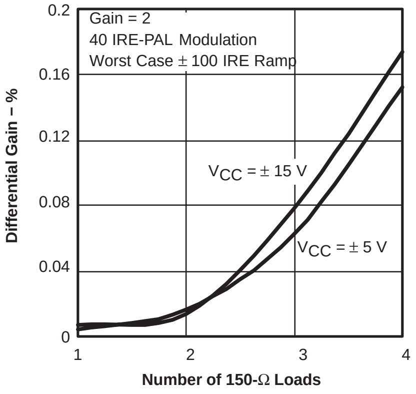
SETTING TIME vs OUTPUT STEP

Figure 33



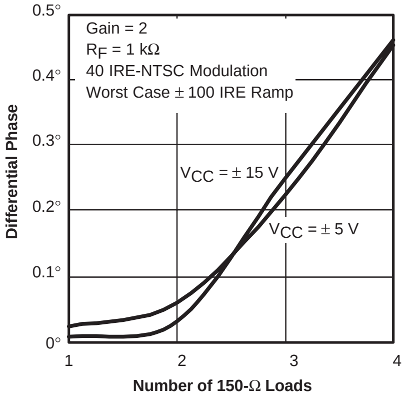
DIFFERENTIAL GAIN vs NUMBER OF 150-Ω LOADS

Figure 34



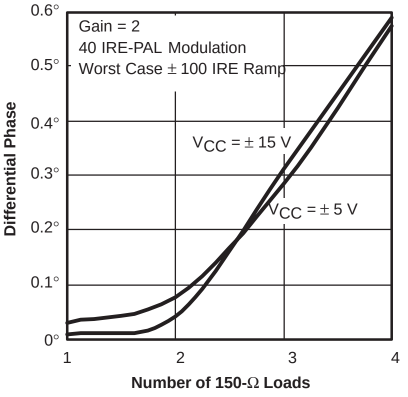
DIFFERENTIAL GAIN vs NUMBER OF 150-Ω LOADS

Figure 35



DIFFERENTIAL PHASE vs NUMBER OF 150-Ω LOADS

Figure 36



DIFFERENTIAL PHASE vs NUMBER OF 150-Ω LOADS

Figure 37

TYPICAL CHARACTERISTICS

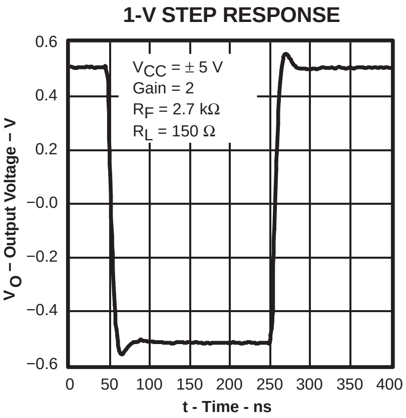

1-V STEP RESPONSE

Figure 38

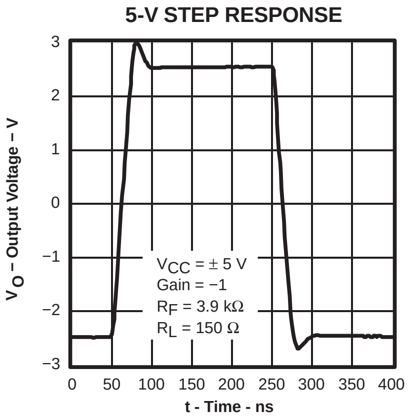

5-V STEP RESPONSE

Figure 39

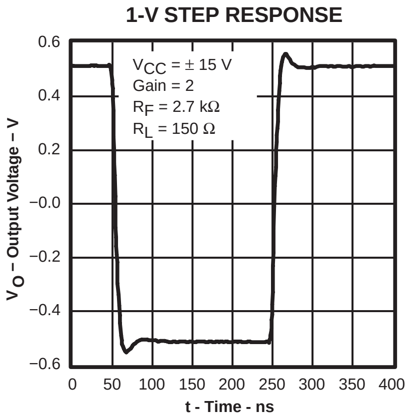

1-V STEP RESPONSE

Figure 40

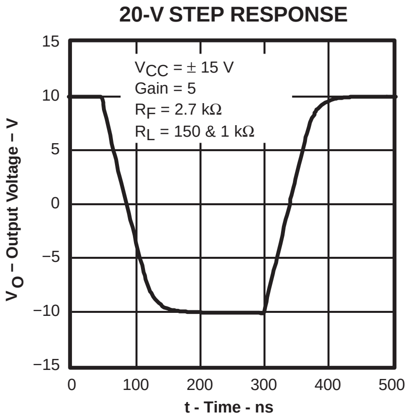

20-V STEP RESPONSE

Figure 41

APPLICATION INFORMATION

THEORY OF OPERATION

The THS405x is a high-speed operational amplifier configured in a voltage feedback architecture. It is built using a 30-V, dielectrically isolated, complementary bipolar process with NPN and PNP transistors possessing f_Ts of several GHz. This results in an exceptionally high performance amplifier that has a wide bandwidth, high slew rate, fast settling time, and low distortion. A simplified schematic is shown in Figure 42.

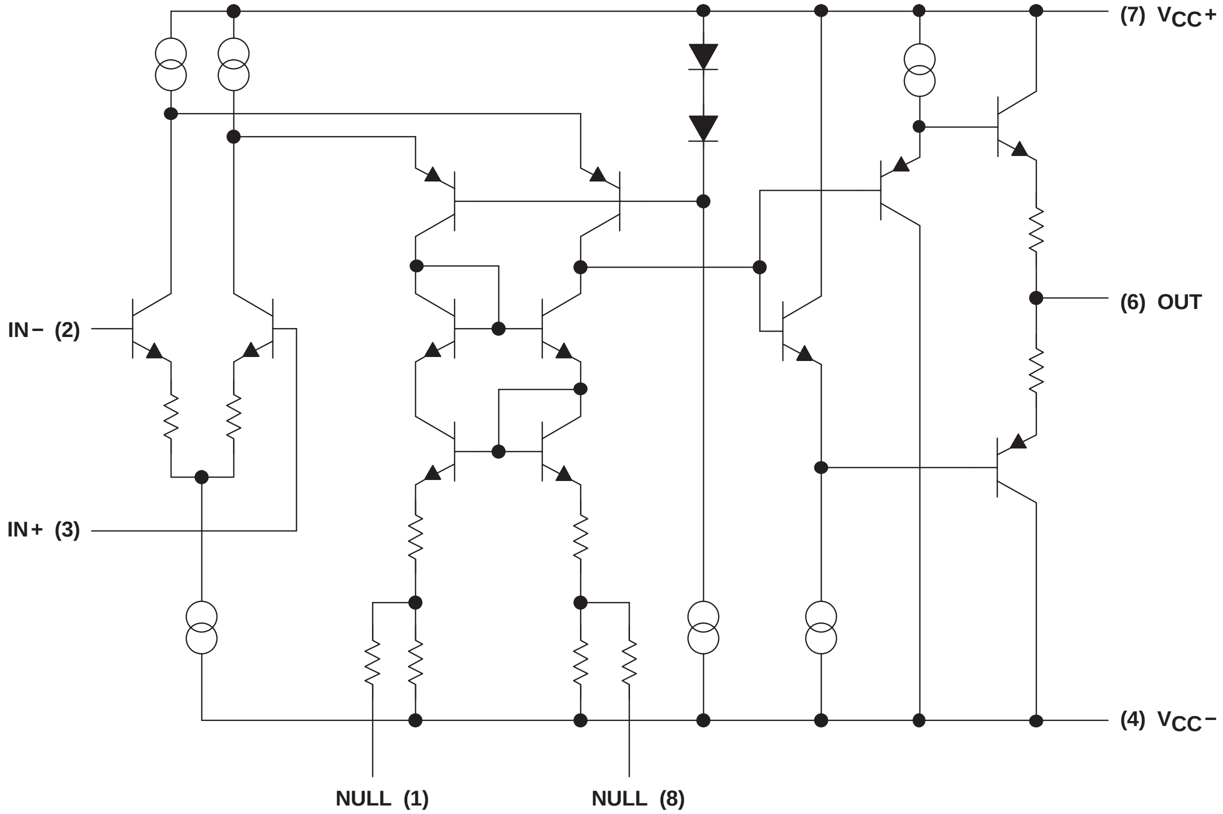


Figure 42. THS405x Simplified Schematic

NOISE CALCULATIONS AND NOISE FIGURE

Noise can cause errors on very small signals. This is especially true when amplifying small signals, where signal-to-noise ratio (SNR) is very important. The noise model for the THS405x is shown in Figure 43. This model includes all of the noise sources as follows:

- e_n = Amplifier internal voltage noise ($nV/\sqrt{Hz}$)
- IN+ = Noninverting current noise ($pA/\sqrt{Hz}$)
- IN− = Inverting current noise ($pA/\sqrt{Hz}$)
- e_{Rx} = Thermal voltage noise associated with each resistor ($e_{Rx} = 4\ kTR_x$)

APPLICATION INFORMATION

NOISE CALCULATIONS AND NOISE FIGURE (CONTINUED)

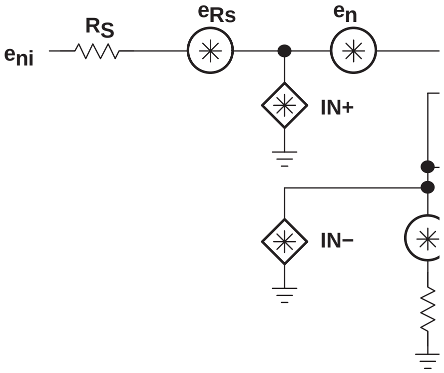


Figure 43. Noise Model

The total equivalent input noise density (e_{ni}) is calculated by using the following equation:

$$e_{ni} = \sqrt{\left(e_n\right)^2 + \left(IN+ \times R_S\right)^2 + \left(IN- \times \left(R_F \parallel R_G\right)\right)^2 + 4\,kTR_S + 4\,kT\left(R_F \parallel R_G\right)}$$

Where:

k = Boltzmann’s constant = 1.380658×10^{-23}
T = Temperature in degrees Kelvin (273 +°C)
$R_F \parallel R_G$ = Parallel resistance of R_F and R_G

To get the equivalent output noise of the amplifier, just multiply the equivalent input noise density (e_{ni}) by the overall amplifier gain (A_V).

$$e_{no} = e_{ni}\,A_V = e_{ni}\left(1 + \frac{R_F}{R_G}\right) \text{ (noninverting case)}$$

As the previous equations show, to keep noise at a minimum, small value resistors should be used. As the closed-loop gain is increased (by reducing R_G), the input noise is reduced considerably because of the parallel resistance term. This leads to the general conclusion that the most dominant noise sources are the source resistor (R_S) and the internal amplifier noise voltage (e_n). Because noise is summed in a root-mean-squares method, noise sources smaller than 25% of the largest noise source can be effectively ignored. This can greatly simplify the formula and make noise calculations much easier to calculate.

For more information on noise analysis, please refer to the *Noise Analysis* section in *Operational Amplifier Circuits Applications Report* (literature number SLVA043).

APPLICATION INFORMATION

NOISE CALCULATIONS AND NOISE FIGURE (CONTINUED)

This brings up another noise measurement usually preferred in RF applications, the noise figure (NF). Noise figure is a measure of noise degradation caused by the amplifier. The value of the source resistance must be defined and is typically 50 Ω in RF applications.

$$NF = 10\log\left[\frac{{e_{ni}}^2}{\left(e_{Rs}\right)^2}\right]$$

Because the dominant noise components are generally the source resistance and the internal amplifier noise voltage, we can approximate noise figure as:

$$NF = 10\log\left[1+\frac{\left[\left(e_n\right)^2+\left(IN+\times R_S\right)^2\right]}{4\ kTR_S}\right]$$

Figure 44 shows the noise figure graph for the THS405x.

NOISE FIGURE
vs
SOURCE RESISTANCE

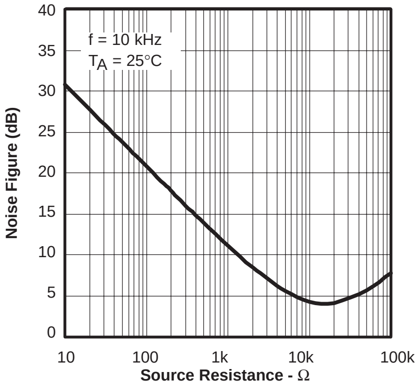


Figure 44. Noise Figure vs Source Resistance

APPLICATION INFORMATION

DRIVING A CAPACITIVE LOAD

Driving capacitive loads with high performance amplifiers is not a problem as long as certain precautions are taken. The first is to realize that the THS405x has been internally compensated to maximize its bandwidth and slew rate performance. When the amplifier is compensated in this manner, capacitive loading directly on the output will decrease the device's phase margin leading to high frequency ringing or oscillations. Therefore, for capacitive loads of greater than 10 pF, it is recommended that a resistor be placed in series with the output of the amplifier, as shown in Figure 45. A minimum value of 20 Ω should work well for most applications. For example, in 75-Ω transmission systems, setting the series resistor value to 75 Ω both isolates any capacitance loading and provides the proper line impedance matching at the source end.

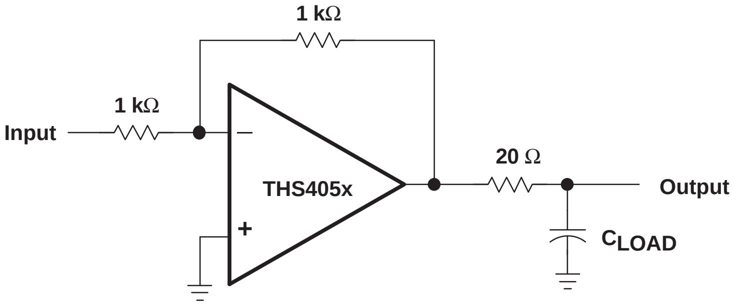


Figure 45. Driving a Capacitive Load

OFFSET NULLING

The THS405x has very low input offset voltage for a high-speed amplifier. However, if additional correction is required, an offset nulling function has been provided on the THS4051. The input offset can be adjusted by placing a potentiometer between terminals 1 and 8 of the device and tying the wiper to the negative supply. This is shown in Figure 46.

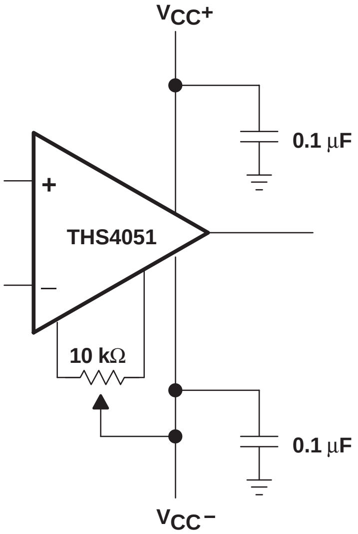
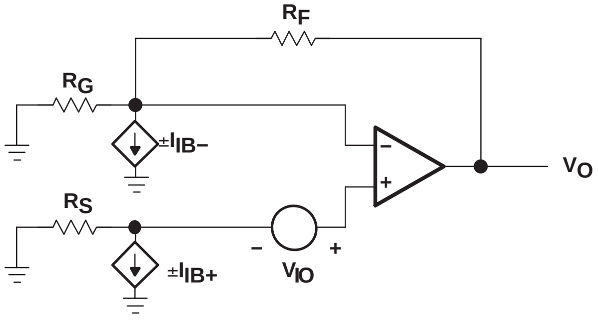


Figure 46. Offset Nulling Schematic

APPLICATION INFORMATION

OFFSET VOLTAGE

The output offset voltage, (V_{OO}) is the sum of the input offset voltage (V_{IO}) and both input bias currents (I_{IB}) times the corresponding gains. The following schematic and formula can be used to calculate the output offset voltage:



$$V_{OO} = V_{IO}\left(1 + \frac{R_F}{R_G}\right) \pm I_{IB+}\, R_S\left(1 + \frac{R_F}{R_G}\right) \pm I_{IB-}\, R_F$$

Figure 47. Output Offset Voltage Model

OPTIMIZING UNITY GAIN RESPONSE

Internal frequency compensation of the THS405x was selected to provide very wideband performance yet still maintain stability when operated in a noninverting unity gain configuration. When amplifiers are compensated in this manner there is usually peaking in the closed loop response and some ringing in the step response for very fast input edges, depending upon the application. This is because a minimum phase margin is maintained for the G=+1 configuration. For optimum settling time and minimum ringing, a feedback resistor of 620 Ω should be used as shown in Figure 48. Additional capacitance can also be used in parallel with the feedback resistance if even finer optimization is required.

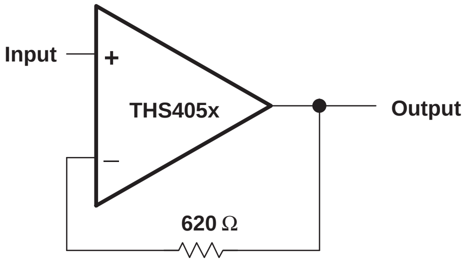


Figure 48. Noninverting, Unity Gain Schematic

APPLICATION INFORMATION

GENERAL CONFIGURATIONS

When receiving low-level signals, limiting the bandwidth of the incoming signals into the system is often required. The simplest way to accomplish this is to place an RC filter at the noninverting terminal of the amplifier (see Figure 49).

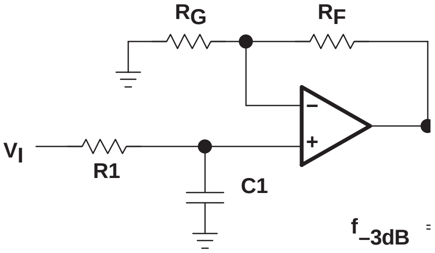


Figure 49. Single-Pole Low-Pass Filter

If even more attenuation is needed, a multiple pole filter is required. The Sallen-Key filter can be used for this task. For best results, the amplifier should have a bandwidth that is 8 to 10 times the filter frequency bandwidth. Failure to do this can result in phase shift of the amplifier.

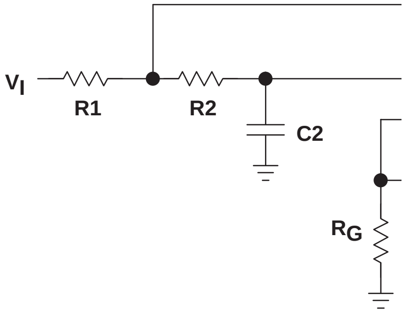


Figure 50. 2-Pole Low-Pass Sallen-Key Filter

APPLICATION INFORMATION

CIRCUIT LAYOUT CONSIDERATIONS

To achieve the levels of high frequency performance of the THS405x, follow proper printed-circuit board high frequency design techniques. A general set of guidelines is given below. In addition, a THS405x evaluation board is available to use as a guide for layout or for evaluating the device performance.

- Ground planes − It is highly recommended that a ground plane be used on the board to provide all components with a low inductive ground connection. However, in the areas of the amplifier inputs and output, the ground plane can be removed to minimize the stray capacitance.
- Proper power supply decoupling − Use a 6.8-µF tantalum capacitor in parallel with a 0.1-µF ceramic capacitor on each supply terminal. It may be possible to share the tantalum among several amplifiers depending on the application, but a 0.1-µF ceramic capacitor should always be used on the supply terminal of every amplifier. In addition, the 0.1-µF capacitor should be placed as close as possible to the supply terminal. As this distance increases, the inductance in the connecting trace makes the capacitor less effective. The designer should strive for distances of less than 0.1 inches between the device power terminals and the ceramic capacitors.
- Sockets − Sockets are not recommended for high-speed operational amplifiers. The additional lead inductance in the socket pins will often lead to stability problems. Surface-mount packages soldered directly to the printed-circuit board is the best implementation.
- Short trace runs/compact part placements − Optimum high frequency performance is achieved when stray series inductance has been minimized. To realize this, the circuit layout should be made as compact as possible, thereby minimizing the length of all trace runs. Particular attention should be paid to the inverting input of the amplifier. Its length should be kept as short as possible. This will help to minimize stray capacitance at the input of the amplifier.
- Surface-mount passive components − Using surface-mount passive components is recommended for high frequency amplifier circuits for several reasons. First, because of the extremely low lead inductance of surface-mount components, the problem with stray series inductance is greatly reduced. Second, the small size of surface-mount components naturally leads to a more compact layout thereby minimizing both stray inductance and capacitance. If leaded components are used, it is recommended that the lead lengths be kept as short as possible.

GENERAL POWERPAD™ DESIGN CONSIDERATIONS

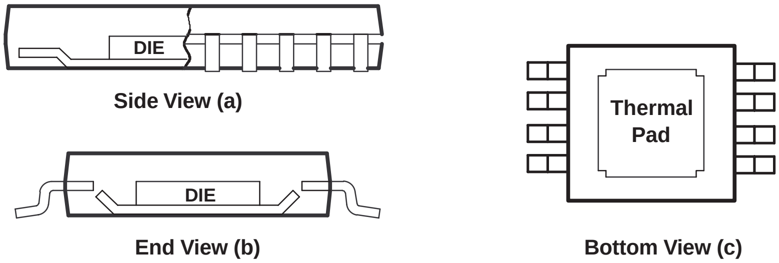
The THS405x is available packaged in a thermally-enhanced DGN package, which is a member of the PowerPAD™ family of packages. This package is constructed using a downset leadframe upon which the die is mounted [see Figure 51(a) and Figure 51(b)]. This arrangement results in the lead frame being exposed as a thermal pad on the underside of the package [see Figure 51(c)]. Because this thermal pad has direct thermal contact with the die, excellent thermal performance can be achieved by providing a good thermal path away from the thermal pad.

The PowerPAD™ package allows for both assembly and thermal management in one manufacturing operation. During the surface-mount solder operation (when the leads are being soldered), the thermal pad can also be soldered to a copper area underneath the package. Through the use of thermal paths within this copper area, heat can be conducted away from the package into either a ground plane or other heat dissipating device.

The PowerPAD™ package represents a breakthrough in combining the small area and ease of assembly of the surface mount with the, heretofore, awkward mechanical methods of heatsinking.

APPLICATION INFORMATION

GENERAL POWERPAD™ DESIGN CONSIDERATIONS (CONTINUED)



NOTE A: The thermal pad is electrically isolated from all terminals in the package.

Figure 51. Views of Thermally Enhanced DGN Package

Although there are many ways to properly heatsink this device, the following steps illustrate the recommended approach.

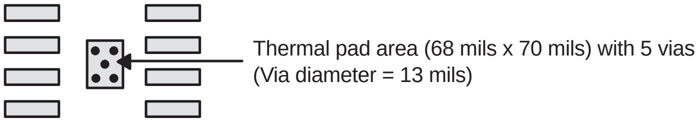


Figure 52. PowerPAD™ PCB Etch and Via Pattern

1. Prepare the PCB with a top side etch pattern as shown in Figure 52. There should be etch for the leads as well as etch for the thermal pad.
2. Place five holes in the area of the thermal pad. These holes should be 13 mils in diameter. Keep them small so that solder wicking through the holes is not a problem during reflow.
3. Additional vias may be placed anywhere along the thermal plane outside of the thermal pad area. This helps dissipate the heat generated by the THS405xDGN IC. These additional vias may be larger than the 13-mil diameter vias directly under the thermal pad. They can be larger because they are not in the thermal pad area to be soldered so that wicking is not a problem.
4. Connect all holes to the internal ground plane.
5. When connecting these holes to the ground plane, *do not* use the typical web or spoke via connection methodology. Web connections have a high thermal resistance connection that is useful for slowing the heat transfer during soldering operations. This makes the soldering of vias that have plane connections easier. In this application, however, low thermal resistance is desired for the most efficient heat transfer. Therefore, the holes under the THS405xDGN package should make their connection to the internal ground plane with a complete connection around the entire circumference of the plated-through hole.
6. The top-side solder mask should leave the terminals of the package and the thermal pad area with its five holes exposed. The bottom-side solder mask should cover the five holes of the thermal pad area. This prevents solder from being pulled away from the thermal pad area during the reflow process.
7. Apply solder paste to the exposed thermal pad area and all of the IC terminals.
8. With these preparatory steps in place, the THS405xDGN IC is simply placed in position and run through the solder reflow operation as any standard surface-mount component. This results in a part that is properly installed.

APPLICATION INFORMATION

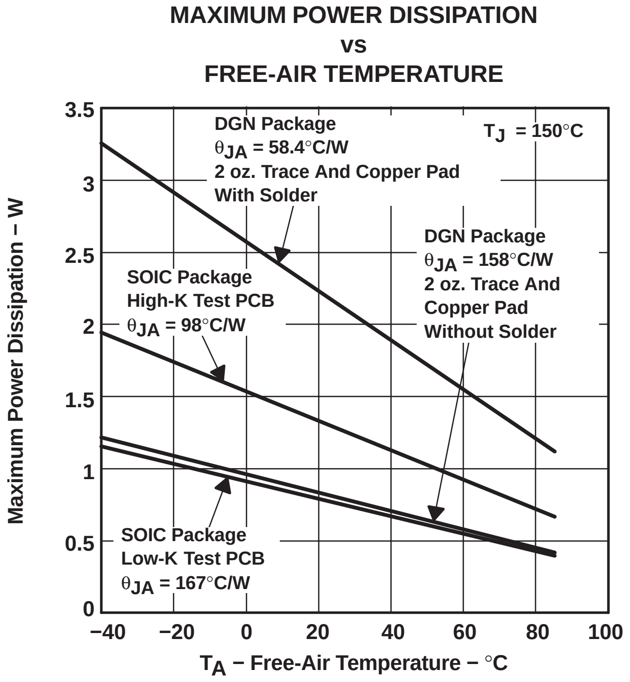
GENERAL POWERPAD™ DESIGN CONSIDERATIONS (CONTINUED)

The actual thermal performance achieved with the THS405xDGN in its PowerPAD™ package depends on the application. In the example above, if the size of the internal ground plane is approximately 3 inches × 3 inches (or 76.2 mm × 76.2 mm), then the expected thermal coefficient, θ_{JA}, is about 58.4°C/W. For comparison, the non-PowerPAD™ version of the THS405x IC (SOIC) is shown. For a given θ_{JA}, the maximum power dissipation is shown in Figure 53 and is calculated by the following formula:

$$P_D = \left(\frac{T_{MAX} - T_A}{\theta_{JA}}\right)$$

Where:

P_D = Maximum power dissipation of THS405x IC (watts)
T_{MAX} = Absolute maximum junction temperature (150°C)
T_A = Free-ambient air temperature (°C)
$\theta_{JA} = \theta_{JC} + \theta_{CA}$
θ_{JC} = Thermal coefficient from junction to case
θ_{CA} = Thermal coefficient from case to ambient air (°C/W)



NOTE A: Results are with no air flow and PCB size = 3”× 3”

Figure 53. Maximum Power Dissipation vs Free-Air Temperature

More complete details of the PowerPAD™ installation process and thermal management techniques can be found in the Texas Instruments Technical Brief, *PowerPAD™ Thermally Enhanced Package.* This document can be found at the TI web site (www.ti.com) by searching on the key word PowerPAD™. The document can also be ordered through your local TI sales office. Refer to literature number SLMA002 when ordering.

APPLICATION INFORMATION

GENERAL POWERPAD™ DESIGN CONSIDERATIONS (CONTINUED)

The next consideration is the package constraints. The two sources of heat within an amplifier are quiescent power and output power. The designer should never forget about the quiescent heat generated within the device, especially devices with multiple amplifiers. Because these devices have linear output stages (Class A-B), most of the heat dissipation is at low output voltages with high output currents. Figure 54 to Figure 57 show this effect, along with the quiescent heat, with an ambient air temperature of 50°C. Obviously, as the ambient temperature increases, the limit lines shown will drop accordingly. The area under each respective limit line is considered the safe operating area. Any condition above this line will exceed the amplifier's limits and failure may result. When using $V_{CC} = \pm 5$ V, there is generally not a heat problem, even with SOIC packages. But, when using $V_{CC} = \pm 15$ V, the SOIC package is severely limited in the amount of heat it can dissipate. The other key factor when looking at these graphs is how the devices are mounted on the PCB. The PowerPAD™ devices are extremely useful for heat dissipation. But, the device should always be soldered to a copper plane to fully use the heat dissipation properties of the PowerPAD™. The SOIC package, on the other hand, is highly dependent on how it is mounted on the PCB. As more trace and copper area is placed around the device, θ_{JA} decreases and the heat dissipation capability increases. The currents and voltages shown in these graphs are for the total package. For the dual amplifier package (THS4052), the sum of the RMS output currents and voltages should be used to choose the proper package. The graphs shown assume that both amplifier outputs are identical.

THS4051
MAXIMUM RMS OUTPUT CURRENT
vs
RMS OUTPUT VOLTAGE DUE TO THERMAL LIMITS

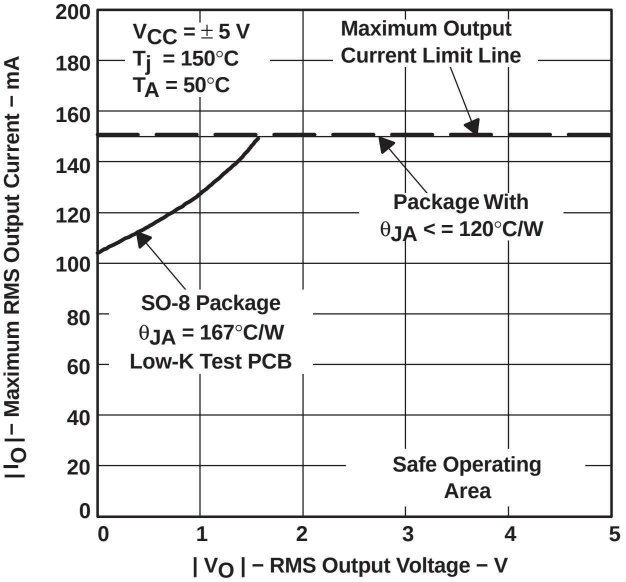


Figure 54

THS4051
MAXIMUM RMS OUTPUT CURRENT
vs
RMS OUTPUT VOLTAGE DUE TO THERMAL LIMITS

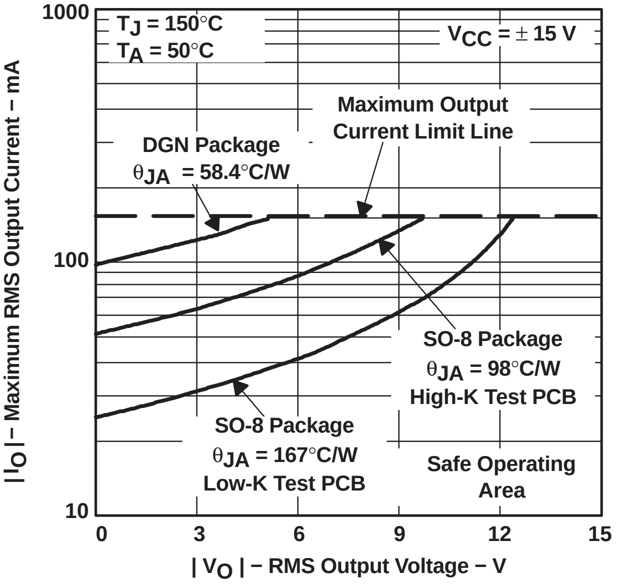


Figure 55

APPLICATION INFORMATION

GENERAL POWERPAD™ DESIGN CONSIDERATIONS (CONTINUED)

THS4052
MAXIMUM RMS OUTPUT CURRENT
vs
RMS OUTPUT VOLTAGE DUE TO THERMAL LIMITS

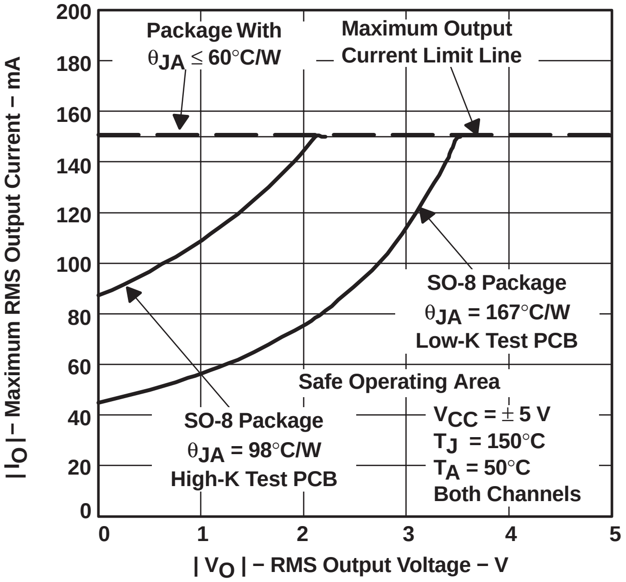


Figure 56

THS4052
MAXIMUM RMS OUTPUT CURRENT
vs
RMS OUTPUT VOLTAGE DUE TO THERMAL LIMITS

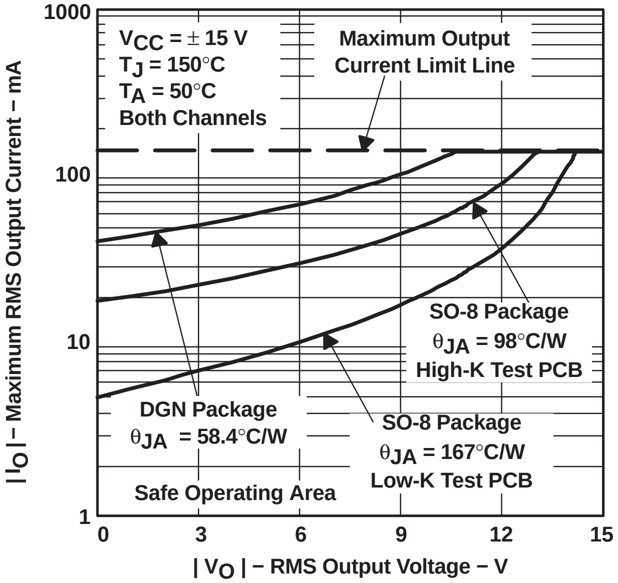


Figure 57

APPLICATION INFORMATION

EVALUATION BOARD

An evaluation board is available for the THS4051 (literature number SLOP220) and THS4052 (literature number SLOP234). This board has been configured for very low parasitic capacitance in order to realize the full performance of the amplifier. A schematic of the evaluation board is shown in Figure 58. The circuitry has been designed so that the amplifier may be used in either an inverting or noninverting configuration. For more information, please refer to the *THS4051 EVM User's Guide* or the *THS4052 EVM User's Guide*. To order the evaluation board, contact your local TI sales office or distributor.

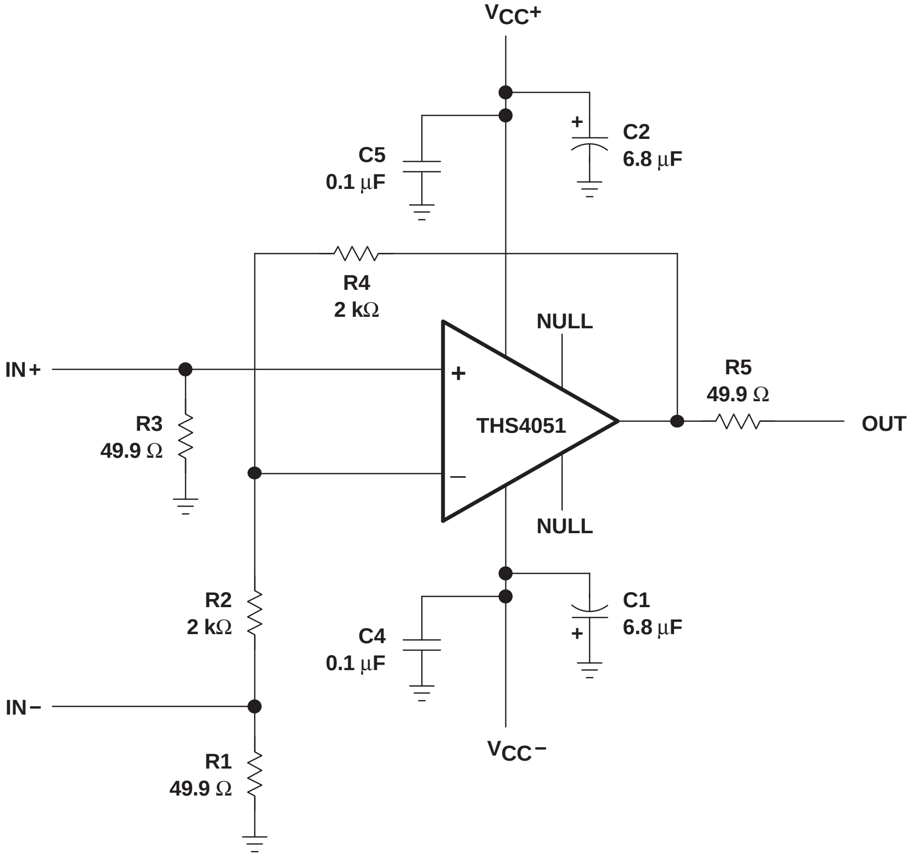


Figure 58. THS4051 Evaluation Board Schematic

PACKAGING INFORMATION

Orderable Device	Status [1]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [2]	Lead/Ball Finish	MSL Peak Temp [3]
THS4051CD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
THS4051CDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
THS4051CDGN	ACTIVE	MSOP-Power PAD	DGN	8	80	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
THS4051CDGNG4	ACTIVE	MSOP-Power PAD	DGN	8	80	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
THS4051CDGNR	ACTIVE	MSOP-Power PAD	DGN	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
THS4051CDGNRG4	ACTIVE	MSOP-Power PAD	DGN	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
THS4051CDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
THS4051CDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
THS4051ID	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
THS4051IDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
THS4051IDGN	ACTIVE	MSOP-Power PAD	DGN	8	80	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
THS4051IDGNG4	ACTIVE	MSOP-Power PAD	DGN	8	80	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
THS4051IDGNR	ACTIVE	MSOP-Power PAD	DGN	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
THS4051IDGNRG4	ACTIVE	MSOP-Power PAD	DGN	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
THS4051IDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
THS4051IDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
THS4052CD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
THS4052CDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
THS4052CDGN	ACTIVE	MSOP-Power PAD	DGN	8	80	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
THS4052CDGNG4	ACTIVE	MSOP-Power PAD	DGN	8	80	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
THS4052CDGNR	ACTIVE	MSOP-	DGN	8	2500	Green (RoHS &	CU NIPDAU	Level-1-260C-UNLIM

Orderable Device	Status [1]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [2]	Lead/Ball Finish	MSL Peak Temp [3]
		Power PAD				no Sb/Br)		
THS4052CDGNRG4	ACTIVE	MSOP-Power PAD	DGN	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
THS4052CDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
THS4052CDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
THS4052ID	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
THS4052IDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
THS4052IDGN	ACTIVE	MSOP-Power PAD	DGN	8	80	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
THS4052IDGNG4	ACTIVE	MSOP-Power PAD	DGN	8	80	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
THS4052IDGNR	ACTIVE	MSOP-Power PAD	DGN	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
THS4052IDGNRG4	ACTIVE	MSOP-Power PAD	DGN	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
THS4052IDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
THS4052IDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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OTHER QUALIFIED VERSIONS OF THS4051 :

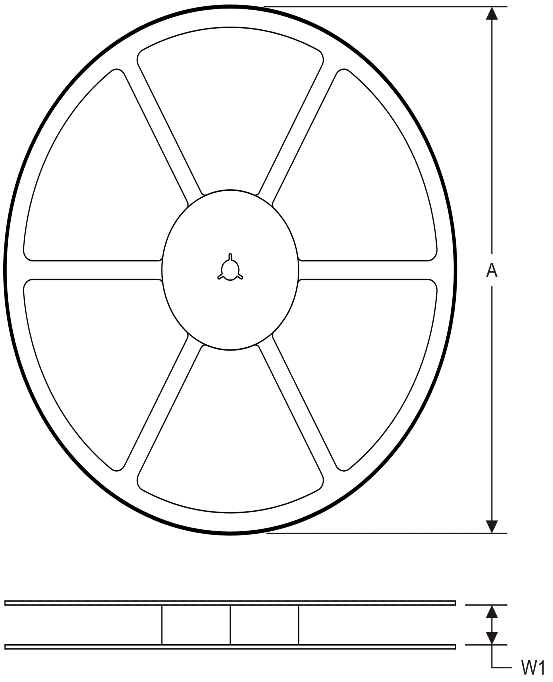
- Military: THS4051M

NOTE: Qualified Version Definitions:

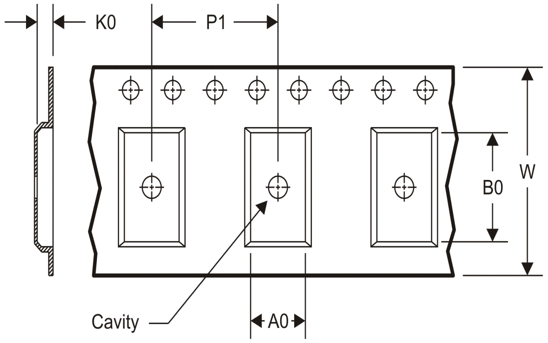
  - Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



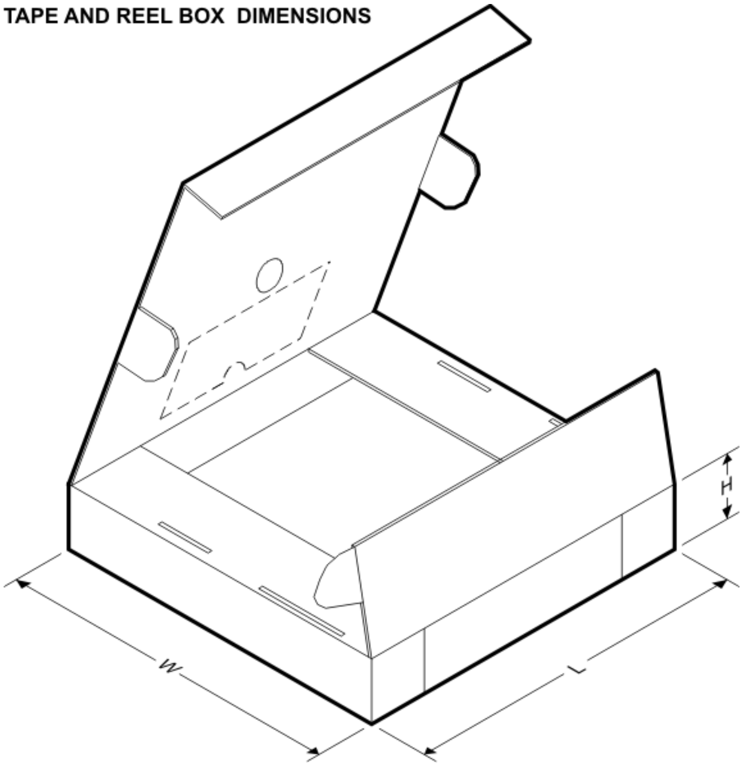
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
THS4051CDGNR	MSOP-PowerPAD	DGN	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
THS4051CDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
THS4051IDGNR	MSOP-PowerPAD	DGN	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
THS4051IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
THS4052CDGNR	MSOP-PowerPAD	DGN	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
THS4052CDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
THS4052IDGNR	MSOP-PowerPAD	DGN	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
THS4052IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

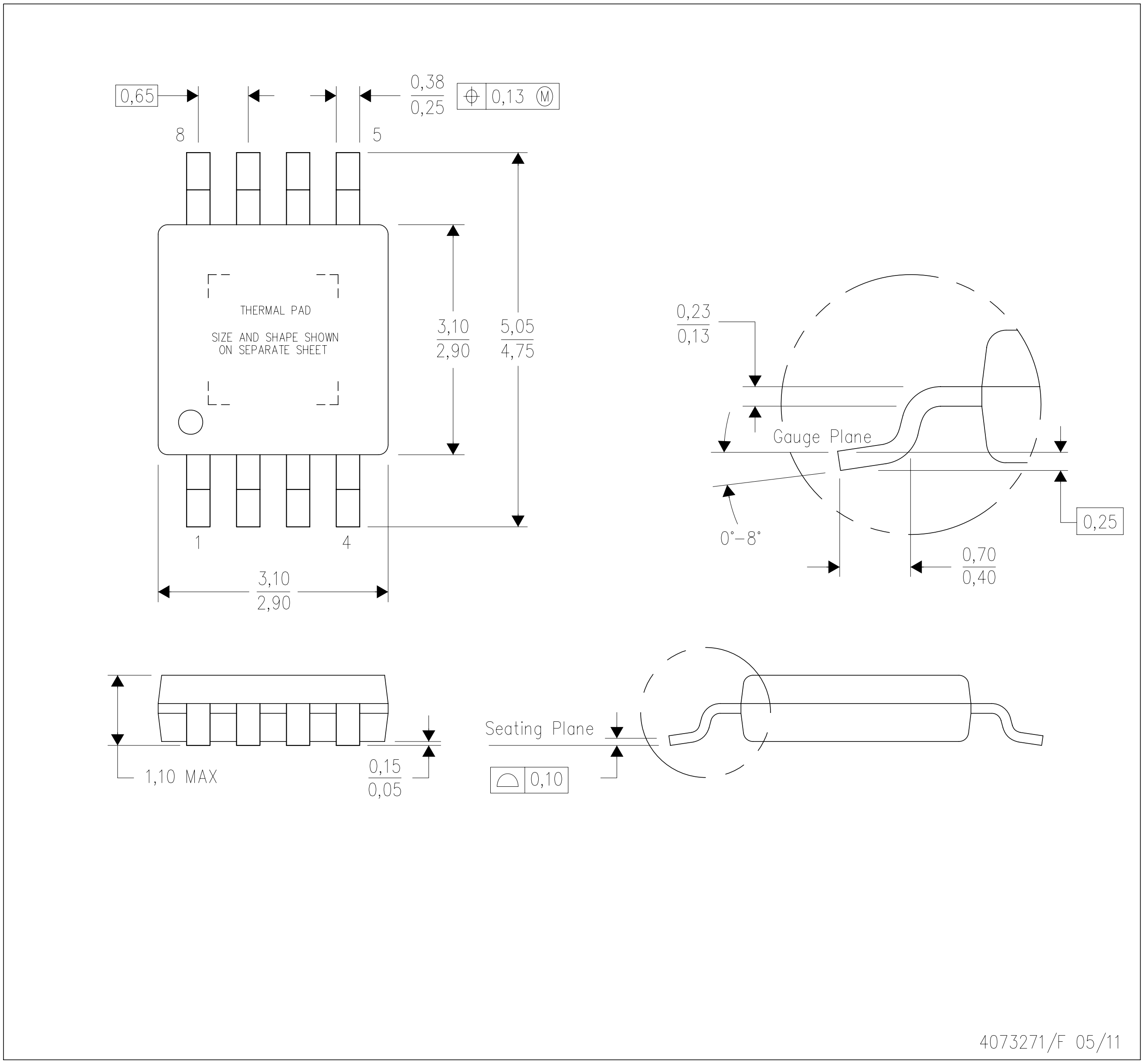
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
THS4051CDGNR	MSOP-PowerPAD	DGN	8	2500	358.0	335.0	35.0
THS4051CDR	SOIC	D	8	2500	367.0	367.0	35.0
THS4051IDGNR	MSOP-PowerPAD	DGN	8	2500	358.0	335.0	35.0
THS4051IDR	SOIC	D	8	2500	367.0	367.0	35.0
THS4052CDGNR	MSOP-PowerPAD	DGN	8	2500	358.0	335.0	35.0
THS4052CDR	SOIC	D	8	2500	367.0	367.0	35.0
THS4052IDGNR	MSOP-PowerPAD	DGN	8	2500	358.0	335.0	35.0
THS4052IDR	SOIC	D	8	2500	367.0	367.0	35.0

DGN (S-PDSO-G8) PowerPAD™ PLASTIC SMALL OUTLINE



NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion.
- D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http: //www.ti.com>.
- E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
- F. Falls within JEDEC MO–187 variation AA–T

PowerPAD is a trademark of Texas Instruments.

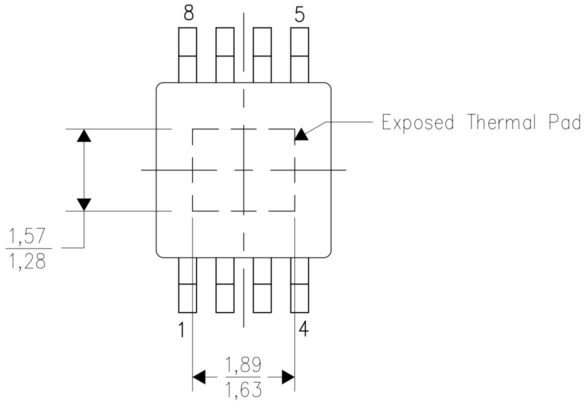
DGN (S-PDSO-G8) PowerPAD™ PLASTIC SMALL OUTLINE

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Top View

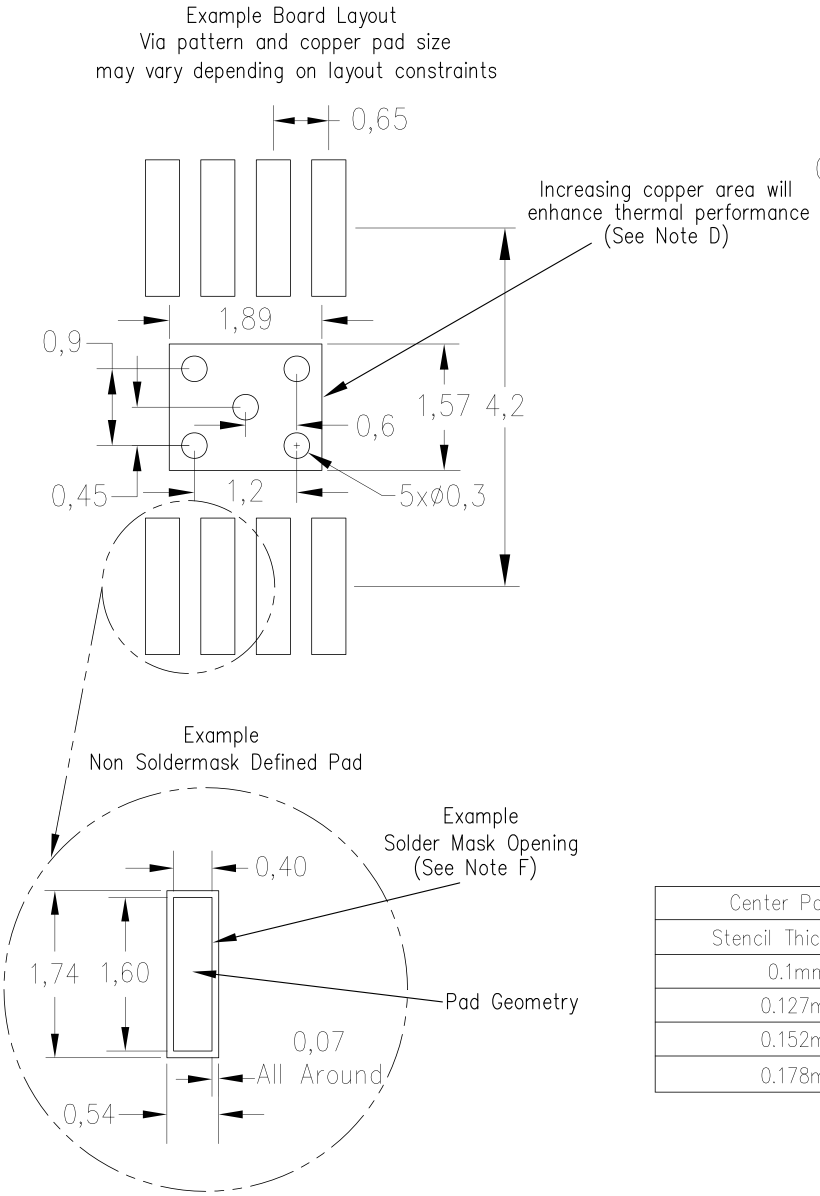
Exposed Thermal Pad Dimensions

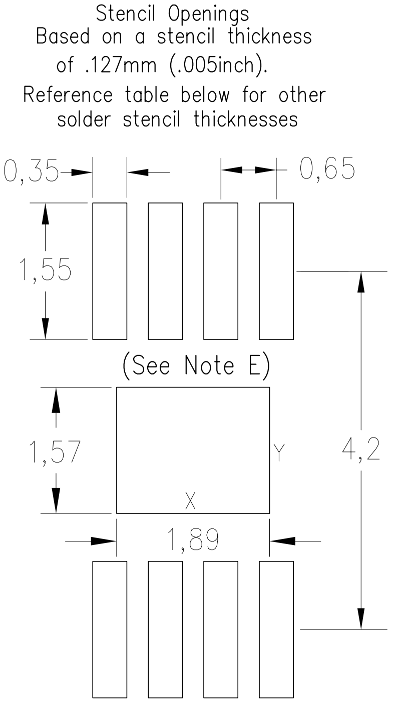
4206323-2/I 12/11

NOTE: All linear dimensions are in millimeters

PowerPAD is a trademark of Texas Instruments

DGN (R-PDSO-G8) PowerPAD™ PLASTIC SMALL OUTLINE





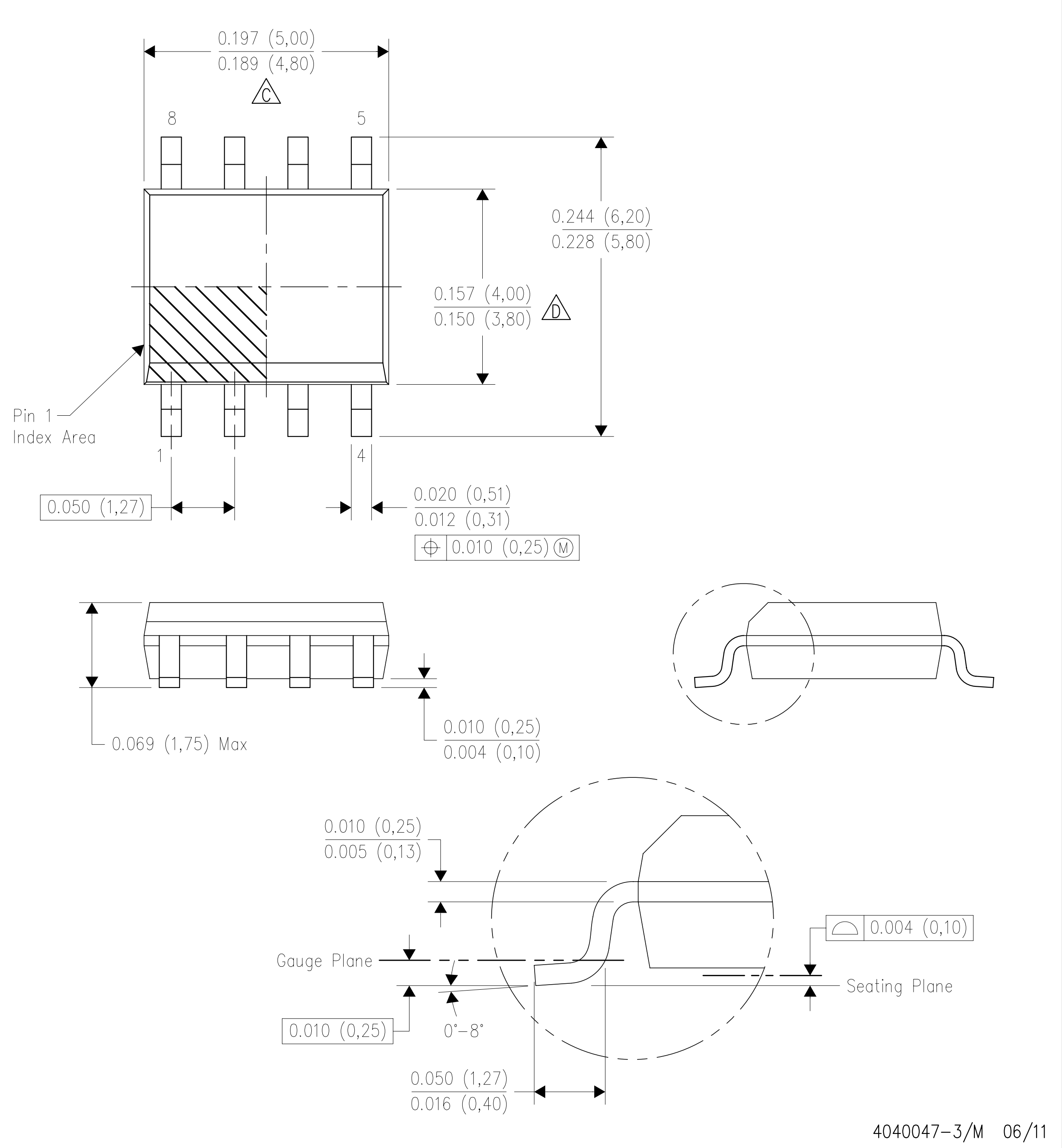
Center Power Pad Solder Stencil Opening		
Stencil Thickness	X	Y
0.1mm	2.0	1.7
0.127mm	1.89	1.57
0.152mm	1.75	1.45
0.178mm	1.65	1.35

4207737-2/E 04/11

NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
- D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http: //www.ti.com>. Publication IPC-7351 is recommended for alternate designs.
- E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.
- F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

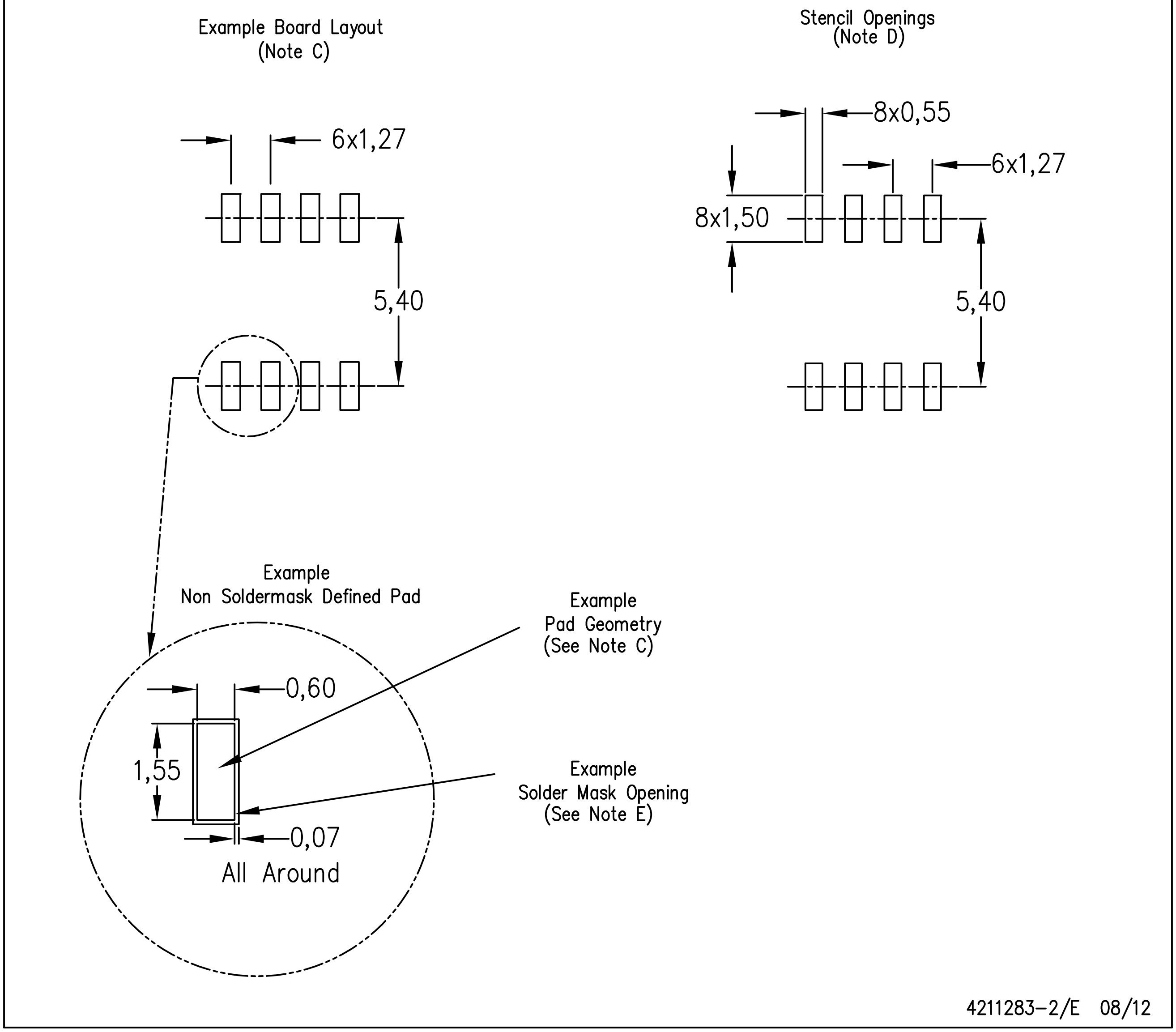
PowerPAD is a trademark of Texas Instruments

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS–012 variation AA.

D (R-PDSO-G8) PLASTIC SMALL OUTLINE



4211283-2/E 08/12

NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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Only those TI components which TI has specifically designated as military grade or “enhanced plastic” are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components which have ***not*** been so designated is solely at the Buyer's risk, and that Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

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DLP® Products	www.dlp.com	Consumer Electronics	www.ti.com/consumer-apps
DSP	dsp.ti.com	Energy and Lighting	www.ti.com/energy
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Microcontrollers	microcontroller.ti.com	Video and Imaging	www.ti.com/video
RFID	www.ti-rfid.com		
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